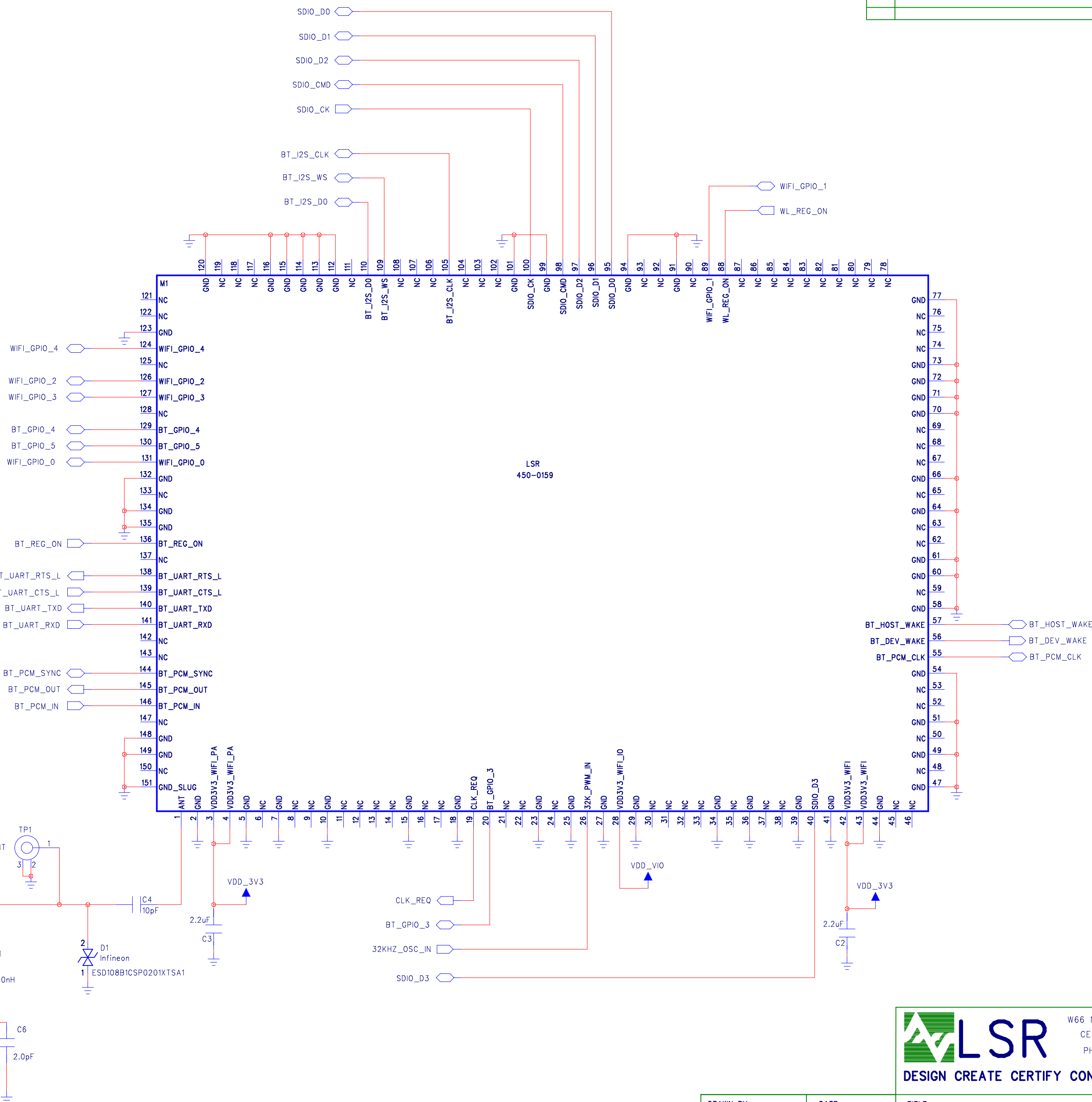
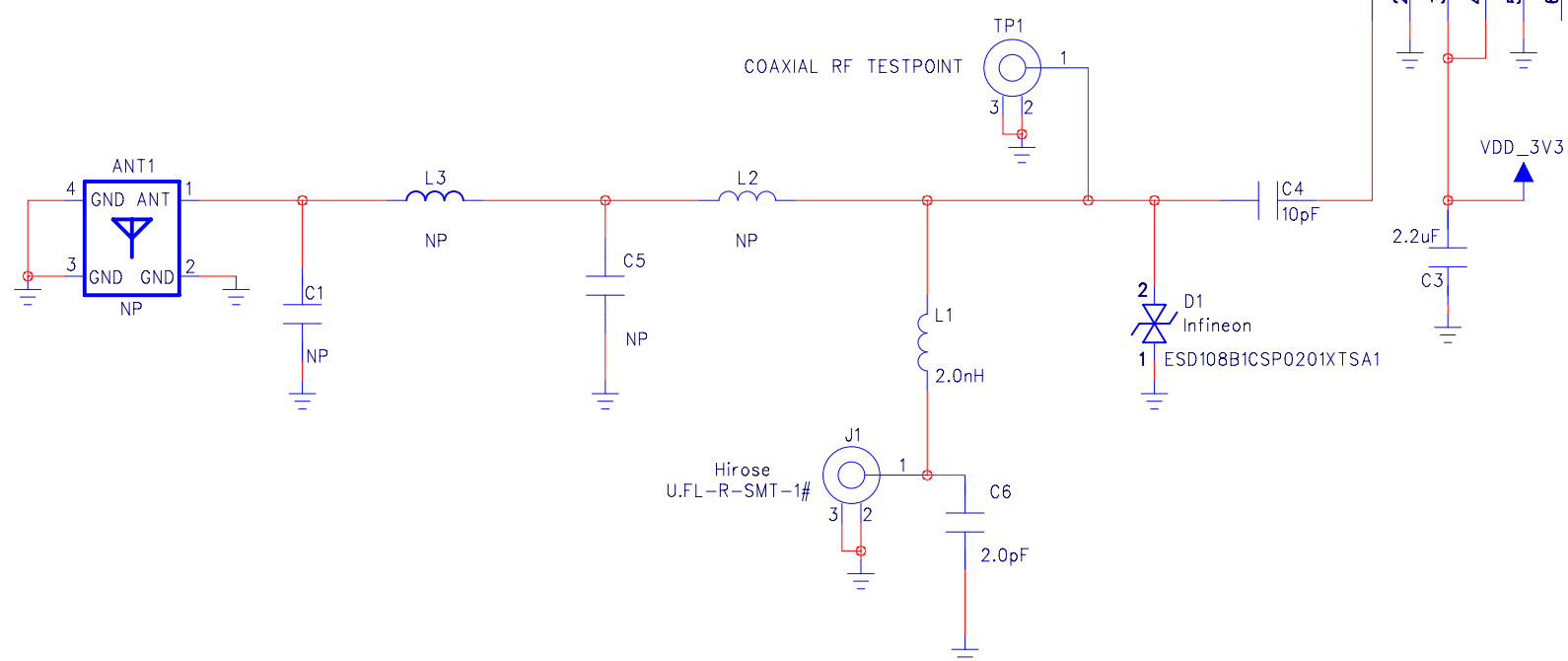


The diagram illustrates the pin configuration for the ESP8266 module. It shows 27 pins (P1 to P27) and their connections. The pins are organized as follows:

- Left Side (P1 to P14):**
  - P1: Ground
  - P2: BT\_PCM\_SYNC
  - P3: BT\_PCM\_IN
  - P4: BT\_PCM\_OUT
  - P5: SOURCE VDD\_3V3
  - P6: Ground
  - P7: WIFI\_GPIO\_4
  - P8: WIFI\_GPIO\_3
  - P9: WIFI\_GPIO\_2
  - P10: WIFI\_GPIO\_1
  - P11: WIFI\_GPIO\_0
  - P12: WL\_REG\_ON
  - P13: CLK\_REQ
  - P14: Ground
- Bottom (P15 to P27):**
  - P15: BT\_GPIO\_3
  - P16: BT\_GPIO\_4
  - P17: BT\_GPIO\_5
  - P18: Ground
  - P19: 32KHz\_OSC\_IN
  - P20: SOURCE VDD\_VIO
  - P21: BT\_REG\_ON
  - P22: SDIO\_D0
  - P23: SDIO\_D1
  - P24: Ground
  - P25: SDIO\_D2
  - P26: SDIO\_CMD
  - P27: SDIO\_D3
- Top (P42 to P45):**
  - P42: Ground
  - P43: Ground
  - P44: Ground
  - P47: Ground
  - P46: Ground
  - P45: Ground
- Right Side (P46 to P49):**
  - P46: BT\_HOST\_WAKE
  - P47: BT\_DEV\_WAKE
  - P48: BT\_PCM\_CLK
  - P49: BT\_I2S\_WS
  - P50: BT\_I2S\_D0
  - P51: BT\_I2S\_CLK
  - P52: BT\_UART\_RXD
  - P53: BT\_UART\_TXD
  - P54: BT\_UART\_CTS\_L
  - P55: BT\_UART\_RTS\_L
  - P56: Ground
  - P57: SDIO\_CLK
  - P58: Ground
  - P59: Ground



REVISION RECORD		
REV.	DESCRIPTION:	DATE:
1.0	INITIAL RELEASE ECN-154-2015	8/5/15
3.0	ECN-222-2015	12/8/15
3.1	ECN-244-2015	12/16/15
3.2	ECN-7-2016	1/11/16



PCB1  
LSR  
750-00740  
Sterling-LWB Module PCB



DRAWN BY: MIKE HENNIG	DATE: 07/02/2015	TITLE: SCHEMATIC		
CHECKED BY: BRIAN PETTED	DATE: 08/05/2015	PROJECT: Sterling-LWB, U.FL		
HW APPROVED BY: JMB	DATE: 08/05/2015	SIZE: C	DRAWING NO: 332-00740	REV: 3.2
FILENAME: 332-00740-R3.2.sch		SCALE: DO NOT		SHEET: 1 OF