Datasheet

SDC-MSD40NBT

Version 5.12

REVISION HISTORY

Version	Rev. Date	Change Description	Approved By
1.0	08/01/11	Initial Release	
1.1	08/08/11	Updated I/O information for select pins in the Pin table	
1.2	08/26/11	Added PCM Timing information	
1.3	10/05/11	Added BT/antenna note, MSD30AG/MSD40NBT Pin Comparison table, MSD40NBT/T-Board image, MSD40NBT schematic	
1.4	10/27/11	Added PCM defaults	
1.5	12/01/11	General edits including: revisions to PIN table, finalized specifications data, added *Integration Consideration* section	
1.6	12/02/11	Updated the MSD40NBT schematic and current Consumption numbers in the Specifications table; Added series resistors information to the "Integration Considerations" section and added product image	
1.7	12/23/11	Added revised mechanical drawing	
1.8	01/03/12	Updated Specifications table	
1.9	02/08/12	Added pin note and power notes	
1.10	02/13/12	Updated mechanical drawing with new side view measurement New product photo and new T-Board photo with Rev. 6 device	
1.11	02/16/12	Updated mechanical drawings spacer image and transmit power numbers	
2.0	6/29/12	Updated BT Transmit Power	
2.1	7/5/12	Updated Receiver Sensitivity values	
2.2	7/11/12	Updated notes regarding CMD pull-ups	
2.3	8/15/12	Updated Operating Temperature	
3.0	10/15/12	Updated format (converted to Laird) and Mounting section with revised spacer information; Added AS/NZS (Australia, New Zealand) certifications; Changed pin name of Pin 12 and updated AS/NZS links	
3.1	12/4/12	Made corrections to "Recommended Operating Conditions and DC Electrical Characteristics" table	
4.0	1/29/12	Updated Receive Sensitivity Data	
4.1	1/30/13	Updated 5GHz frequency and channel data	
4.2	17 May 2013	Added BT Priority *Important* note to the Block Diagram.	
4.3	11 July 2013	Fixed ICC certification error (changed IC ID: 6616A-SDCSSD40L to IC ID: 6616A-SDCMSD40NBT)	
4.4	20 Sept 2013	Updated Operating and Storage Temperature	Dale Chapman
4.5	11 Oct 2013	Removed references to summitdata.com.	Sue White
4.6	26 Feb 2014	Added BT SIG certification section	Jonathan Kaye
4.7	19 Mar 2014	Added note regarding the following pins: CHIP_PWD_L, SYS_RST_L, BT_RST_L, VDDIO_DR	Andrew Chen
4.8	20 Oct 2014	Updated Hardware Schematic.	Andrew Chen
4.9	19 Oct 2015	Added **Approved By** column; updated or removed links	Sue White

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Version	Rev. Date	Change Description	Approved By
5.0	12 Aug 2016	Changed *Hardware Integration Guide* to *Datasheet.*	Sue White
5.1	16 Sept 2016	Added the EU Declaration of Conformity	Sue White
5.2	21 Feb 2017	Updated FCC data to 24 non-overlapping channels	Jay White
5.3	09 May 2017	Updated CE/EU Declaration of Conformity section	Maggie Teng
5.4	05 June 2017	Updated CE DoC with new RED standards	Tom Smith
5.5	07 June 2017	Fixed errors in the DoC	Maggie Teng
5.6	20 June 2017	Changed **EN 301 893 v2.1.0 (2017-03)** to **EN 301 893 v2.1.1 (2017-05)**	Tom Smith
5.7	19 Dec 2017	Removed references to MIC (Japan) certification	Jay White
5.8	13 July 2018	Updated IC Regulatory section	Maggie Teng
5.9	25 Oct 2019	Updated warranty information – changed three years to one year	Jay White
5.10	03 Sept 2020	Updated EU Regulatory section	Ryan Urness
5.11	29 Oct 2020	Updated Regulatory information	Ryan Urness
5.12	21 Feb 2021	Moved detailed regulatory information to a separate document	Jonathan Kaye

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1 SCOPE

This document describes key hardware aspects of the SDC-MSD40NBT radio module. This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from a number of sources and includes information found in the Broadcom BCM4329 data sheet issued in June of 2009.

Contact Laird or visit the MSD40NBT page of the Laird website for the newest version of this document.

2 OPERATIONAL DESCRIPTION

This device is an SDC-MSD40NBT radio module which supports IEEE 802.11a/b/g/n standards via an SDIO (Secure Digital Input/Output) interface and Bluetooth version 2.1 via a serial UART (Universal Asynchronous Receiver/Transmitter) interface. The radio operates in unlicensed portions of the 2.4 GHz and 5 GHz radio frequency spectrum. The device is compliant with IEEE 802.11a, 802.11b, 802.11g, and 802.11n standards using Direct Sequence Spread Spectrum (DSSS) and Orthogonal Frequency Division Multiplexing (OFDM), and supports Bluetooth 2.1 using Frequency Hopping Spread Spectrum (FHSS). The device supports all 802.11a, 802.11b, 802.11g, 802.11n, and Bluetooth data rates and automatically adjusts data rates and operational modes based on various environmental factors.

When operating on channels in the UNII-2 and UNII-2 Extended bands that are in the 5GHz portion of the frequency spectrum and are subject to Dynamic Frequency Selection requirements, the SDC-MSD40NBT fully conforms to applicable regulatory requirements. In the event that specified types of radar are detected by the network infrastructure, the SDC-MSD40NBT fully conforms to commands from the infrastructure for radar avoidance.

The SDC-MSD40NBT interfaces to host devices via a 60-pin connector. The device is based on the Broadcom BCM4329chip which is an integrated device providing a Media Access Controller (MAC), a Physical Layer Controller (PHY or baseband processor), and fully integrated dual-band radio transceiver. To maximize operational range, the SDC-MSD40NBT incorporates a 5 GHz power amplifier (PA) to increase transmit power. The frequency stability for both 2.4 GHz (802.11b and 802.11g) and 5 GHz (802.11a) operation is +/- 20 ppm.

The SDC-MSD40NBT has its own RF shielding and does not require shielding provided by the host device into which it is installed in order to maintain compliance with applicable regulatory standards. As such, the device may be tested in a standalone configuration via an extender card.

The device buffers all data inputs so that it will comply with all applicable regulations even in the presence of over-modulated input from the host device. Similarly, the SDC-SSD40NBT incorporates power regulation to comply with all applicable regulations even when receiving excess power from the host device.

The SDC-MSD40NBTprovides two unique U.FL type antenna connectors to support dual band transmit and receive diversity. Supported host device antenna types include dipole and monopole antennas.

Regulatory operational requirements are included with this document and may be incorporated into the operating manual of any device into which the SDC-MSD40NBT is installed. The SDC-MSD40NBT is designed for installation into mobile devices such as vehicle mount data terminals (which typically operate at distances greater than 20 cm from the human body) and portable devices such as handheld data terminals (which typically operate at distances less than 20 cm from the human body). See “Documentation Requirements” for more information.

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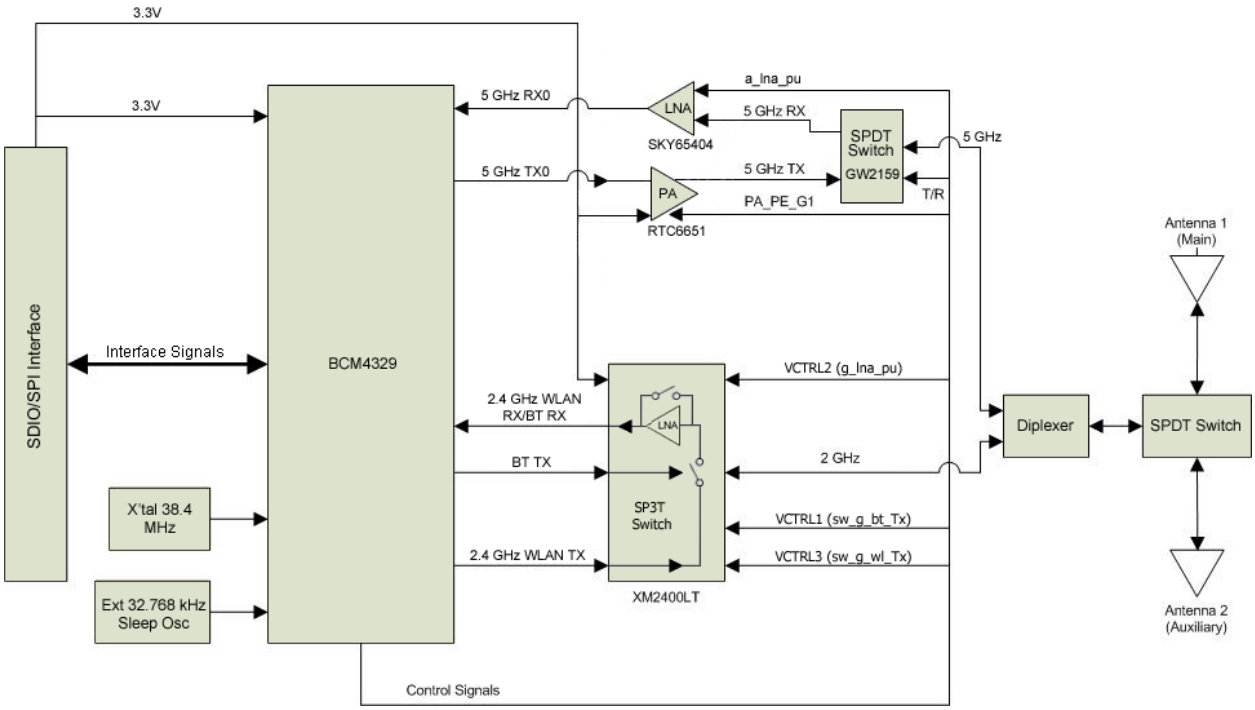
3 Block Diagram



Note: Transmitter frequencies for Wi-Fi are 2412-2462 MHz and 5180-5805 MHz. Transmitter frequencies for BT are 2402-2480 MHz.

Note: BT functions on the AUX port and *not* on the Main port. For Wi-Fi and BT single-antenna implementations, the AUX port *must* be used.

IMPORTANT: When BT is transmitting high priority traffic (such as during a scan and/or when sending audio traffic) Wi-Fi receive is sent to the main antenna port (even when set to *AUX only)*. When high priority transmission ends, Wi-Fi receive functionality returns to the AUX port (when set to AUX only). For optimal Wi-Fi performance, we recommend that you populate both the Main and the AUX ports with an antenna.

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4 SPECIFICATIONS

Table 1: Specifications

Feature	Description
Physical Interface	Molex 54722-0607 60-pin connector (mates to Molex 55560-0607 60-pin connector)
Wi-Fi Interface	1-bit or 4-bit Secure Digital I/O
Bluetooth Interface	Host Controller Interface (HCI) using High Speed UART
Antenna Interface	2 Hirose U.FL connectors for dual-band antenna diversity IMPORTANT: When using a single antenna, it MUST be connected to the Auxiliary (AUX) port. BT functions on the AUX port and not the Main port. For WiFi/BT single-antenna implementations, the AUX port must be used.
Main Chip	Broadcom BCM4329
Input Voltage Requirements	3.3 VDC ± 10% (core)
I/O Signaling Voltage	3.3 VDC ± 10%
Average Current Consumption, VDDIO = 3.3 volts (At maximum transmit power setting) ***Note:*** Standby *refers to the radio operating in PM1 powersave mode.*	**802.11a (with BT in standby)** Transmit: 282 mA (931 mW) Receive: 92 mA (304 mW) Standby: TBD **802.11b (with BT in standby)** Transmit: 314 mA (1036 mW) Receive: 92 mA (304 mW) Standby: TBD **802.11g (with BT in standby)** Transmit: 288 mA (950 mW) Receive: 92 mA (304 mW) Standby: TBD **802.11n (2.4 GHz) (with BT in standby)** Transmit: 292 mA (964 mW) Receive: 92 mA (304 mW) Standby: TBD **802.11n (5 GHz) (with BT in standby)** Transmit: 270 mA (891 mW) Receive: 92 mA (304 mW) Standby: TBD **Bluetooth (with Wi-Fi in standby)** Transmit: TBD mA (TBD mW) Receive: TBD mA (TBD mW)
Operating Temperature	-30° to 80°C (-22° to 176°F)
Operating Humidity	10 to 90% (non-condensing)
Storage Temperature	-30° to 85°C (-22° to 185°F)

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Feature	Description
Storage Humidity	10 to 90% (non-condensing)
Maximum Electrostatic Discharge	8 kV
Length	32 mm (1.26 in.)
Width	22 mm (0.87 in.)
Thickness	5.05mm (0.17 in.)
Weight	3.0 g (0.11 oz.)
Mounting	60-pin connector, mounting holes (M2 screws)
Wi-Fi Media	Direct Sequence-Spread Spectrum (DSSS) Complementary Code Keying (CCK) Orthogonal Frequency Divisional Multiplexing (OFDM)
Bluetooth Media	Frequency Hopping Spread Spectrum (FSSS)
Wi-Fi Media Access Protocol	Carrier sense multiple access with collision avoidance (CSMA/CA)
Network Architecture Types	Infrastructure and ad hoc
Wi-Fi Standards	IEEE 802.11a, 802.11b, 802.11d, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n
Bluetooth Standards	Bluetooth version 2.1 with Enhanced Data Rate
Wi-Fi Data Rates Supported	802.11a (OFDM) 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11b (DSSS, CCK) 1, 2, 5.5, 11 Mbps 802.11g (OFDM) 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n (OFDM, MCS 0-7) 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2 Mbps
Wi-Fi Modulation	BPSK @ 1, 6, 6.5, 7.2 and 9 Mbps QPSK @ 2, 5.5, 11, 12, 13, 14.4,18, 19.5 and 21.7 Mbps 16-QAM @ 24, 26, 28.9, 36, 39 and 43.3 Mbps 64-QAM @ 48, 52, 54, 57.8, 58.5, 65, and 72.2 Mbps
802.11n Spatial Streams	1 (Single Input, Single Output)
Supported Bluetooth Data Rates	1, 2, 3 Mbps
Bluetooth Modulation	GFSK@ 1 Mbps π/4-DQPSK@ 2 Mbps 8-DPSK@ 3 Mbps
Supported Regulatory Domains	FCC EU MIC (Japan) KC (Korea)
Wi-Fi and Bluetooth 2.4 GHz Frequency Bands	EU: 2.4 GHz to 2.483 GHz FCC: 2.4 GHz to 2.483 GHz MIC (Japan): 2.4 GHz to 2.495 GHz KC: 2.4 GHz to 2.483 GHz

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Feature	Description
Wi-Fi 2.4 GHz Operating Channels	EU:13 (3 non-overlapping) MIC (Japan):14 (4 non-overlapping) FCC:11 (3 non-overlapping) KCC:13 (3 non-overlapping)
5 GHz Frequency Bands	**EU** 5.15 GHz to 5.35 GHz 5.47 GHz to 5.725 GHz **FCC** 5.15 GHz to 5.35 GHz 5.47 GHz to 5.725 GHz 5.725 GHz to 5.82 GHz **MIC (Japan)** 5.15 GHz to 5.35 GHz **KC** 5.15 GHz to 5.35 GHz 5.725 GHz to 5.82 GHz
5 GHz Operating Channels	EU: 19 non-overlapping FCC: 24 non-overlapping MIC (Japan): 8 non-overlapping KC: 12 non-overlapping
Transmit Power ***Note:*** *Transmit power varies according to individual country regulations. All values nominal, +/-2 dBm.* ***Note:*** *Summit 40 series radios support a single spatial stream and 20 MHz channels only.*	**802.11a** 6 Mbps 16 dBm (40 mW) 54 Mbps 14 dBm (25 mW) **802.11b** 1 Mbps 17 dBm (50 mW) 11 Mbps 16 dBm (40 mW) **802.11g** 6 Mbps 15 dBm (32 mW) 54 Mbps 13 dBm (20 mW) **802.11n (2.4 GHz)** 6.5 Mbps (MCS0) 15 dBm (32 mW) 65 Mbps (MCS7) 11 dBm (13 mW) **802.11n (5 GHz)** 6.5 Mbps (MCS0) 16 dBm (40 mW) 65 Mbps (MCS7) 13 dBm (20 mW) **Bluetooth** 1 Mbps -0.5 dBm (1.1 mW) 2 Mbps -0.5 dBm (1.1 mW) 3 Mbps -0.5 dBm (1.1 mW)

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Feature	Description
Typical Receiver Sensitivity ***Note:*** *All values nominal, +/-3 dBm.*	**802.11a:** 6 Mbps -90 dBm 24 Mbps -84 dBm 54 Mbps -75 dBm (PER <= 10%) **802.11b:** 1 Mbps -96 dBm 11 Mbps -89 dBm (PER <= 10%) **802.11g:** 6 Mbps -90 dBm 24 Mbps -84 dBm 54 Mbps -74 dBm (PER <= 10%) **802.11n (2.4 GHz)** MCS0 Mbps -90 dBm MCS4 Mbps -79 dBm MCS7 Mbps -72 dBm **802.11n (5 GHz)** MCS0 Mbps -89 dBm MCS4 Mbps -79 dBm MCS7 Mbps -71 dBm **Bluetooth:** 1 Mbps TBD 2 Mbps TBD 3 Mbps TBD
Operating Systems Supported	Windows Mobile 6.5, 6.1, 6.0, 5.0 Windows Embedded CE 7.0, 6.0, 5.0 Linux, 2.6.x, 3.x.x kernel
Security	**Standards** Wireless Equivalent Privacy (WEP) Wi-Fi Protected Access (WPA) IEEE 802.11i (WPA2) **Encryption** Wireless Equivalent Privacy (WEP, RC4 Algorithm) Temporal Key Integrity Protocol (TKIP, RC4 Algorithm) Advanced Encryption Standard (AES, Rijndael Algorithm) Encryption Key Provisioning Static (40-bit and 128-bit lengths) Pre-Shared (PSK) Dynamic **802.1X Extensible Authentication Protocol Types** EAP-FAST PEAP-MSCHAPv2 EAP-TLS PEAP-TLS EAP-TTLS LEAP PEAP-GTC
Compliance	**EU** EN 300 328 EN 301 489-1 EN 301 489-17 EN 301 893 62311:2008 EN 50665:2017 EN 50385:2017 EU 2015/863 (RoHS 3) **FCC** 47 CFR FCC Part 15.247 47 CFR FCC Part 15.407 47 CFR FCC Part 2.1091 FCC Part 15 Subpart B Class B **ISED Canada** ICES-003 ANSI C63.4:2014 RSS-102 RSS-247 **AS/NZS** AS/NZS 4268:2017 **NCC** LP0002 (100-06-28) – Wi-Fi LP0002 (100-06-28) - Bluetooth

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Feature	Description
Certifications	Wi-Fi Alliance 802.11a, 802.11b, 802.11g , 802.11n WPA Enterprise WPA2 Enterprise Cisco Compatible Extensions (Version 4) Bluetooth SIG Qualification
Warranty	**Limited Lifetime**
	All specifications are subject to change without notice

5 Recommended Operating Conditions and DC Electrical Characteristics

Table 2: Recommended Operating Conditions and DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	DC Supply Voltage	3.0	3.3	3.6	V
VDD_IO	DC Supply Voltage (I/O)	1.8	-	3.3	V
V_{IL}	Low Level Input Voltage (VDDO = 3.3V)	-	-	0.8	V
V_{IH}	High Level Input Voltage (VDDO = 3.3V)	2.0	-	-	V
V_{OL}	Low Level Output Voltage (100 µA load)	-	-	0.2	V
V_{OH}	High Level Output Voltage (-100 µA load)	VDDIO– 0.2V	-	-	V
I_{IL}	Low Current Input	-	0.3	-	µA
I_{IH}	High Current Input	-	0.3	-	µA
I_{OL}	Low Current Output (VDDO = 3.3V, V_{OL} = 0.4V)	-	-	3.0	mA
I_{OH}	High Current Output (VDDO = 3.3V, V_{OH} = 2.9V)	-	-	3.0	mA
C_{IN}	Input Capacitance	-	-	5	pF
	BT UART Baud Rate	9600 bps	115.2 Kbps (default coming out of reset)	4 Mbps	bps/Kbps/Mbps

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5.1.1 SDIO Timing Requirements

The following figure (Figure 1) and table display SDIO default mode timing.

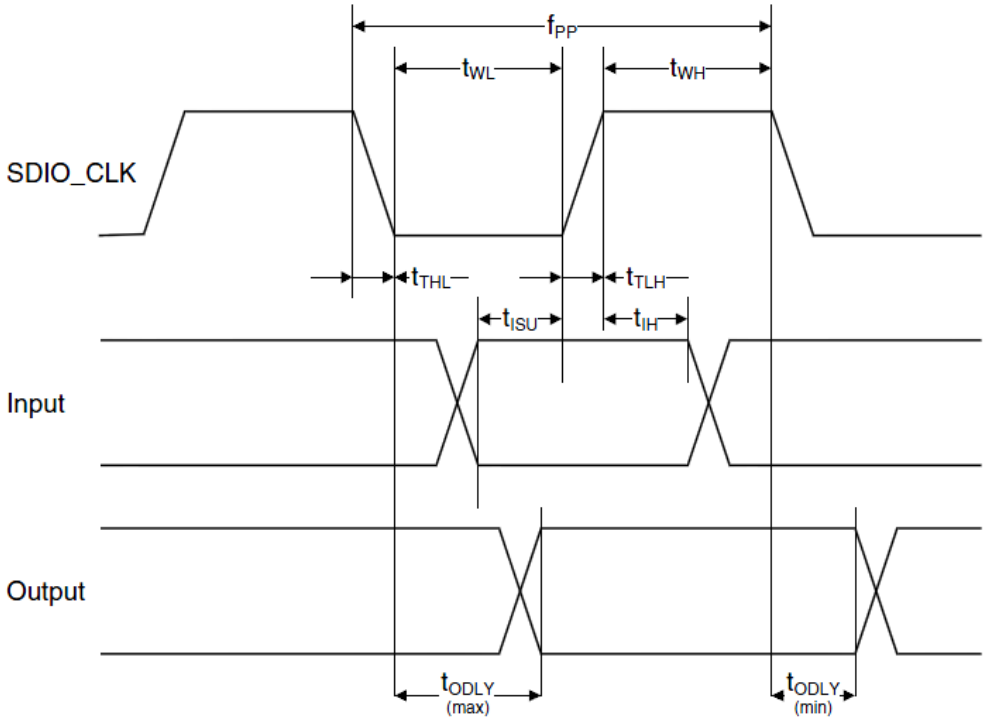

Figure 1: SDIO Default Mode Timing

Note: Timing is based on CL ≤ 40pF load on CMD and Data.

Table 3: SDIO Timing Requirements

Symbol	Parameter	Min.	Typ.	Max.	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL*)					
fPP	Frequency – Data Transfer mode	0	-	25	MHz
fOD	Frequency – Identification mode	0	-	400	kHz
tWL	Clock low time	10	-	-	ns
tWH	Clock high time	10	-	-	ns
tTLH	Clock rise time	-	-	10	ns
tTHL	Clock low time	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
tISU	Input setup time	5	-	-	ns
tIH	Input hold time	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
tODLY	Output delay time – Data Transfer mode	0	-	14	ns
tODLY	Output delay time – Identification mode	0	-	50	ns
*min(Vih) = 0.7 x VDDIO and max(ViL) = 0.2 x VDDIO.					

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5.1.2 UART Timing Requirements

The following figure (Figure 2) displays UART timing.

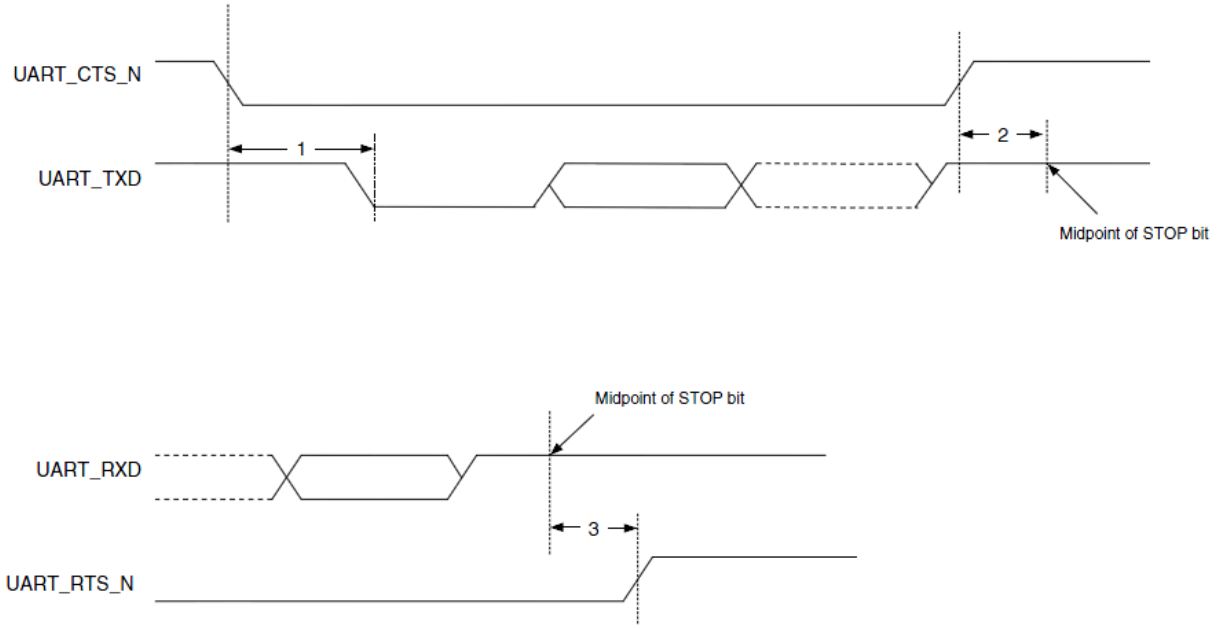

Figure 2: UART Timing Requirements

Note: The UART 4-wire interface supports Bluetooth 2.1 HCI Specification.

Table 4: UART Timing Requirements

Reference	Description	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low to UART_TXD valid	-	-	24	Baudout cycles
2	Setup time, BT_UART_CTShigh before midpoint of stop bit	-	-	10	ns
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	-	-	2	Baudout cycles

5.1.3 PCM Interface Timing

PCM Defaults	Long Frame Sync, Master Mode
Short Frame Sync, Master Mode	Long Frame Sync, Slave Mode
Short Frame Sync, Slave Mode	

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5.1.4 PCM Defaults

SCO Routing	PCM
Clock Mode	Master
Sync Mode	Master
Frame Type	Short

Interface Rate	512
Sample Interval	8khz
16 bit mono	

5.1.4.1 Short Frame Sync, Master Mode

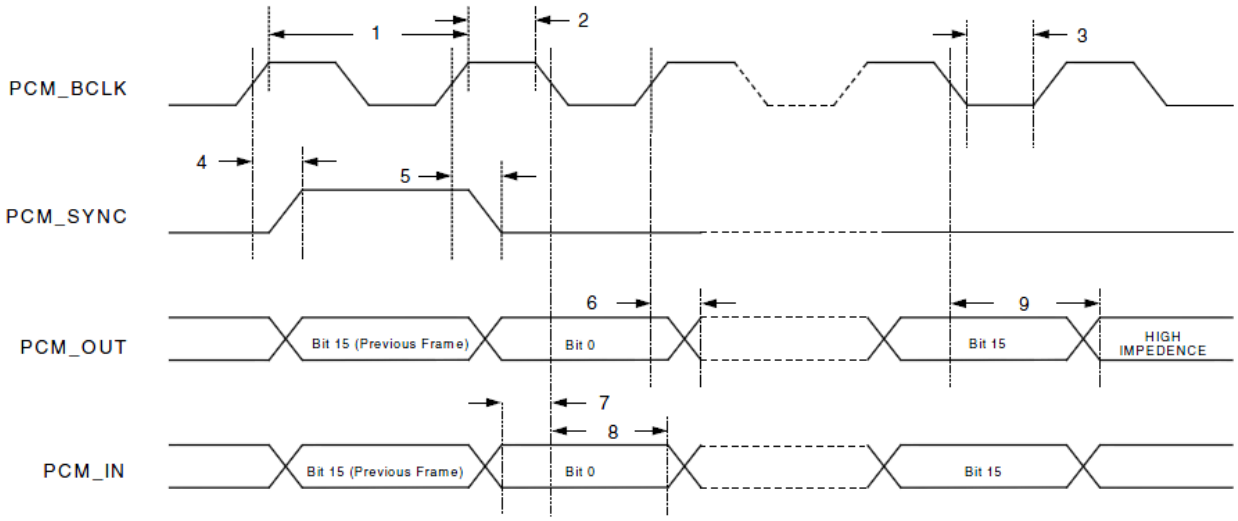

Figure 3: Short Frame Sync, Master Mode

Table 5: Short Frame Sync, Master Mode

Reference	Description	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	128	-	2048	kHz
2	PCM bit clock high time	128	-	-	ns
3	PCM bit clock low time	209	-	-	ns
4	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC high	-	-	50	ns
5	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC low	-	-	50	ns
6	Delay from BT_PCM_CLK rising edge to data valid on BT_PCM_OUT	-	-	50	ns
7	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	-	-	ns
8	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	-	-	ns
9	Delay from falling edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	-	-	50	ns

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5.1.4.2 Short Frame Sync, Slave Mode

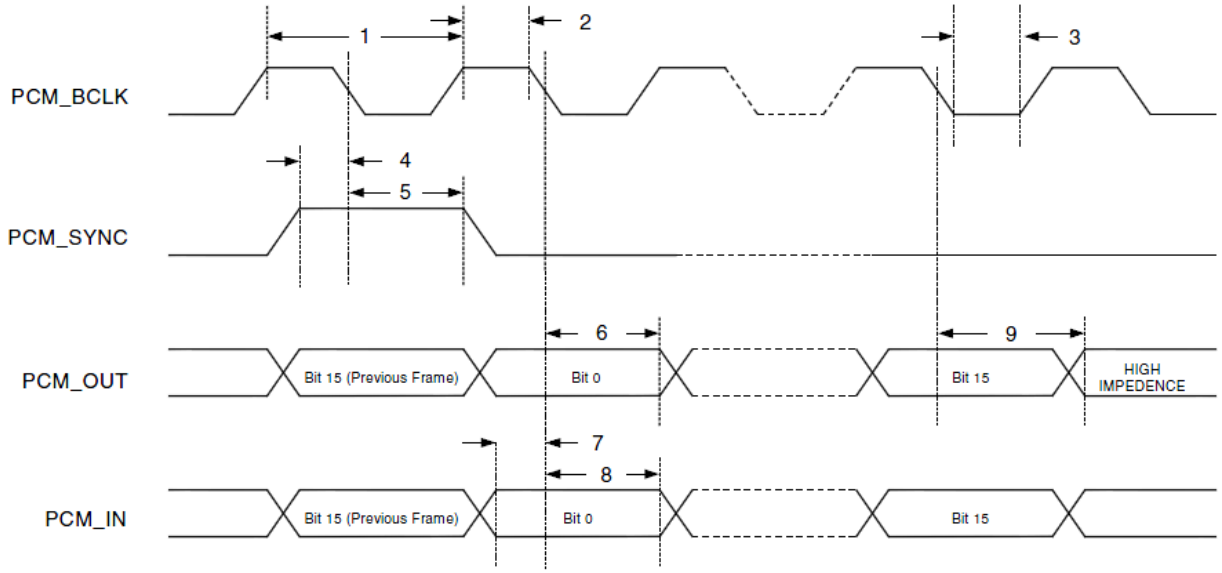

Figure 4: Short Frame Sync, Slave Mode

Table 6: Short Frame Sync, Slave Mode

Reference	Description	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	128	-	2048	kHz
2	PCM bit clock high time	209	-	-	ns
3	PCM bit clock low time	209	-	-	ns
4	Setup time for BT_PCM_SYNC before falling edge of BT_PCM_BCLK	50	-	-	ns
5	Hold time for BT_PCM_SYNC after falling edge of BT_PCM_CLK	10	-	-	ns
6	Hold time of BT_PCM_OUT after BT_PCM_CLK falling time	-	-	175	Ns
7	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	-	-	ns
8	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	-	-	ns
9	Delay from falling edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	-	-	100	ns

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5.1.4.3 Long Frame Sync, Master Mode

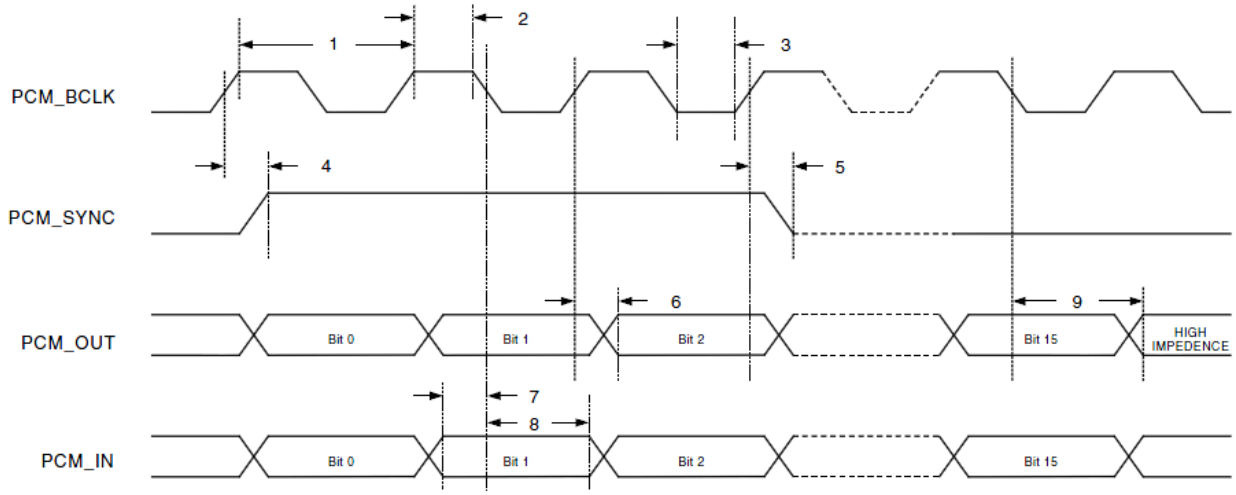

Figure 5: Long Frame Sync, Master Mode

Table 7: Long Frame Sync, Master Mode

Reference	Description	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	128	-	2048	kHz
2	PCM bit clock high time	209	-	-	ns
3	PCM bit clock low time	209	-	-	ns
4	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC high during first bit time	-	-	50	ns
5	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC low during third bit time	-	-	50	ns
6	Delay from BT_PCM_CLK rising edge to data valid on BT_PCM_OUT	-	-	50	ns
7	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	-	-	ns
8	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	-	-	ns
9	Delay from falling edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	-	-	50	ns

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5.1.4.4 Long Frame Sync, Slave Mode

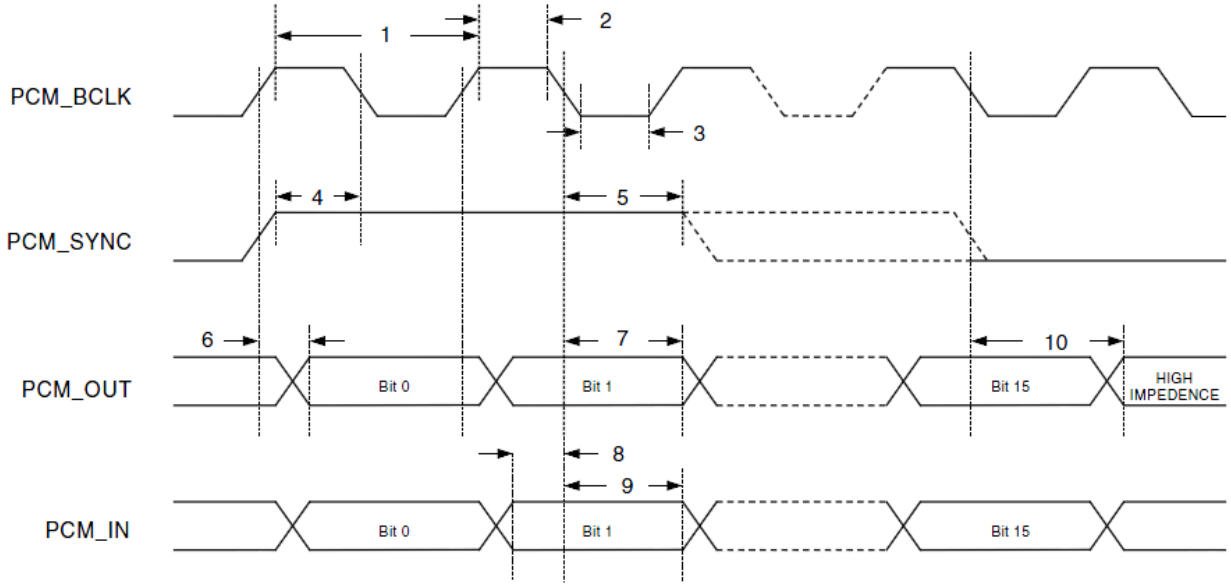

Figure 6: Long Frame Sync, Slave Mode

Table 8: Long Frame Sync, Slave Mode

Reference	Description	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	128	-	2048	kHz
2	PCM bit clock high time	209	-	-	ns
3	PCM bit clock low time	209	-	-	ns
4	Setup time for BT_PCM_SYNC before falling edge of BT_PCM_CLK during first bit time	50	-	-	ns
5	Hold time for BT_PCM_SYNC after falling edge of BT_PCM_CLK during second bit period. **Note:** BT_PCM_SYNC may go low any time from second bit period to last bit period.	10	-	-	ns
6	Delay from rising edge of BT_PCM_CLK or BT_PCM_SYNC (whichever is later) to data valid for first bit on BT_PCM_OUT	-	-	50	ns
7	Hold time of BT_PCM_OUT after BT_PCM_CLK falling edge	-	-	175	ns
8	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	-	-	ns
9	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	-	-	ns
10	Delay from falling edge of BT_PCM_CLK or BT_PCM_SYNC (whichever is later) during last bit in slot to BT_PCM_OUT becoming high impedance	-	-	100	

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6 Pin Definitions

Wi-Fi	Bluetooth	Wi-Fi/Bluetooth

Table 9: Pin Definitions

Pin Number	Pin Name	I/O	Voltage Reference	Description
1	GND	-		Ground
2	BT_UART_TXD	O	VDDIO	Bluetooth UART Serial Output
3	BT_PRIORITY	I/O	VDDIO	No connect. Not currently supported in the firmware. When not in use, leave open (float).
4	BT_GPIO_6	I/O	VDDIO	3.3V I/O Signaling
5	BT_UART_RTS_N	O	VDDIO	Request-to-send signal for the Bluetooth UART interface, active low.
6	BT_UART_RXD	I	VDDIO	Bluetooth UART Serial Input.
7	BT_HOST_WAKE_B	O		Host Wake-up Signal from the MSD40NBT to the host indicating that the radio requires attention. Asserted – Host device must wake-up or remain awake. Deasserted – Host device may sleep when sleep criteria are met The signal polarity is software configurable and can be asserted high or low. **Note:** The default is low but this is only applicable for specific Bluetooth Sleep mode settings. By default, the radio has “No Sleep Mode Set”.
8	RSVD	O	VDDIO	Reserved for Wake on Wireless Wake on Wireless is not currently supported in the radio firmware. Do not connect when not used
9	RSVD	O	VDDIO	Reserved. Bluetooth LED Activity Indicator, active high.
10	BT_PCM_OUT	O	VDDIO	PCM data output
11	BT_UART_CTS_N	I	VDDIO	Clear-to-send signal for the Bluetooth UART interface, active low.
12	BT_WAKE_B	I	VDDIO	BT Device Wake-up: Signal from the host to the radio indicating that the host requires attention. Asserted – Bluetooth device must wake-up or remain awake Deasserted – Bluetooth device may sleep when sleep criteria are met The signal polarity is software configurable and can be asserted high or low. **Note:** The default is low but this is only applicable for specific Bluetooth Sleep mode settings. By default, the radio has “No Sleep Mode Set”.
13	VCC3_3	-		3.3V Module Power

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Pin Number	Pin Name	I/O	Voltage Reference	Description
14	No Connect			Not Used. Leave Open (Float)
15	No Connect			Not Used. Leave Open (Float)
16	No Connect			Not Used. Leave Open (Float)
17	No Connect			Not Used. Leave Open (Float)
18	No Connect			Not Used. Leave Open (Float)
19	No Connect			Not Used. Leave Open (Float)
20	BT_PCM_SYNC	I/O	VDDIO	PCM sync signal Default master (output); can be configured slave (input)
21	No Connect			Not Used. Leave Open (Float)
22	BT_PCM_IN	I	VDDIO	PCM data input
23	No Connect			Not Used. Leave Open (Float)
24	BT_PCM_CLK	I/O	VDDIO	PCM clock Default master (output): can be configured slave (input)
25	No Connect			Not Used. Leave Open (Float)
26	SYS_RST_L	I	VDDIO	Resets the Wi-Fi radio, active low. Must be asserted when power is first applied to the radio; then released before any transaction can start (see Note 1). See “Electrical Considerations” for the recommended SYS_RST_L circuitry) See Note 2.
27	SDIO_DATA_2	I/O	VDDIO	SDIO Data 2 **Note:** See “Integration Considerations” for additional integration information.
28	RSVD	O	VDDIO	Reserved. No Connect.
29	VCC3_3	-		3.3V Module Power
30	GND	-		Ground
31	GND	-		Ground
32	BT_RST_L	I	VDDIO	Resets the BT radio, active low. Must be asserted when power is first applied to the radio; then released before any transaction can start. See Note 2.
33	No Connect			Not Used. Leave Open (Float)
34	No Connect			Not Used. Leave Open (Float)
35	No Connect			Not Used. Leave Open (Float)
36	RSVD	I/O	VDDIO	Reserved. No Connect.
37	No Connect			Not Used. Leave Open (Float)
38	No Connect			Not Used. Leave Open (Float)
39	No Connect			Not Used. Leave Open (Float)
40	No Connect			Not Used. Leave Open (Float)
41	No Connect			Not Used. Leave Open (Float)
42	RSVD	O	VDDIO	Reserved. No Connect.
43	No Connect			Not Used. Leave Open (Float)
44	No Connect			Not Used. Leave Open (Float)

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Pin Number	Pin Name	I/O	Voltage Reference	Description	
45	No Connect			Not Used. Leave Open (Float)	
46	No Connect			Not Used. Leave Open (Float)	
47	No Connect			Not Used. Leave Open (Float)	
48	CHIP_PWD_L	I	VDDIO	Powers down both the BT and WLAN radios, active low (see Note 1). See Note 2.	
49	No Connect			Not Used. Leave Open (Float)	
50	RSVD	I/O	VDDIO	Reserved for GPIO	
51	No Connect			Not Used. Leave Open (Float)	
52	RSVD	I/O	VDDIO	Reserved for GPIO	
53	RSVD	I/O	VDDIO	Reserved for GPIO	
54	RSVD	I/O	VDDIO	Reserved for GPIO	
55	SDIO_CMD	I/O	VDDIO	SDIO Command	**Note:** See "Integration Considerations" for additional integration information.
56	SDIO_CLK	I	VDDIO	SDIO Clock (25MHz max)	
57	SDIO_DATA_0	I/O	VDDIO	SDIO Data 0	
58	SDIO_DATA_3	I/O	VDDIO	SDIO Data 3	
59	SDIO_DATA_1	I/O	VDDIO	SDIO Data 1	
60	GND	-		Ground	

Note 1: Regarding SYS_RST_L and CHIP_PWD_L:

Simply releasing SYS_RST_L and CHIP_PWD_L does not guarantee that the BCM4329 chip in the SSD40NBT module comes out of reset. Ensure that both VDD and VDDIO have been applied to the SSD40NBT for at least 110 ms before attempting to initiate SDIO communications. A slightly longer delay is better (safer).

Note 2: If the following lines are available on the radio you are integrating into your system, you must connect and control them with the host device.

CHIP_PWD_L
SYS_RST_L
BT_RST_L
VDDIO_DR

If the radio stays powered up and the host goes down or is reset, communications cannot be re-established with the radio. The host SDIO controller must re-establish communication with the radio by reloading the radio firmware after a power-on or a reset.

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6.1.1 Control Signal Timing Diagrams

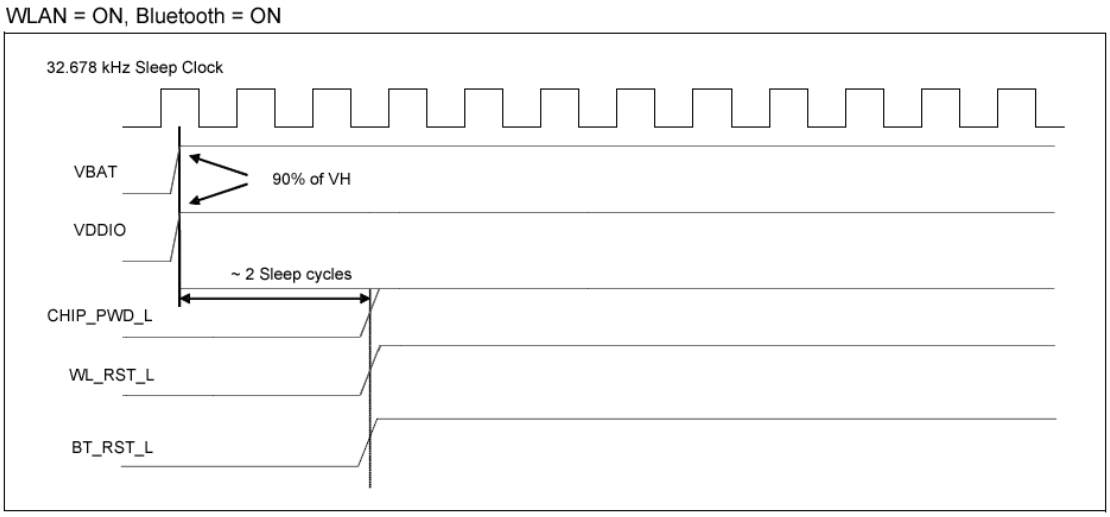

Figure 7: WLAN = ON, Bluetooth = ON

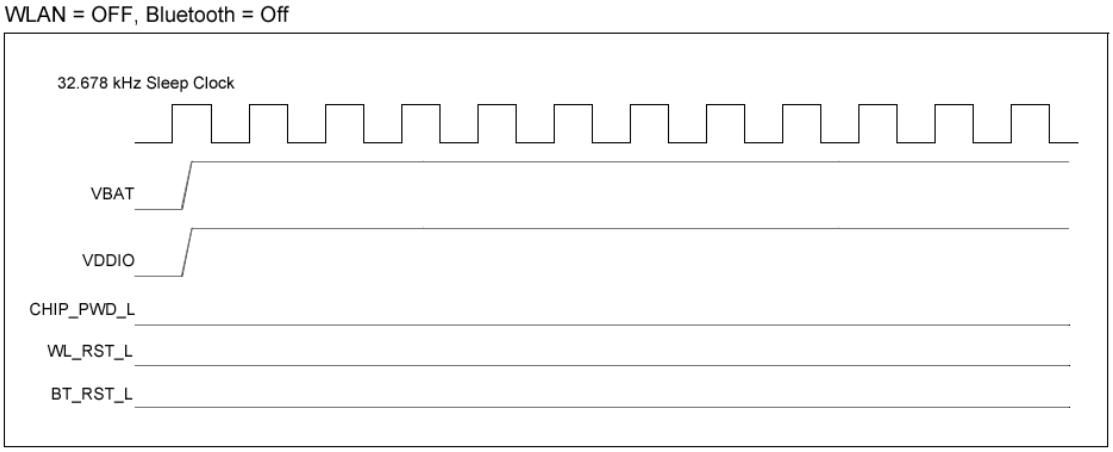

Figure 8: WLAN = OFF, Bluetooth = OFF

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6.2 MSD30AG and MSD40NBT Pin Comparison Table

Note: Click here for a pin comparison table for the MSD10AG, MSD30AG, and MSD40NBT devices.

Pin #	MSD30AG	MSD40NBT	Pin #	SSD30AG	SSD40NBT
	Pin Name	Pin Name		Pin Name	Pin Name
1	GND	GND	31	GND	GND
2	RSVD	BT_UART_TXD	32	RSVD	BT_RST_L
3	BT_PRIORITY	BT_PRIORITY	33	No Connect	No Connect
4	BT_FREQ	BT_GPIO_6	34	No Connect	No Connect
5	RSVD	BT_UART_RTS_N	35	No Connect	No Connect
6	RSVD	BT_UART_RXD	36	BT_ACTIVE	BT_ACTIVE
7	RSVD	BT_HOST_WAKE_B	37	No Connect	No Connect
8	WL_GPIO_1	RSVD	38	No Connect	No Connect
9	RSVD	RSVD	39	No Connect	No Connect
10	RSVD	BT_PCM_OUT	40	No Connect	No Connect
11	RSVD	BT_UART_CTS_N	41	No Connect	No Connect
12	RSVD	RSVD	42	WL_LED_ACT	WL_LED_ACT
13	VCC3_3	VCC3_3	43	No Connect	No Connect
14	No Connect	No Connect	44	No Connect	No Connect
15	No Connect	No Connect	45	No Connect	No Connect
16	No Connect	No Connect	46	No Connect	No Connect
17	No Connect	No Connect	47	No Connect	No Connect
18	No Connect	No Connect	48	CHIP_PWD_L	CHIP_PWD_L
19	No Connect	No Connect	49	No Connect	No Connect
20	RSVD	BT_PCM_SYNC	50	RSVD	RSVD
21	No Connect	No Connect	51	No Connect	No Connect
22	RSVD	BT_PCM_IN	52	RSVD	RSVD
23	No Connect	No Connect	53	RSVD	BT_GPIO_7
24	RSVD	BT_PCM_CLK	54	RSVD	RSVD
25	No Connect	No Connect	55	SDIO_CMD	SDIO_CMD
26	SYS_RST_L	SYS_RST_L	56	SDIO_CLK	SDIO_CLK
27	SDIO_DATA_2	SDIO_DATA_2	57	SDIO_DATA_0	SDIO_DATA_0
28	WLAN_ACTIVE	RSVD	58	SDIO_DATA_3	SDIO_DATA_3
29	VCC3_3	VCC3_3	59	SDIO_DATA_1	SDIO_DATA_1
30	GND	GND	60	GND	GND

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6.3 Integration Considerations

The following Wi-Fi information should be taken into consideration when integrating the SSD40NBT.

Series resistors are recommended in all six SDIO lines (27-56 ohms typically):

- SDIO_CLK
- SDIO_CMD
- SDIO_DATA_0
- SDIO_DATA_1
- SDIO_DATA_2
- SDIO_DATA_3

Note: Although these values may vary with the properties of your host interface and the PCB, they are a reasonable starting point.

Note: The series resistors in the SDIO bus provide several design benefits:

- If a host controller has too high of a drive strength, then bus ringing may result. Series resistors can reduce this ringing on the I/O lines.

- Adding 27-56 ohms of series resistance on the SDIO bus will reduce sharp transitional edges, which may reduce EMI.

- Having the series resistors in the PCB layout allows for design flexibility; If they are later found to be unnecessary, zero (0) ohm jumpers may be used in their place

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7 MECHANICAL SPECIFICATIONS

7.1 Connector Overview

MSD40NBT connector: Molex 54722-0607 60-pin connector

Mating connector (on board): Molex 55560-0607 60-pin connector

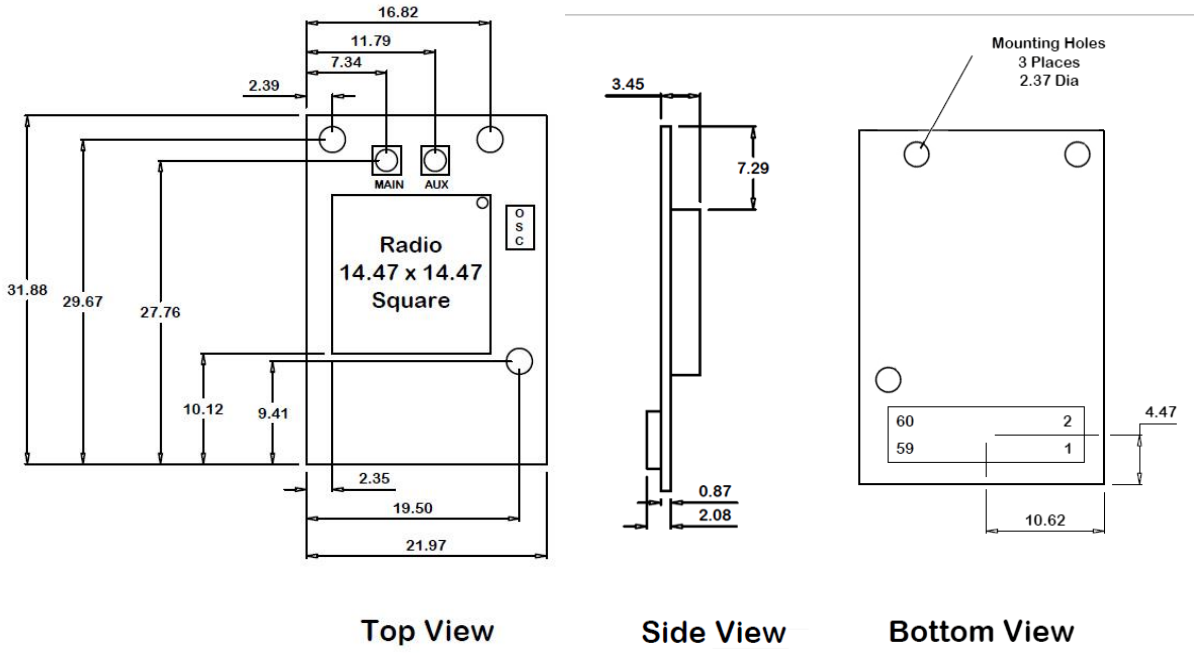

Figure 9: Mechanical Drawing

7.1.1 MSD40NBT Attached to T-Board

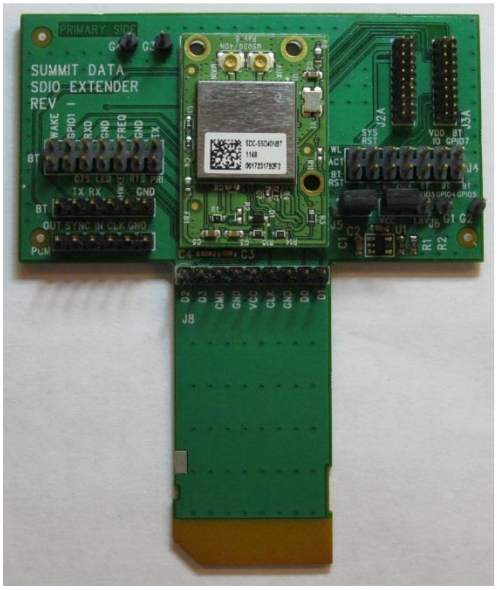

Figure 10: MSD40NBT attached to T-board

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7.2 Mounting

The SDC-MSD40NBT connects to the host via a 60-pin connector. In addition, there are three mounting holes used to secure the device to the host using 2 mm mounting screws.

Summit recommends a 1.5 mm metal spacer (bushing) with a conductive mounting screw to connect the exposed ground pads of the radio circuit board to the host ground plane. A 1.5 mm conductive metal spacer with a maximum OD of 4 mm maximizes grounding of the radio and helps to reduce emissions from the radio circuit board. The spacer may also prevent the MSD board from slanting and breaking the connection to the host device when the board is attached to the host.

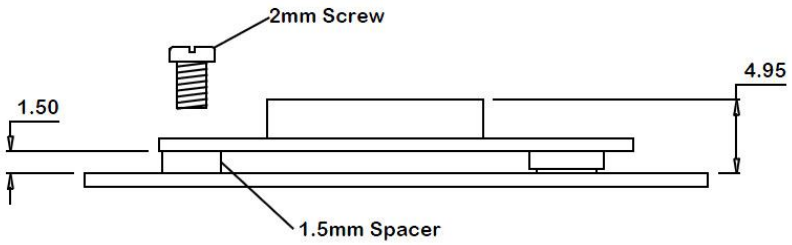

Figure 11: Mounting Recommendations

8 RF Layout Design Guidelines

The following is a list of RF layout design guidelines and recommendation when installing a Summit radio into your device.

- Do not run antenna cables directly above or directly below the radio.
- Do not place any parts or run any high speed digital lines below the radio.
- If there are other radios or transmitters located on the device (such as a Bluetooth radio), place the devices as far apart from each other as possible.
- Ensure that there is the maximum allowable spacing separating the antenna connectors on the Summit radio from the antenna. In addition, do not place antennas directly above or directly below the radio.
- Summit recommends the use of a double shielded cable for the connection between the radio and the antenna elements.
- Summit has provided three plated mounting holes that can be used for grounding. When additional ground plane is required, you may use some or all of these grounded mounting holes.
- Use proper electro-static-discharge (ESD) procedures when installing the Summit radio module.

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9 Regulatory

Note: For complete regulatory information, refer to the MSD40NBT Regulatory Information document which is also available from the MSD40NBT product page.

The MSD40NBT holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	TWG-SDCMSD40NBT
EU	N/A
Canada (ISED)	6616A-SDCMSD40NBT
Taiwan (NCC)	CCAB12LP1340T9
Australia	N/A
New Zealand	N/A

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10 Bluetooth SIG Approvals

10.1 Subsystem Combinations

This application note covers the procedure for generating a new Declaration ID for a Subsystem combination on the Bluetooth SIG website. In the instance of subsystems, a member can combine two or more subsystems to create a complete Bluetooth End Product solution.

The following is a sample subsystem listings to use as a reference:

Design Name	Owner	Declaration ID	Link to listing on the SIG website
MSD40NBT	Laird	B019705	https://www.bluetooth.org/tpg/QLI_viewQDL.cfm?qid=19705
Windows 8 (Host Subsystem)	Microsoft Corporation	B012854	https://www.bluetooth.org/tpg/QLI_viewQDL.cfm?qid=12854

10.2 Assumptions

This procedure assumes that the member is simply combining two subsystems to create a new design, without any modification to the existing, qualified subsystems. This is achieved by using the listing interface on the Bluetooth SIG website. Figure 12 shows the basic subsystem combination of a controller and host subsystem. The controller provides the RF/BB/LM and HCI layers, with the host providing L2CAP, SDP, GAP, RFCOMM/SPP and any other specific protocols and profiles existing in the host subsystem listing. The design may also include a profile subsystem.

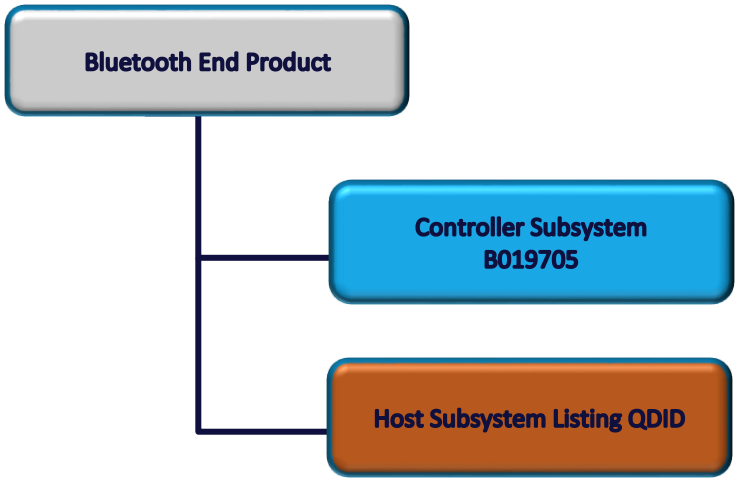

Figure 12: Basic subsystem combination of a controller and host subsystem

The Qualification Process requires each company to registered as a member of the Bluetooth SIG – www.bluetooth.org

The following link provides a link to the Bluetooth Registration page:
https://www.bluetooth.org/login/register/

For each Bluetooth design it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:
https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document:
https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

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To start the listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

In step 1, select **Reference a Qualified Design** and enter the Declaration IDs of each subsystem used in the End Product design. You can then select your pre-paid Declaration ID from the drop down menu or go to the Purchase Declaration ID page, (please note that unless the Declaration ID is pre-paid or purchased with a credit card, it will not be possible to proceed until the SIG invoice is paid.

Once all the relevant sections of step 1 are complete, complete steps 2, 3, and 4 as described in the help document. Your new Design will be listed on the SIG website and you can print your Certificate and DoC.

For further information please refer to the following training material:
https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

11 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

Laird Connectivity
Support Centre: https://www.lairdconnect.com/resources/support
Email: wireless.support@lairdconnectivity.com
Phone: Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610
Web: https://www.lairdconnect.com/products

Note: Information contained in this document is subject to change.

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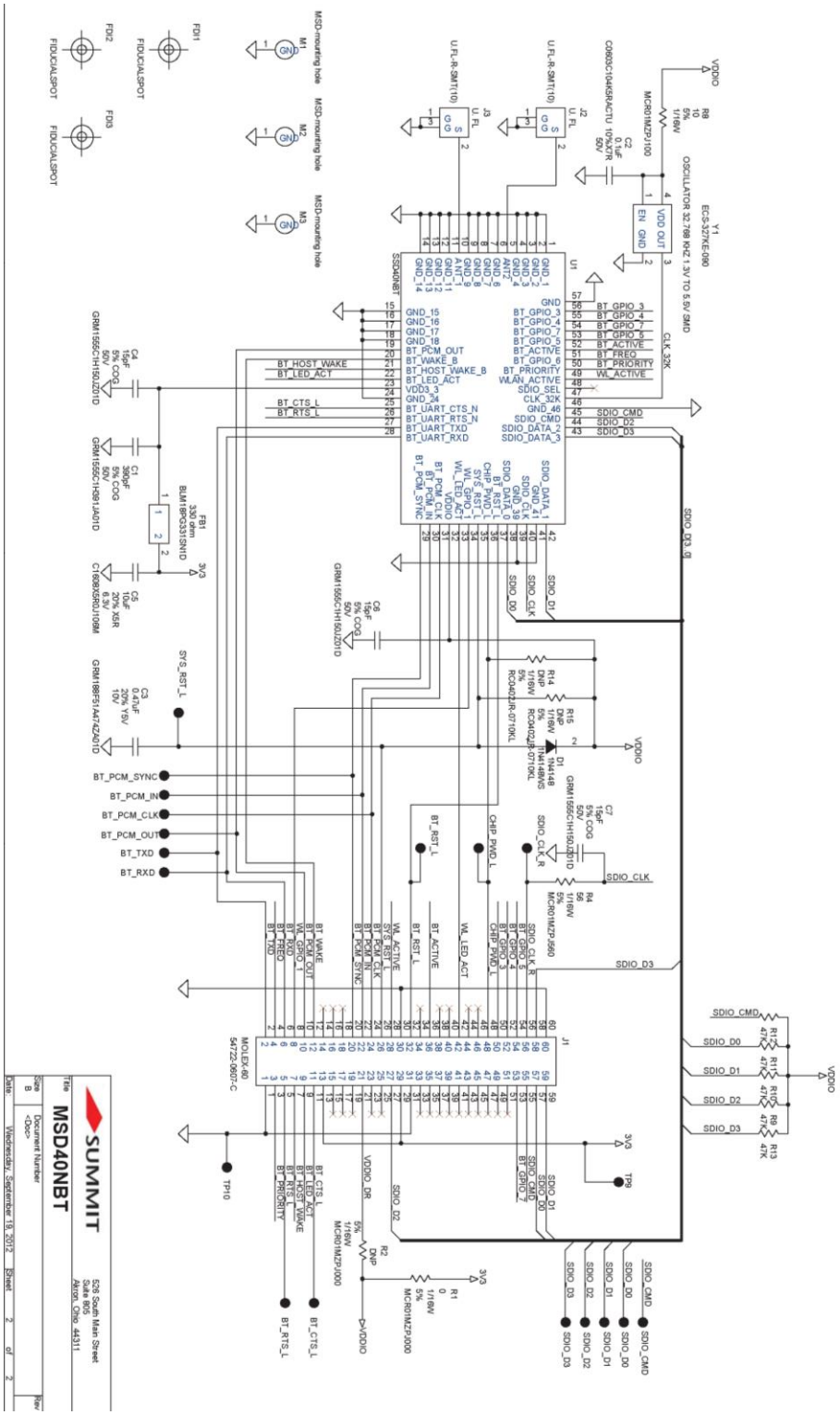
12 Appendix A: Schematic

The following SDC-MSD40NBT schematic may be used as a reference.



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