Laird™

CONNECTIVITY

Datasheet

SSD45N

Version 3.0

REVISION HISTORY

Version	Date	Notes	Contributor(s)	Approver
1.0	23 July 2014	Initial Release		Andrew Chen
1.1	5 August 2014	Added note to SDIO Timing Requirements regarding SDIO bus clock rate.		Andrew Chen
1.2	26 Mar 2015	Fixed Operational Temperature numbers.		Andrew Chen
1.3	15 Oct 2015	Updated Antenna Data Sheet links		Sue White
1.4	1 April 2016	Added note to CPU_WARM_RESET		N. Zach Hogya
1.5	15 Aug 2016	Converted from *Hardware Integration Guide* to *Datasheet*.		Sue White
1.6	07 Sept 2016	Added EU Declaration of Conformity		Sue White
1.7	21 Feb 2017	Updated FCC data to 24 non-overlapping channels		Jay White
1.8	10 Mar 2017	Updated 5 GHz frequency bands and operating channels information		Kris Sidle
1.9	19 Apr 2017	Fixed FCC frequency ranges		Miles Chung
1.10	1 May 2017	OS Support		Jay White
1.11	24 May 2017	Updated EU DoC with RED standards		Maggie Teng
1.12	15 June 2017	Updated EU DoC – new style		Tom Smith
2.0	15 June 2018	New template. Updated Industry Canada section with new certifications		Maggie Smith
2.1	10 Jan 2019	Added NCC and MIC regulatory information Updated logos and URLs		Maggie Teng
2.2	23 Oct 2019	Updated warranty information	Sue White	Jay White
2.3	16 Nov 2020	Updates regulatory information	Ryan Urness	Jay White
3.0	21 Feb 2021	Transferred all detailed regulatory information to a separate document	Sue White	Jonathan Kaye

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1 Scope

This document describes key hardware aspects of the Laird SSD45N radio module. This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from a number of sources and includes information found in the Qualcomm Atheros (QCA) AR6003 data sheet issued in January 2010, along with other documents provided from Qualcomm Atheros.

The information in this document is subject to change. Please contact Laird or visit the documentation tab of the SSD45N product page to obtain the most recent version of this document.

2 Operational Description

This device is a Laird SSD45N radio module which supports IEEE 802.11a/b/g/n standards via an SDIO (Secure Digital Input/Output) interface. The radio operates in unlicensed portions of the 2.4 GHz and 5 GHz radio frequency spectrum. The device is compliant with IEEE 802.11a, 802.11b, 802.11g, and 802.11n standards using Direct Sequence Spread Spectrum (DSSS) and Orthogonal Frequency Division Multiplexing (OFDM). The device supports all 802.11a, 802.11b, 802.11g, and 802.11n data rates and automatically adjusts data rates and operational modes based on various environmental factors.

When operating on channels in the UNII-2 and UNII-2 Extended bands that are in the 5GHz portion of the frequency spectrum and are subject to Dynamic Frequency Selection requirements, the SSD45N fully conforms to applicable regulatory requirements. In the event that specified types of radar are detected by the network infrastructure, the SSD45N fully conforms to commands from the infrastructure for radar avoidance.

The SSD45N is a System in Package (SiP) Quad Flat pack, No leads (QFN) module. The device is based on the Qualcomm Atheros AR6003 chip which is an integrated device providing a Media Access Controller (MAC), a Physical Layer Controller (baseband or BB processor), and fully integrated dual-band radio transceiver. To maximize operational range, the SSD45N incorporates external 2.4 and 5 GHz power amplifiers (PA) to increase transmit power. The frequency stability for both 2.4 GHz (802.11b and 802.11g) and 5 GHz (802.11a) operation is +/- 20 ppm.

The SSD45N has its own RF shielding and does not require shielding provided by the host device into which it is installed in order to maintain compliance with applicable regulatory standards. As such, the device may be tested in a standalone configuration via an extender card.

The device buffers all data inputs so that it will comply with all applicable regulations even in the presence of over-modulated input from the host device. Similarly, the SSD45N incorporates power regulation to comply with all applicable regulations even when receiving excess power from the host device.

The SSD45N combines the 2.4 and 5 GHz signal path to signal U.FL type antenna connectors to support dual band transmission and receive. An antenna diversity function is **NOT** supported in this product. Supported host device antenna types include dipole and monopole antennas.

Regulatory operational requirements are included with this document and may be incorporated into the operating manual of any device into which the SSD45N is installed. The SSD45N is designed for installation into mobile devices such as vehicle mount data terminals (which typically operate at distances greater than 20 cm from the human body) and portable devices such as handheld data terminals (which typically operate at distances less than 20 cm from the human body). See Documentation Requirements for more information.

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3 Block Diagram

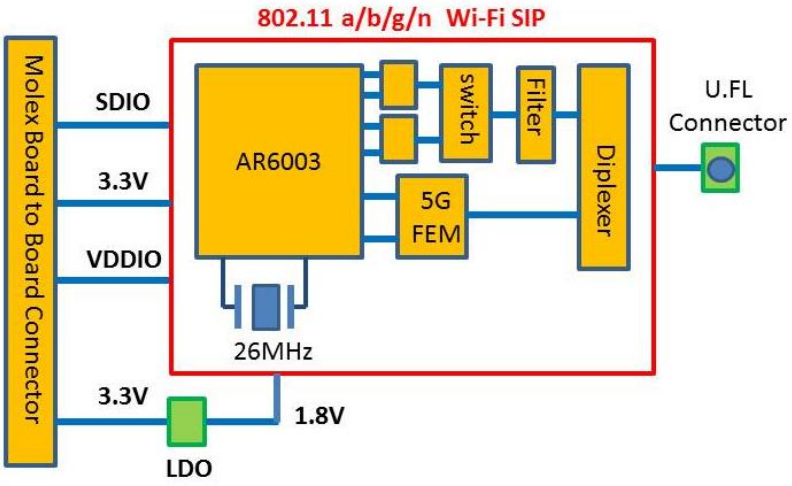

Figure 1: SSD45 Block Diagram

Note: Transmitter frequencies for Wi-Fi are 2412-2462 MHz and 5180-5805 MHz.

4 Specifications

Table 1: Specifications

Feature	Description					
Physical Interface	QFN package					
Wi-Fi Interface	1-bit or 4-bit Secure Digital I/O **Note:** Can support 1.8 V or 3.3 V depending on the supply voltage on DVDD_SDIO.					
Antenna Interface	50 ohm RF impedance					
Main Chip	Qualcomm Atheros AR6003 single-chip client					
Input Voltage Requirements	3.3 VDC ± 5% (core)					
I/O Signalling Voltage	3.3 VDC ± 5% 1.8 VDC ± 5%					
Average Current Consumption (At maximum transmit power setting) **Note:** *Standby* refers to the radio operating in PM1 powersave mode.		**Mode**	**1.8 V**		**3.3 V**	
			Avg. Current	**Max. Current**	**Avg. Current**	**Max. Current (mA)**
	802.11a	Transmit	0.11	0.11	496	500
		Receive	0.11	-	0.2	-
		Standby	TBD	TBD	TBD	TBD
	802.11b	Transmit	0.11	0.11	380	420
		Receive	0.11	-	0.2	-
		Standby	TBD	TBD	TBD	TBD
	802.11g	Transmit	0.11	0.11	355	410

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Feature	Description					
		Receive	0.11	-	0.2	-
		Standby	TBD	TBD	TBD	TBD
	802.11n (2.4 GHz)	Transmit	0.11	0.11	342	420
		Receive	0.11	-	0.2	-
		Standby	TBD	TBD	TBD	TBD
	802.11n (5 GHz)	Transmit	0.11	0.11	422	500
		Receive	0.11	-	0.2	-
		Standby	TBD	TBD	TBD	TBD
	Sleep	N/A	TBD	TBD	TBD	TBD
Operating Temperature	-20° to +70°C (-4° to +158°F)					
Operating Humidity	10 to 95% (non-condensing)					
Storage Temperature	-40° to 85°C (-40° to +185°F)					
Storage Humidity	10 to 95% (non-condensing)					
Maximum Electrostatic Discharge	Maximum Contact Discharge (CD): 4 kV Maximum Air Discharge (AD): 8 kV					
Length/Width/Thickness	11.0 mm x 11.0 mm x 1.3 mm (with shield) with a tolerance of 0.1 mm at each axis.					
Weight						
Wi-Fi Media	Direct Sequence-Spread Spectrum (DSSS) Complementary Code Keying (CCK) Orthogonal Frequency Divisional Multiplexing (OFDM)					
Wi-Fi Media Access Protocol	Carrier sense multiple access with collision avoidance (CSMA/CA)					
Network Architecture Types	Infrastructure and ad hoc					
Wi-Fi Standards	IEEE 802.11a, 802.11b, 802.11d, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n					
Wi-Fi Data Rates Supported	802.11a (OFDM): 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11b (DSSS, CCK): 1, 2, 5.5, 11 Mbps 802.11g (OFDM): 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n (OFDM,HT20,MCS 0-7): 6.5,13,19.5, 26, 39,52, 58.5, 72.2 Mbps 7.2,14.4, 21.7, 28.9,43.3, 57.8, 65 Mbps					
Wi-Fi Modulation	BPSK @ 1, 6, 6.5, 7.2 and 9 Mbps QPSK @ 2, 5.5, 11, 12, 13, 14.4,18, 19.5 and 21.7 Mbps 16-QAM @ 24, 26, 28.9, 36, 39 and 43.3 Mbps 64-QAM @ 48, 52, 54, 57.8, 58.5, 65, and 72.2 Mbps					
802.11n Spatial Streams	1x1 SISO (Single Input, Single Output)					
Regulatory Domain Support	FCC EU MIC (Japan) KC (Korea)					
2.4 GHz Frequency Bands	EU: 2.4 GHz to 2.483 GHz FCC: 2.4 GHz to 2.483 GHz MIC (Japan): 2.4 GHz to 2.495 GHz KC: 2.4 GHz to 2.483 GHz					

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Feature	Description
2.4 GHz Operating Channels	EU:13 (3 non-overlapping) MIC (Japan):14 (4 non-overlapping) FCC:11 (3 non-overlapping) KCC:13 (3 non-overlapping)
5 GHz Frequency Bands	**EU** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/132/136/140) **FCC** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/ 132/136/140) 5.725 GHz to 5.85 GHz (Ch 149/153/157/161/165) **MIC (Japan)** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/ 132/136/140) **KC** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124) 5.725 GHz to 5.825 GHz (Ch 149/153/157/161)
5 GHz Operating Channels	EU:19 non-overlapping) MIC: 19 non-overlapping FCC: 24 non-overlapping KC: 19 non-overlapping
Transmit Power **Note:** Transmit power varies according to individual country regulations. All values nominal, +/-2 dBm. **Note:** Laird 45 series radios support a single spatial stream and 20 MHz-wide channels only.	**802.11a:** 6 Mbps 15 dBm (32 mW) 54 Mbps 15 dBm (32 mW) **802.11b:** 1 Mbps 16 dBm (40 mW) 11 Mbps 16 dBm (40 mW) **802.11g:** 6 Mbps 16 dBm (40 mW) 54 Mbps 14 dBm (25 mW) **802.11n** (2.4 GHz): 6.5 Mbps (MCS0) 16 dBm (40 mW) 65 Mbps (MCS7) 12 dBm (16 mW) **802.11n** (5 GHz): 6.5 Mbps (MCS0) 15 dBm (32 mW) 65 Mbps (MCS7) 12 dBm (16 mW)
Typical Receiver Sensitivity **Note:** All values nominal, +/-3 dBm.	**802.11a:** 6 Mbps -91 dBm 54 Mbps -73 dBm (PER <=10%) **802.11b:** 1 Mbps -92 dBm 11 Mbps -84 dBm (PER <=10%) **802.11g:** 6 Mbps -91 dBm 54 Mbps -74 dBm (PER <=10%) **802.11n** (2.4 GHz): MCS0 Mbps -89 dBm MCS7 Mbps -71 dBm **802.11n** (5 GHz): MCS0 Mbps -89 dBm MCS7 Mbps -71 dBm
Operating Systems Supported	Android, Linux
Security	**Standards** Wireless Equivalent Privacy (WEP) Wi-Fi Protected Access (WPA) IEEE 802.11i (WPA2) **Note:** Support for Federal Information Processing Standards (FIPS) is pending. **Encryption** Wireless Equivalent Privacy (WEP, RC4 Algorithm) Temporal Key Integrity Protocol (TKIP, RC4 Algorithm) Advanced Encryption Standard (AES, Rijndael Algorithm) **Encryption Key Provisioning** Static (40-bit and 128-bit lengths) Pre-Shared (PSK)

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Feature	Description
	Dynamic **802.1X Extensible Authentication Protocol Types** EAP-FAST PEAP-MSCHAPv2 EAP-TLS PEAP-TLS EAP-TTLS LEAP PEAP-GTC
Compliance	**EU Regulatory Domain** EN 300 328 62311:2008 EN 301 489-1 EN 50665:2017 EN 301 489-17 EN 50385:2017 EN 301 893 EU 2015/863 (RoHS 3) **FCC Regulatory Domain** 47 CFR FCC Part 2.1091 47 CFR FCC Part 15.247 47 CFR FCC Part 15.407 **ISED Canada** RSS-210 RSS-247 **MIC (Japan) Regulatory Domain** *ARIB STD-T66/RCR STD-33 (2.4 GHz)* *Article 2 Item 19, Category WW (2.4GHz Channels 1-13)* *Article 2 Item 19-2, Category GZ (2.4GHz Channel 14)* *ARIB STD-T71 (5 GHz)* *Article 2 Item 19-3 Category XW (5150-5250 W52 and 5250-5350 W53)*
Certifications **Note:** These certifications are pending.	Wi-Fi Alliance 802.11a, 802.11b, 802.11g , 802.11n WPA Enterprise WPA2 Enterprise Cisco Compatible Extensions (Version 4)
Warranty	**One-year warranty**
	All specifications are subject to change without notice

5 Recommended Operating Conditions and DC Electrical Characteristics

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD3_3	Power supply voltage with respect to ground	-0.3	-	4.0	V
VDD1_8	Power supply voltage with respect to ground	-0.3	-	2.5	V
DVDD_SDIO	Power supply voltage with respect to ground	-0.3	-	4.0	V
DVDD_SOC1	Power supply voltage with respect to ground	-0.3	-	4.0	V
DVDD_SOC2	Power supply voltage with respect to ground	-0.3	-	4.0	V
Voltage Ripple	±2%, 10 KHz~100KHz, maximum values not exceeding operating voltage	-	-	2	%
RFin	Maximum RF input (references to 50 ohm)	-	-	+10	dBm

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Table 3: Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD3_3	Power supply voltage with respect to ground	3.14	3.3	3.46	V
VDD1_8	Power supply voltage with respect to ground	1.71	1.8	1.89	V
DVDD_SDIO	Power supply voltage with respect to ground	1.71	-	3.46	V
DVDD_SOC1	Power supply voltage with respect to ground	1.71	-	3.46	V
DVDD_SOC2	Power supply voltage with respect to ground	1.71	-	3.46	V

Note: VDD_IO is a voltage from the host platform to configure the I/O signal level. It can be set 1.8 V or 3.3 V.

6 DC Electrical Characteristics

6.1 General DC Electrical Characteristics (3.3V & 1.8V I/O operation)

Table 4 and Table 5 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 4: General DC electrical characteristics (for 3.3 V I/O operation)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		-	0.7 x V_{DD}	-	TBD	V
V_{IL}	Low Level Input Voltage		-	TBD	-	0.3 x V_{DD}	V
I_{IL}	Input Leakage Current	Without pull-up or pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	0	-	-3	nA
		With pull-up	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	16	-	48	µA
		With pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	-14	-	-47	µA
V_{OH}	High Level Output Voltage		I_{OH} = -4 mA	0.9 x V_{DD}	-	-	V
			I_{OH} = -12 mA	0.9 x V_{DD}	-	-	V
V_{OL}	Low Level Output Voltage		I_{OH} = 4 mA	-	-	0.1 x V_{DD}	V
			I_{OH} = 12 mA	-	-	0.1 x V_{DD}	V

Table 5: General DC electrical characteristics (For 1.8 V I/O operation)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		-	0.7 x V_{DD}	-	TBD	V
V_{IL}	Low Level Input Voltage		-	TBD	-	0.3 x V_{DD}	V
I_{IL}	Input Leakage Current	Without pull-up or pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	0	-	-3	nA
		With pull-up	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	3.5	-	13	µA
		With pull-down	0 V < V_{IN} < V_{DD} 0 V < V_{OUT} < V_{DD}	-6.2	-	-23	µA
V_{OH}	High Level Output Voltage		I_{OH} = -4 mA	0.9 x V_{DD}	-	-	V
			I_{OH} = -12 mA	0.9 x V_{DD}	-	-	V
V_{OL}	Low Level Output Voltage		I_{OH} = 4 mA	-	-	0.1 x V_{DD}	V
			I_{OH} = 12 mA	-	-	0.1 x V_{DD}	V

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6.1.1 SDIO Timing Requirements

The following figure (Figure 2) and table (Table 6) display SDIO default mode timing.

Note: The SDIO bus should not exceed a 25 MHz clock rate.

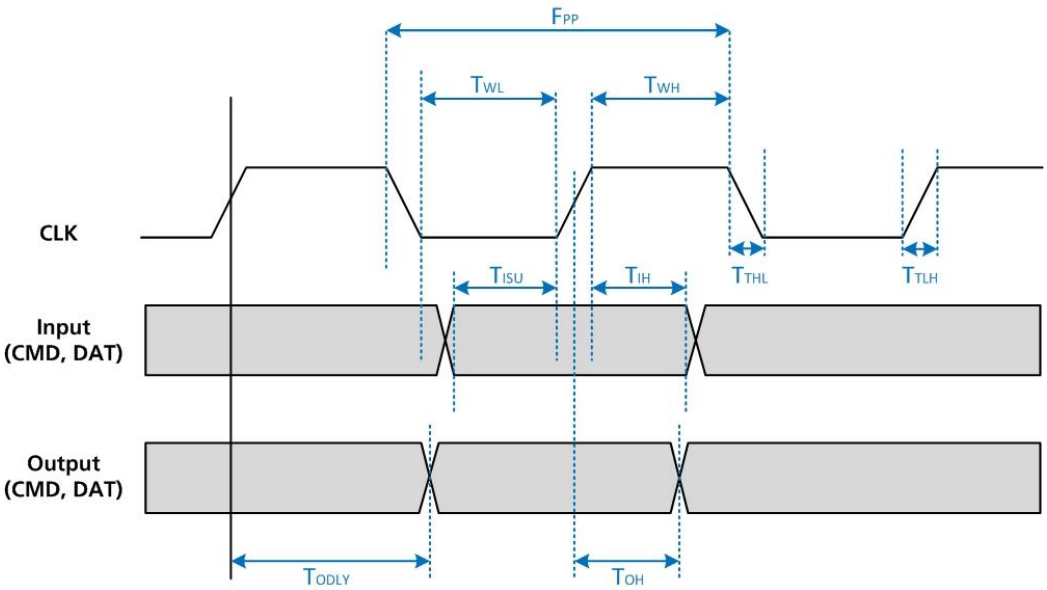

Figure 2: SDIO Default Mode Timing

Note: Timing is based on CL ≤ 40 pF load on CMD and Data.

Table 6: SDIO Timing Requirements

Symbol	Parameter	Min.	Typ.	Max.	Unit
fPP	Frequency – Data Transfer mode	0	-	50	MHz
tWL	Clock low time	7	-	-	ns
tWH	Clock high time	7	-	-	ns
tTLH	Clock rise time	-	-	10	ns
tTHL	Clock low time	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
tISU	Input setup time	6	-	-	ns
tIH	Input hold time	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
tODLY	Output delay time – Data Transfer mode	0	-	14	ns

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7 Pin Definitions

Table 6: Pin Definitions

Pin #	Pin Name	I/O	Default State	Ref.	Description	If Unused
1	GND	-	-	-	Ground	Must be connected to GND
2	RF_IN-OUT	I/O	-	-	RF signal for transmission and receiving	
3	GND	-	-	-	Ground	Must be connected to GND
4	GND	-	-	-	Ground	Must be connected to GND
5	GND	-	-	-	Ground	Must be connected to GND
6	GND	-	-	-	Ground	Must be connected to GND
7	GND	-	-	-	Ground	Must be connected to GND
8	GND	-	-	-	Ground	Must be connected to GND
9	VDD3_3	-	-	-	3.3 V module power	
10	TMS	I	High		JTAG Test Mode Select input	No Connect
11	TDI	I	High		JTAG Test Data In input	No Connect
12	TDO/WLAN_ UART_TXD	O	High		JTAG Test Data Out output	No Connect
13	TCK	I	High		JTAG Test Clock input	No Connect
14	GND	-	-	-	Ground	Must be connected to GND
15	GND	-	-	-	Ground	Must be connected to GND
16	DEBUG_UART_TX D	O	Hi-Z	DVDD _SOC 2	Output for debug message for software test	No Connect
17	NC	-	-	-	-	No Connect
18	NC	-	-	-	-	No Connect
19	NC	-	-	-	-	No Connect
20	VDD3_3	-	-	-	3.3 V module power	
21	GND	-	-	-	Ground	Must be connected to GND
22	SDIO_CLK	I	Hi-Z	VDD_I O	SDIO clock	
23	SDIO_DATA_1	I/O	Pull-H	VDD_I O	SDIO data pin bit 1	

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Pin #	Pin Name	I/O	Default State	Ref.	Description	If Unused
24	SDIO_DATA_0	I/O	Pull-H	VDD_IO	SDIO data pin bit 0	
25	SDIO_CMD	I/O	Pull-H	VDD_IO	SDIO command	
26	SDIO_DATA_2	I/O	Pull-H	VDD_IO	SDIO data pin bit 2	
27	SDIO_DATA_3	I/O	Pull-H	VDD_IO	SDIO data pin bit 3	
28	GND	-	-	-	Ground	Must be connected to GND
29	VCC3_3	-	-	-	3.3 V module power	
30	GND	-	-	-	Ground	Must be connected to GND
31	VDD3_3	-	-	-	3.3 V module power	
32	VDD3_3	-	-	-	3.3 V module power	
33	VDD_IO	-	-	-	I/O bus voltage configuration; Either 3.3 V or 1.8 V	
34	GND	-	-	-	Ground	Must be connected to GND
35	CLK_32K	I			Optional External 32kHz clock input	
36	GND	-	-	-	Ground	Must be connected to GND
37	BT_CLK_OUT	O			Reference clock output to to BT chip	No Connect
38	GND				Ground	Must be connected to GND
39	BT_RX_FRAME	I			Optional software GPIO	
40	BT_ACTIVE	I	Hi-Z	VDD_IO	Asserted for BT TX/RX	No Connect
41	BT_PRIORITY	I	Hi-Z	VDD_IO	Priority of BT transmission and direction (TX or RX)	No Connect
42	BT_FREQ	I			BT FREQUENCY signal from BT chip	No Connect
43	WL_LED_ACTIVE	O	Low		Decision of coexistence logic for BT frame. A logic high indicates BT to stop transmission. A logic low allows BT to continue with TX/RX.	No Connect
44	BT_CLK_REQ	I			Clock request signal from BT chip	Must be connected to GND
45	GND	-	-	-	Ground	Must be connected to GND
46	CLK_REQ_OUT	O	-	-	CLK_REQ signal indicating when a reference clock is needed.	
47	VDD1_8	-	-	-	1.8V power supply	
48	VDD1_8	-	-	-	1.8V power supply	
49	DVDD_SOC1	-	-	-	GPIO	
50	CHIP_PWD_L	I	Pull-H	VDD_IO	Input signal to power down the module. Active low See Note Regarding CHIP_PWD_L.	

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Pin #	Pin Name	I/O	Default State	Ref.	Description	If Unused
51	HMODE0	I			Select the host interface SDIO: HM0=High; HM1=high GSPI: HM0=Low HM1=High	
52	HMODE1	I				
53	CPU_WARM_RESET	O			Optional Wake On Wireless output	
54	GND				Ground	Must be connected to GND
55	ANTE	O			Antenna Control signal for RF front end component	
56	GND	-	-	-	Ground	Must be connected to GND
57	GND	-	-	-	Ground	Must be connected to GND
58	GND	-	-	-	Ground	Must be connected to GND
59	GND	-	-	-	Ground	Must be connected to GND
60	GND	-	-	-	Ground	Must be connected to GND

7.1 Signal Names and Signal Types

Type	Symbol	Description
Signal Name	NC	No connection should be made to this pin
	_L	At the end of the signal name, indicates active low signals
	P	At the end of the signal name, indicates the positive side of a differential signal
	N	At the end of the signal name indicates the negative side of a differential signal
Signal Types	I/OH	A digital bidirectional signal, with a weak internal pull-up
	I/OL	A digital bidirectional signal, with a weak internal pull-down
	OA	An analog output signal
	O	A digital output signal
	P	A power or ground signal

7.2 Reference Clock, Sleep Clock, and Clock Sharing

The Laird SSD45N has a built-in 26 MHz clock and a 32.768 KHz sleep clock; an additional external reference clock is unnecessary. Be sure to ground pin 35 to enable the internal sleep clock.

The SSD45N can provide a buffered reference clock (26 MHz) output at pin 37. This clock can be used to drive other system components such as a Bluetooth device which can significantly reduce BOM cost and size.

Clock sharing implementation is available when the WLAN software is downloaded (Figure 3). To enable this, the following must be done:

Connect BT_CLK_REQ on the Bluetooth circuit to BT_CLK_REQ (pin 44) on the SSD45N.

Connect BT_CLK_OUT (pin 37) on the SSD45N to the Bluetooth circuit clock input.

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CLK_REQ_OUT (pin 46) can be ignored with No Connect (NC). All power supplies must be present when using clock sharing. Clock sharing is available in both sleep and normal operating modes once the software is downloaded.

A filter is required for SSD45N clock output to reduce spurs in the Bluetooth device RF output and to improve the modulation index (Figure 4).

You can use a DC-coupled or AC-coupled clock depending on the requirements of your Bluetooth device. When DC-coupled is used, we recommend the following:

- R3 – 10 ohm
- C1 – 68 pF
- R2 – 0 ohm
- R1 – Remove

When AC-coupled is used, we recommend the following:

- R3 – Change to a capacitor
- C1 – Change to a resistor
- R1 and C1 – Adjust to get required DC bias point
- R2 – Adjust to get a better match between the SSD45N and the Bluetooth device

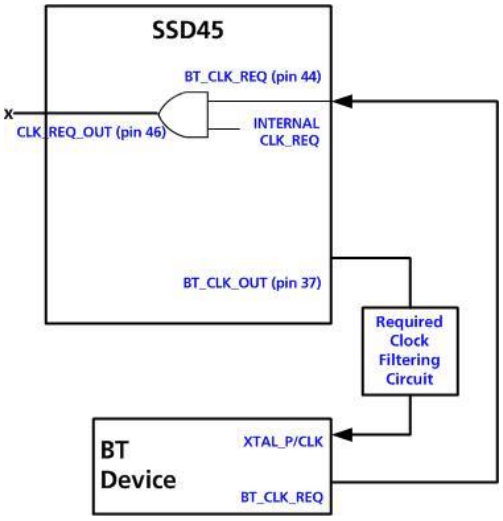

Figure 3: Clock sharing implementation

Note: We recommend that the length between the SSD45N and the BT device is smaller than 1200 mil in the clock trace layout. (Figure 4)

Note: Bluetooth clock sharing filtering circuit involves three resistors and one capacitor. This could be reduced to one resistor and one capacitor with future releases but it depends on the test result. (Figure 4)

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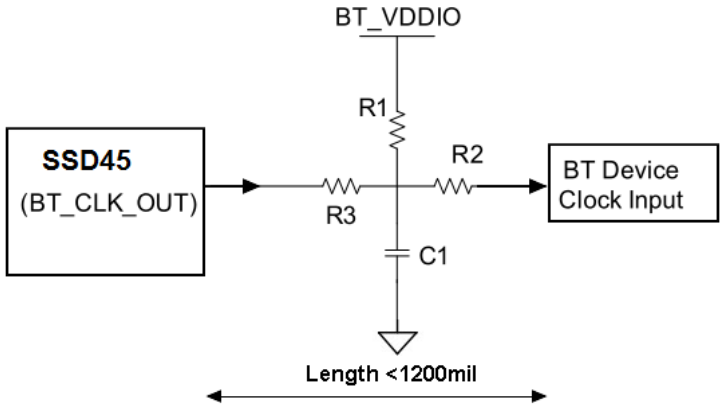

Figure 4: Filtering circuit when using clock sharing

7.3 CPU_WARM_RESET

The CPU_WARM_RESET pin (pin 53) is dedicated to wake-on-wireless (WoW); it is the hardware toggle point for WoW from the host (and requires a hardware toggle input from the host).

Once the system (and client device) are placed into a low-power state, the client device generally remains associated with its current AP to receive and monitor incoming frames. If one of the specified patterns is detected in the frame, the client wakes the system by asserting a hardware pin. Once awake, the client's driver is notified of the change in power state and data connectivity with the AP is re-established.

Because CPU_WARM_RESET defaults low, the WoW interrupt is active high.

Note: The CPU_WARM_RESET signal must NOT be pulled high.

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7.4 Reset and Power On/Off Timing

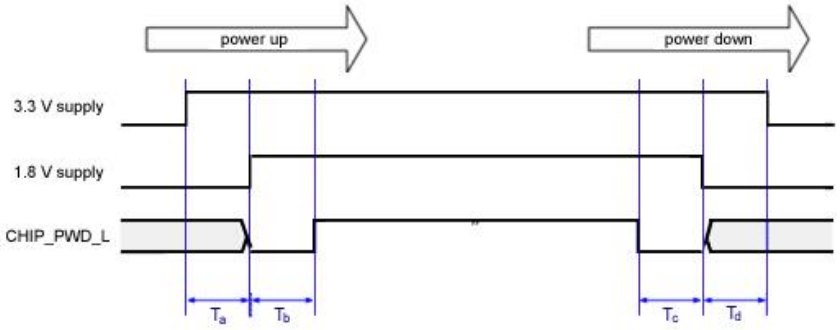

Figure 5: Power on/down timing

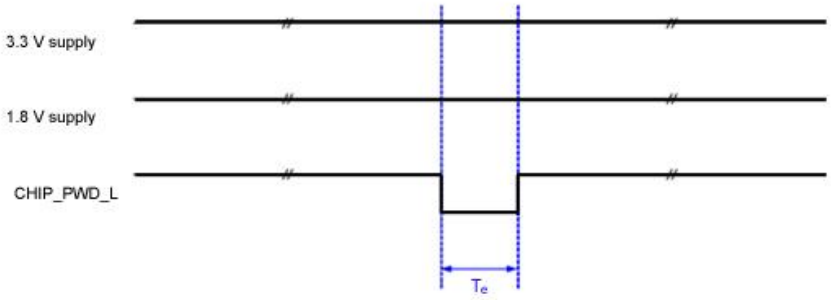

Figure 6: Reset timing

	Description	Minimum (µsec)
T_a	Time between VBAT, VDD33, and I/O supplies valid and 1.8 V supply valid[1]	0
T_b	Time between 1.8 V supply valid and CHIP_PWD_L deassertion	5
T_c	Time between CHIP_PWD_L assertion and 1.8 V supply invalid	0
T_d	Time between 1.8 V supply invalid and VBAT, VDD33, and I/O supplies invalid	N/A[2]
T_e	Length of CHIP_PWDP_L pulse	5

[1] Supply valid represents the voltage level has reached 90% level.

[2] No strict requirements. This parameter can also be negative.

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7.5 SSD40NBT and SSD45N Pin Comparison Table

Pin #	Pin Name SSD40NBT	Pin Name SSD45N	Pin #	Pin Name SSD40NBT	Pin Name SSD45N
1	GND	GND	31	RSVD	VDD3_3
2	GND	RF_IN-OUT	32	VDDIO	VDD3_3
3	GND	GND	33	WL_LED_ACT	DVDD_SDIO
4	GND	GND	34	WL_GPIO_1	GND
5	ANT_2	GND	35	SYS_RST_L	CLK_32K
6	GND	GND	36	CHIP_PWD_L	GND
7	GND	GND	37	RSVD	BT_CLK_OUT
8	GND	GND	38	SDIO_DATA_0	GND
9	GND	VDD3_3	39	GND	BT_RX_FRAME
10	ANT_1	TMS	40	SDIO_CLK	BT_ACTIVE
11	GND	TDI	41	GND	BT_PRIORITY
12	GND	TDO/WLAN_UART_TXD	42	SDIO_DATA_1	BT_FREQ
13	GND	TCK	43	SDIO_DATA_3	WLAN_ACTIVE
14	GND	GND	44	SDIO_DATA_2	BT_CLK_REQ
15	GND	GND	45	SDIO_CMD	GND
16	GND	DEBUG_UART_TXD	46	GND	CLK_REQ_OUT
17	GND	NC	47	RSVD	VDD1_8
18	GND	NC	48	SDIO_SEL	VDD1_8
19	BT_PCM_OUT	NC	49	WLAN_ACTIVE	DVDD_SOC1
20	RSVD	DVDD_SOC2	50	BT_PRIORITY	CHIP_PWD_L
21	BT_HOST_WAKE_B	GND	51	BT_FREQ	HMODE0
22	RSVD	SDIO_CLK	52	BT_ACTIVE	HMODE1
23	VDD3_3	SDIO_DATA_1	53	RSVD	CPU_WARM_RESET
24	GND	SDIO_DATA_0	54	RSVD	GND
25	BT_UART_CTS_N	SDIO_CMD	55	RSVD	ANTE
26	BT_UART_RTS_N	SDIO_DATA_2	56	RSVD	GND
27	BT_UART_TXD	SDIO_DATA_3	57	-	GND
28	BT_UART_RXD	GND	58	-	GND
29	RSVD	VBAT/VDD3_3	59	-	GND
30	RSVD	GND	60	-	GND

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8 MECHANICAL SPECIFICATIONS

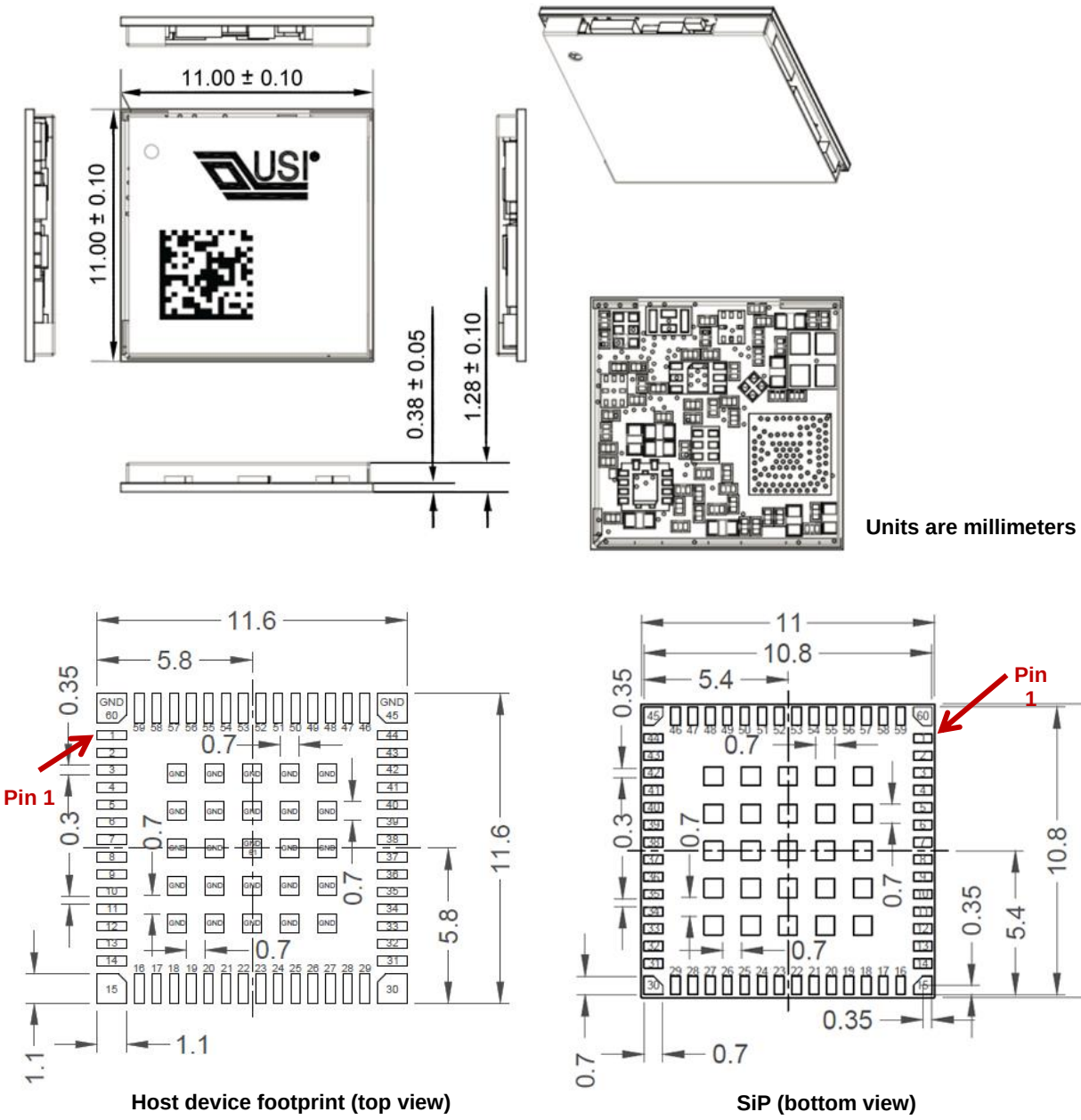

Figure 7: Mechanical Drawings

Note: The following information results from Laird's experience in producing the SDC-SSD45N. Laird provides these data for informational purposes only and provides no warranties or claims with regard to the applicability of this information to a particular design.

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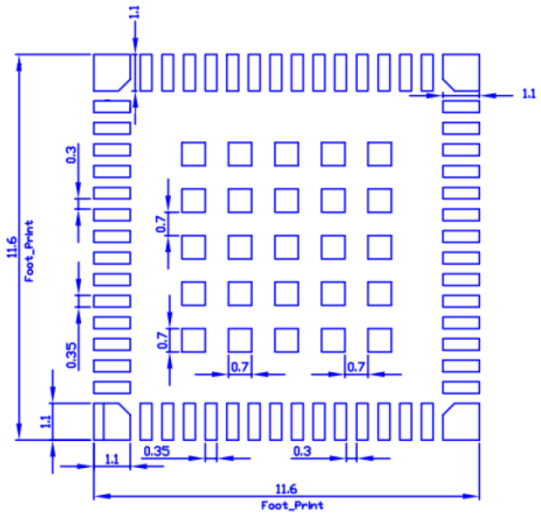

Figure 8: Recommended footprint (top view)

Solder Stencil Opening for Pads (56 signal pads): 1:1 to 1:0.9 (dependent on solder type)

Solder Stencil Opening for Thermal Pads (9 “window pane” pads): 1:0.5 to 1:0.75 (dependent on solder type)

Note: The ground vias that are in the thermal pad (6x6 pattern of 12 mil holes) are open; they are not tented by the solder mask on the bottom side. This allows excess paste to escape from the bottom side to help ensure a flat SIP installation.

Solder Paste Type: No-Clean as the soldered part to board clearance will not allow for adequate post solder cleaning.

Rework is technically challenging due to parts on the SIP reflowing at the same temperature needed for rework. The SDC-SSD45N cannot be lifted by the shield during rework. As such, removal of part for rework is not recommended. Reflow without removal has been successfully used to clear shorts found during x-ray inspection.

Reflow: The SDC-SSD45N is RoHS compliant and as such is sensitive to heat. The below graphic details a typical profile for such and device and is provided for reference purposes.

8.1.1 Recommendations:

If the SSD45N has been removed from the moisture-protective packaging for more than 24 hours, bake at 125 degrees Celsius for 24 hours (per Jedec-STD-033). This is a preparatory step prior to reflow to ensure that the SIPs are sufficiently dehydrated. Reflow should occur immediately following baking to prevent rehydration.

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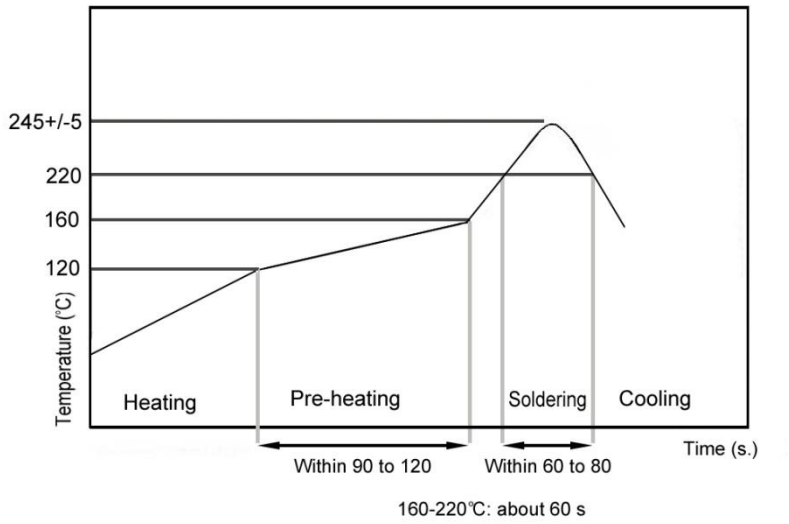

We recommend that the peak temperature at the solder joint be within 240°C ~ 250°C and the maximum component temperature should not exceed 250°C.

We recommend that time above 220°C for the solder joints is between 60-80 seconds, and with a minimum of 50 seconds.

Excessive ramp/cooling rates (>3°C/second) should be avoided.

To develop the reflow profile, we recommend that you place thermocouples at various locations on the assembly to confirm that all locations meet the profile requirements. The critical locations are the solder joints of SiP Module. We also recommend that you use the actual fully loaded assembly to account for the total thermal mass.

9 RF Layout Design Guidelines

The following is a list of RF layout design guidelines and recommendation when installing a Laird radio into your device.

- Do not run antenna cables directly above or directly below the radio.
- Do not place any parts or run any high speed digital lines below the radio.
- If there are other radios or transmitters located on the device (such as a Bluetooth radio), place the devices as far apart from each other as possible.
- Ensure that there is the maximum allowable spacing separating the antenna connectors on the Laird radio from the antenna. In addition, do not place antennas directly above or directly below the radio.
- Laird recommends the use of a double shielded cable for the connection between the radio and the antenna elements.
- Laird has provided three plated mounting holes that can be used for grounding. When additional ground plane is required, you may use some or all of these grounded mounting holes.
- Use proper electro-static-discharge (ESD) procedures when installing the Laird radio module.
- For system schematic relative module, please don't put via on module's pad. To avoid void occupy on solder paste pad.
- Need to place enough ground via under the SSD45NBT.

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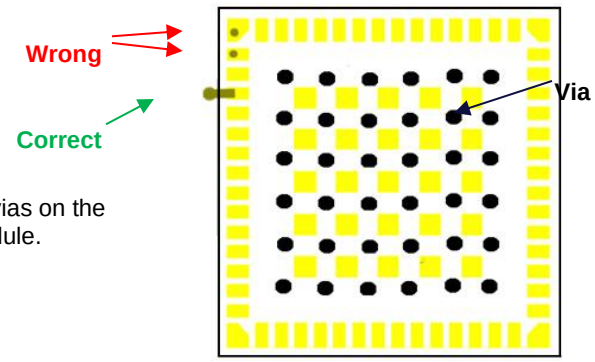


Note: Do not use the vias on the pads of the module.

Figure 9: Module footprint

Important: The landing pad of the U.FL connector will cause induced capacitor when the distance to the reference ground plan is less than 10 mils. This will decrease the RF performance on 5GHz. It is must to remove the ground plan in the inner layer.

Be sure to make the reference ground continuous.

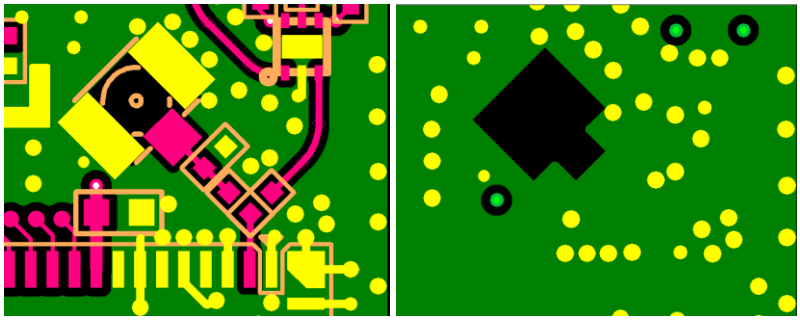
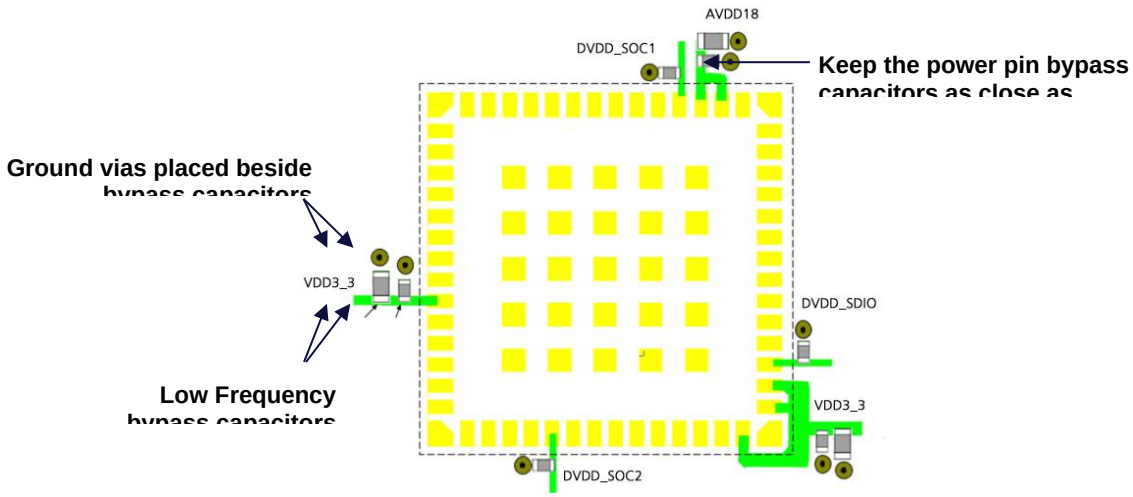


Figure 10: Top layer (left) and inner layer (layer 2) (right)

Location of the decoupling capacitor. As shown on Figure 10, the bypass capacitor should be placed as recommended.



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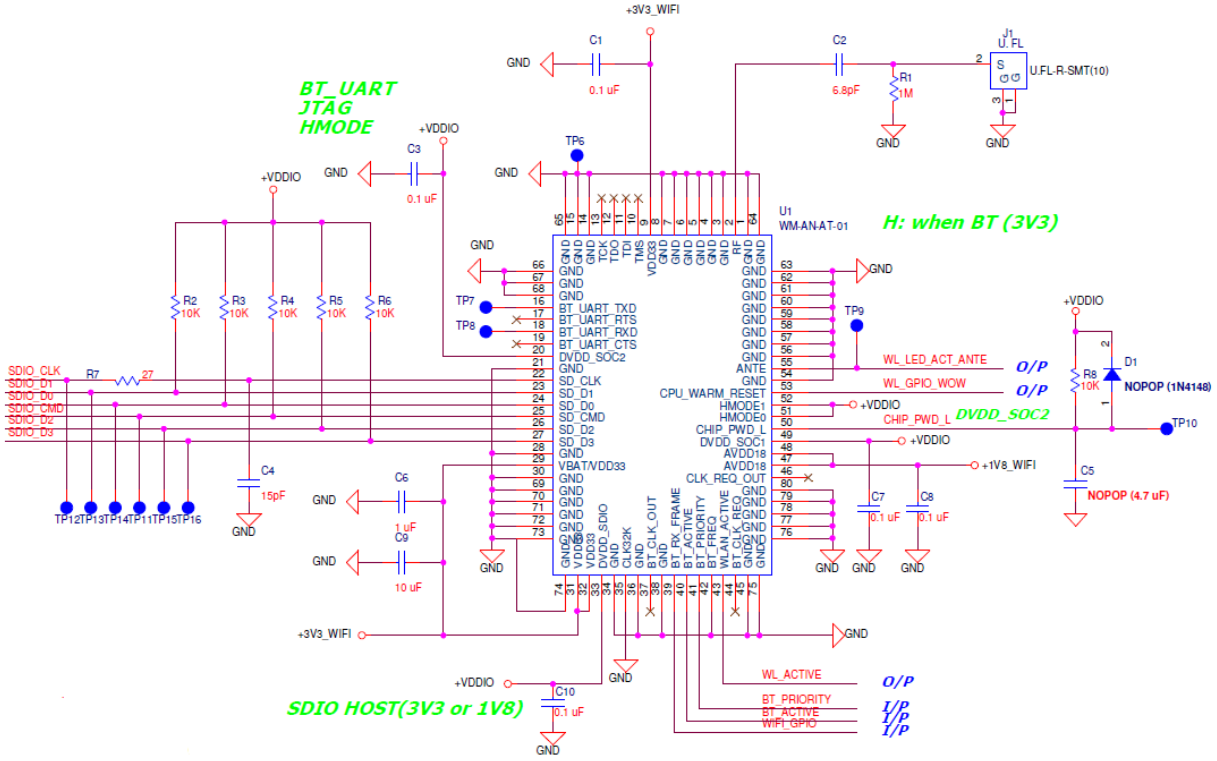
10 Reference Schematic



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11 Regulatory

Note: For complete regulatory information, refer to the SSD45N Regulatory Information document which is also available from the SSD45N product page.

The SSD45N holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-SSD45N
EU	N/A
Canada (ISED)	3147A-SSD45N
Japan (MIC)	201-180906

12 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

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Note: Information contained in this document is subject to change.

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