Datasheet

Pinnacle™ 100 Cellular Modem

Version 2.2

Revision History

Version	Date	Notes	Contributor(s)	Approver
1.0	11 Feb 2020	Initial Release	Mike Richter	Matt Stergiou
1.1	18 March 2020	Updated: Block Diagram, BLE RX Sensitivity, Bluetooth SIG Qualification	Mike Richter	Matt Stergiou
1.2	08 Apr 2020	Fixed typos and missing data	Mike Richter	Matt Stergiou
1.3	12 May 2020	Updated DoC	Ryan Urness	Matt Stergiou
1.4	09 Jun 2020	Updated DoC	Ryan Urness	Matt Stergiou
1.5	31 July 2020	Updated AT&T and PTCRB sections		Jonathan Kaye
1.6	13 Aug 2020	Add note regarding USB protection to the General Parameters Specifications section. Add HL7800 to nRF52840 UART Section.	Mike Richter	Jonathan Kaye
1.7	17 Oct 2020	Fixed table reference error	Rikki Horrigan	Jonathan Kaye
1.8	25 Nov 2020	Updated regulatory information; updated antenna information	Connie Lin	Jonathan Kaye
2.0	15 Feb 2021	Moved detailed regulatory information to separate document	Sue White	Jonathan Kaye
2.1	7 Sept 2021	Added carrier approvals to AT&T and Verizon	Dave Drogowski	Jonathan Kaye
2.2	14 Oct 2021	Fixed table alignment on Table 2: Pin definitions Corrected values in Table 14: UART interface	Dave Drogowski	Andy Ross

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Americas: +1-800-492-2320
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Hong Kong: +852 2923 0610

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1 Overview and Key Features

The Pinnacle™ 100 modem seamlessly incorporates a powerful Cortex M4F controller, full Bluetooth v5 and LTE CAT M1/NB-IoT capabilities – all with full regulatory certifications and LTE carrier approvals.

Develop your application directly on the M4F controller using Zephyr RTOS to cut BOM costs and power consumption. Take advantage of the Zephyr community, Laird Connectivity's sample code (cellular, Bluetooth) and hardware interfaces, OR use our hosted mode AT commands set that augments with commands that provide BLE, NFC and GPIO functionality.

This innovative modem family also offers complete antenna flexibility – on-device, off-board, as well as external antennas – to give you design flexibility, reduce complexity, and simplify your overall product solution.

Extremely power conscious, the Pinnacle™ 100 is ideal for battery-powered devices operating at the edge of your IoT networks, seamlessly bridging the cellular WAN to the BLE network. It's never been easier to bridge wireless Bluetooth 5 sensor data to cloud services like AWS IoT over a low-power LTE connection.

1.1 Features and Benefits

- **LTE-M / NB-IoT** radio via Sierra HL7800
  - **Altair ALT1250** – LTE bands 1, 2, 3, 4, 5, 8*, 12, 13, 20, 28
  - **Nordic nRF52840** – BT v5, Coded PHY (Long range), 1 MPHY & 2 MPHY
- Onboard Cortex-M4F Microcontroller – 32-bit @ 64 MHz, 256 KB of RAM, 1 MB internal flash, 8 MB QSPI**
- **Industrial Temp Range** – Operating range -40° to +85° C
- **Globally and Carrier Certified** – FCC, IC, CE, BT SIG plus PTCRB, GCF and **End Device** certified – AT&T and Verizon
- **Flexible Programming** – Design your way: Hostless mode via Zephyr RTOS or Hosted mode AT Command Set
- **Secure Firmware Upgrade** – Comes pre-programmed with Laird Connectivity's secure bootloader
- **Antenna Options** – Unique integrated antenna variant plus external variant with U.FL connectors
- **Flexible Programming** – Design your way: Hostless mode via Zephyr RTOS or Hosted mode AT Command Set
- **Customisation** – Custom branding, packaging, application development all available.
- **BLE Rx sensitivity**: -93 dBm (1 Mbps), - 101 dBm (125 kbps)

* – Band 8 supported by Laird Connectivity's Dipole Blade DBA6927C1-FSMAM antenna

** – When utilizing Bootloader, full 8 MB not available

1.2 Application Areas

- Cellular IoT
- Connected Medical
- Environmental Monitoring
- Predictive Maintenance
- Retail/Commercial

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2 SPECIFICATION

2.1 Specification Summary

Table 1: Key specifications

Categories/Feature	Implementation
Wireless Specification	
Cellular LTE	▪ Multi-Band cellular operation for world-wide operation ▪ Category M1 and category NB1 support ▪ Power class 3 ▪ Sensitivity: Cat-M1: -99 to -102 dBm (1.4 MHz BW, band-dependent)
Bluetooth®	▪ BT 5.0 – Single mode ▪ 4x Range (CODED PHY support) – BT 5.0 ▪ 2x Speed (2M PHY support) – BT 5.0 ▪ LE Advertising Extensions – BT 5.0 ▪ Concurrent master, slave ▪ BLE Mesh capabilities ▪ Diffie-Hellman based pairing (LE Secure Connections) – BT 4.2 ▪ Data Packet Length Extension – BT 4.2 ▪ Link Layer Privacy (LE Privacy 1.2) – BT 4.2 ▪ LE Dual Mode Topology – BT 4.1 ▪ LE Ping – BT 4.1
Processor	▪ 32-bit ARM® Cortex®-M4F @ 64 MHz ▪ Full-speed 12 Mbps USB controller ▪ +8 dBm BLE TX Power Setting ▪ -93 dBm BLE RX Sensitivity (1 Mbps) ▪ High speed SPI interface 32 MHz ▪ 12 bit/200K SPS ADC ▪ 128-bit AES/ECB/CCM/AAR co-processor

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2.2 Block Diagram

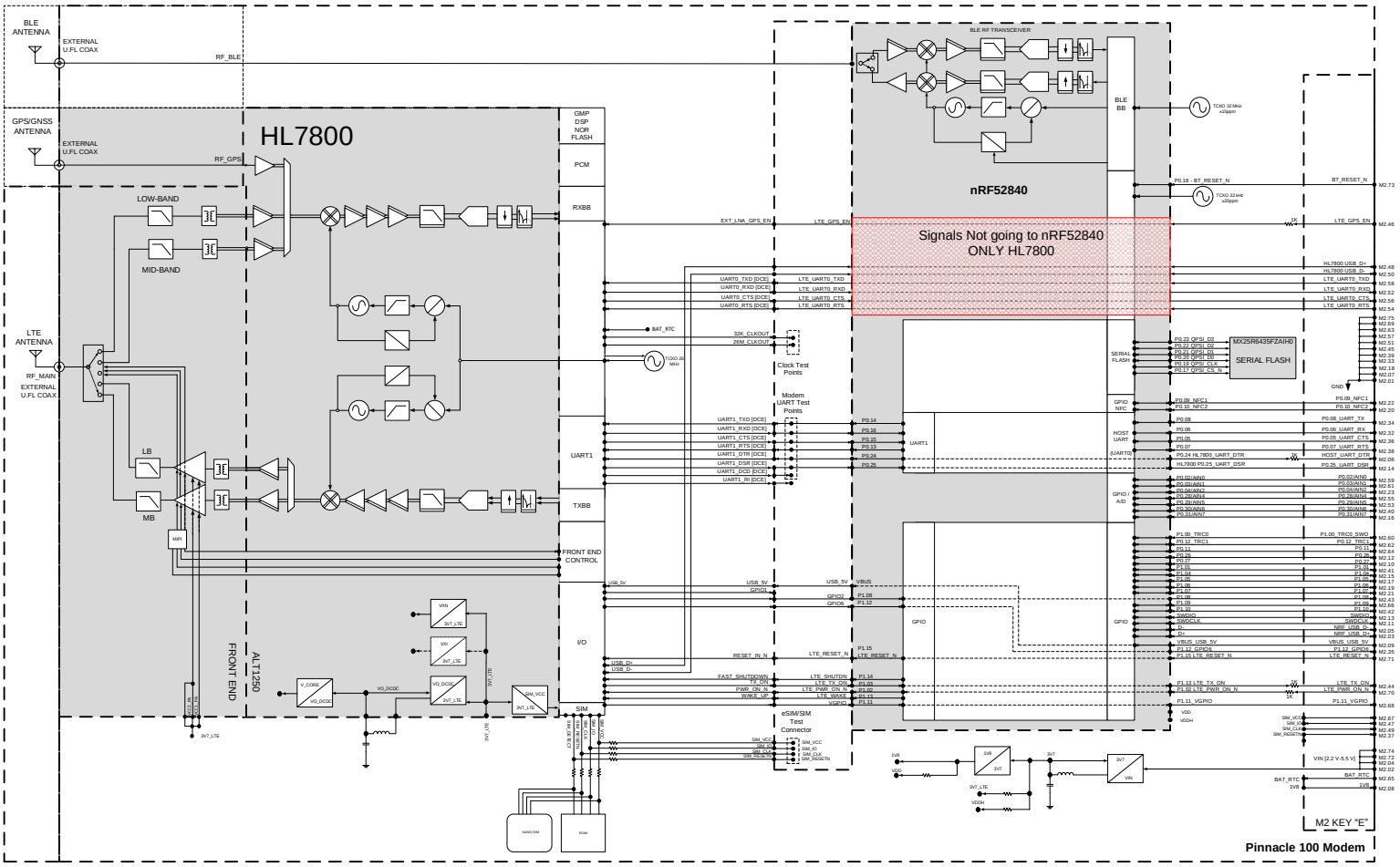

Figure 1: Pinnacle™ 100 block diagram

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2.3 Pin Definitions

Table 2: Pin definitions

Pin #	Pin Name	Default Function	Alternate Function	Type	In/ Out	Pull Up/ Down	Voltage Domain	nRF52840 HL7800 Pin	nRF52840 QFN HL7800 Name	Comment
1	GND			COM					GND	
2	VIN			PI	IN		DC-DC			2.2V – 5.5V
3	NRF_USB_D+	D+		DIO	IN		NRF	AD6 –	D+ –	J10
4	VIN			PI	IN		DC-DC			2.2V – 5.5V
5	NRF_USB_D-	D-	-	DIO	IN		NRF	AD4 –	D- –	J10
6	HOST_UART1_DTR	UART1_DTR		DO			HL			None
7	GND			COM					GND	
8	1V8			PO	OUT		LDO	–	–	1.8V LDO IO Ref
9	USB_5V			PI	IN		NRF HL	AD2 C16	VBUS USB_VBUS	4.35V – 5.5V 4.75V – 5.25V
10	P0.27	P0.27		DIO	IN	PULL-UP	NRF	H2 –	P0.27 –	I2C SCL –
11	SWDCLK	SWDCLK		DIO	IN	PULL-DOWN	NRF	AA24 –	SWDCLK –	SWDCLK –
12	P0.26	P0.26		DIO	IN	PULL-UP	NRF	G1 –	P0.26 –	I2C SDA –
13	SWDIO	SWDIO		DIO	IN	PULL-UP	NRF	AC24 –	SWDIO –	
14	P0.25_UART1_DSR	UART1_DSR		DO	OUT		HL	AC21 C9	P0.25 UART1_DSR	
15	P1.04	P1.04		DIO	IN	PULL-UP	NRF	U24 –	P1.04 –	LED1 (Blue) –
16	P0.31_AIN7	P0.31	AIN7	DIO AIO	IN	PULL-UP	NRF	A8 –	P0.31/AIN7 –	SW1 –
17	P1.05	P1.05		DIO	IN	PULL-UP	NRF	T23 –	P1.05 –	LED2 (Green) –
18	GND			COM					GND	
19	P1.06	P1.06		DIO	IN	PULL-UP	NRF	R24 –	P1.06 –	LED3 (Red) –
20	P0.10_NFC2	P0.10	NFC2	AIO	IN		NRF	J24 –	P0.10/NFC2 –	
21	P1.07	P1.07		DIO	IN	PULL-UP	NRF	P23 –	P1.07 –	LED4 (Green) –
22	P0.09_NFC1	P0.09	NFC1	AIO	IN		NRF	L24 –	P0.09/NFC1 –	
23	P0.04_AIN2	P0.04	AIN2	DIO AIO	IN	PULL-UP	NRF	J1 –	P0.04/AIN2 –	SW3 –
24-31	Mech Key E									
32	HOST_UART_RX	UART_RX		DO	OUT		NRF	L1 –	P0.06 –	
33	GND			COM					GND	
34	HOST_UART_TX	UART_TX		DI	IN	PULL-UP	NRF	N1 –	P0.08 –	
35	P1.12_GPIO6			DO			HL	–	P1.12 GPIO6	
36	HOST_UART_CTS	UART_CTS		DO	OUT		NRF	K2 –	P0.05/AIN3 –	
37	SIM_RST			DO			HL	– C29	– UIM1_RESET	– Support Ext SIM
38	HOST_UART_RTS	UART_RTS		DI	IN		NRF	M2 –	P0.07/TRACECLK –	
39	GND			COM					GND	

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Pin #	Pin Name	Default Function	Alternate Function	Type	In/ Out	Pull Up/ Down	Voltage Domain	nRF52840 HL7800 Pin	nRF52840 QFN HL7800 Name	Comment
40	P0.30_AIN6	P0.30	AIN6	DIO AIO			NRF	B9 –	P0.30/AIN6 –	
41	P1.01			DIO			NRF	Y23 –	P1.01 –	AUTORUN –
42	P1.10			DIO			NRF	A20 –	P1.10 –	
43	P1.08_GPIO2			DO			HL	P2 C10	P1.08 GPIO2	
44	TX_ON			DO	OUT		HL	V23 C60	P1.03 TX_ON	
45	GND			COM					GND	
46	GPS_LNA_EN			DI	IN		HL	– C43	– EXT_LNA_GPS_EN	
47	SIM_IO			DO			HL	– C28	– UIM1_DATA	– Support Ext SIM
48	HL_USB_D+			DIO			HL	– C13	– USB_D+	J7
49	SIM_CLK			DIO			HL	– C27	– UIM1_CLK	– Support Ext SIM
50	HL_USB_D-			DIO			HL	– C12	– USB_D-	J7
51	GND			COM					GND	
52	UART0_RX			DO			HL	– C55	– UART0_RX	– HL7800 Debug
53	P0.29_AIN5		AIN5	DIO AIO			NRF	A10 –	P0.29/AIN5 –	VIN_ADC
54	UART0_RTS			DI			HL	– C58	– UART0_RTS	– HL7800 Debug
55	P0.28_AIN4		AIN4	DIO AIO			NRF	B11 –	P0.28/AIN4 –	VIN_ADC_EN
56	UART0_CTS			DO			HL	– C57	– UART0_CTS	– HL7800 Debug
57	GND			COM					GND	
58	UART0_TX			DI			HL	– C56	– UART0_TX	– HL7800 Debug
59	P0.02_AIN0	P0.02	AIN0	DIO AIO			NRF	A12 –	P0.02/AIN0 –	SW4
60	P1.00_TRC0_SWO	P1.00	TRC0	DIO			NRF	AD22 –	P1.00/TRACEDATA0 –	
61	P0.03_AIN1	P0.03	AIN1	DIO AIO			NRF	B13 –	P0.03/AIN1 –	SW2
62	P0.12_TRC1	P0.12	TRC1	DIO			NRF	U1 –	P0.12/TRACEDATA1 –	
63	GND			COM					GND	
64	P0.11_TRC2	P0.11	TRC2	DIO			NRF	T2 –	P0.11/TRACEDATA2–	
65	BAT_RTC			PI			HL	– C21	– BAT_RTC	
66	P1.09_TRC3	P1.09	TRC3	DIO			NRF	R1 –	P1.09/TRACEDATA3 –	
67	1V8_SIM			PO			HL	– C26	– UIM1_VCC	– Support Ext SIM
68	P1.11_VGPIO	P1.11	VGPIO	DO			HL	B19 C45	P1.11 VGPIO	
69	GND			COM					GND	

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Pin #	Pin Name	Default Function	Alternate Function	Type	In/ Out	Pull Up/ Down	Voltage Domain	nRF52840 HL7800 Pin	nRF52840 QFN HL7800 Name	Comment
70	nPWR_ON			DI			HL	W24 C59	P1.02 PWR_ON_N	
71	nLTE_RESET			DO			HL	A14 C11	P1.15 RESET_IN_N	
72	VIN			PI	IN		DC-DC	–	–	2.2V – 5.5V
73	nBT_RESET			DI			NRF	AC13 –	P0.18/nRESET –	–
74	VIN			PI	IN		DC-DC			2.2V – 5.5V
75	GND			COM					GND	

Note:

AI = Analog Input
AO = Analog Output
AIO = Analog Input/Output
DI = Digital Input
DO = Digital Output
DIO = Digital Input/Output
PI = Power Supply Input
PO = Power Supply Output
COM = Common Ground

2.4 General Parameters

Table 3: General parameters

Parameter	Min	Typical	Max	Unit
VIN supply range	2.2	3.7	5.5	V
VBUS USB supply range	4.75	5.0	5.5	V
Antenna Options				
Integrated	▪ LTE Bent Metal and PCB Trace monopole antenna – on-modem **453-00010 variant**			
External	▪ LTE and BLE dipole antennas (with SMA and RPSMA connector) ▪ Flex carrier PCB antennas (with U.FL connector) **453-00011 variant**. Connection via 3 U.FL			
Physical				
Dimensions	PCI Express Key E Card Edge 453-00010: 48.30 mm x 49.00 mm x 12.89 mm 453-00011: 30.51 mm x 49.00 mm x 4.58 mm			
Weight	453-00010: 9.7 g 453-00011: 4.4 g			
Environmental				
Operating	-40 ˚C to +85 ˚C			
Storage	-40 ˚C to +125 ˚C			
Miscellaneous				
Lead Free	Lead-free and RoHS compliant			
Warranty	One-Year Warranty			
Development Tools				
Development Kit	Development kit per modem SKU (453-00010-K1 and 453-00011-K1)			
Approvals				
Bluetooth®	Full Bluetooth SIG Declaration ID			
FCC/IC/CE	*(Pending)*			

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Parameter	Min	Typical	Max	Unit
PTCRB/GFC		Pending, North America/EU *(Pending)*		
Carrier Certification		Verizon, AT&T, Vodafone *(Pending)*		

Note: Concerning the USB protection, customers should ***always*** add ESD protection to ***any*** interface that is exposed to the outside world. That being said, we do have a Panjit PE1605C2A_R1_00001 on the module at the M.2 connector for pins M.2-5 and M.2-3 as well as M2-50 and M2-48; there is no protection on M.2-9.

3 LTE Hardware Specifications

3.1 LTE RF Parameters

Table 4: LTE RF parameters

Parameter	Min	Typical	Max	Unit
LTE Band Support		1, 2, 3, 4, 5, 8*, 12, 13, 20, 28		
Max LTE TX Power (25°)	21.5	23	24.5	dBm
Rx Sensitivity (25°, 95% maximum throughput)				

Band	M1	GGPP Limit	NB1	GGPP Limit
1	-106			
2	-106	-100.3	-114.5	-107.5
3	-106			
4	-105.5	-102.3	-114	-107.5
5	-105	-100.8	-114	-107.5
8	-105			
12	-105	-99.3	-113.5	-107.5
13	-105.5	-99.3	-114	-107.5
20	-105	-98.3	-114	-107.5
28	-105			

Note: The HL 7800 can support additional LTE Bands, but the antennas and the certifications **DO NOT.**

***** Band 8 supported by Laird Connectivity's Dipole Blade DBA6927C1-FSMAM antenna

3.2 LTE Current

Table 5: LTE current parameters

Parameter @ 25C	2.2V Typ	3.7V Typ	5.5V Typ	Unit
LTE TX Average Current	550	250	200	mA
LTE TX Peak Current	950	650	600	mA
LTE RX Average Current		45		mA
LTE Hibernate		100		uA

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3.2.1 Typical Currents in while connected to LTE network

Using the Hosted firmware, Figure 2, shows the modem's current profile @ 3.7V from boot to establishing a connection to a LTE Cat-M1 Network; Boot 33mA (Marker 1); TX Peak Current 320 mA, Avg Current 63.25mA. Figure 3, shows the Connected RX Average Current: 32.17mA; Peak: 127.68mA. For Low Power Operation see CS-AN-Pinnacle-100-Low-Power-User Guide.pdf

Figure 2: Pinnacle™ 100 Modem Current Profile for boot and establishing a connection

Figure 3: Pinnacle™ 100 Modem Connected RX Current

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3.3 USB Interface Parameters

The HL7800 LTE module has one Universal Serial Bus Interface Full Speed to load firmware updates.

Table 6: USB interface parameters

Signal Name	M2 Pin No	I/O	Comments
D+	3	I/O	
D-	5	I/O	
VBUS	9		When using the Pinnacle™ 100 VBUS pin (which is mandatory when USB interface is used), you ***must*** externally connect a 4.7uF capacitor to ground. ***Note: MUST power the rest of Pinnacle™ 100 modem circuitry through the Vin 2.2-5.5V***

Note: When the USB is used, the lowest power mode supported is Sleep mode.

VBUS must not be connected if Hibernate or Lite Hibernate mode is used.

These signals will be available in future firmware.

3.4 GPS Parameters

3.4.1 LTE_GPS_LNA_EN (M2.46)

The modem M2.46 pin is connected to HL7800 through a series 1K resistor.

Note: This signal will be available in future firmware.

3.4.2 GPS Performance

The HL7800 supports GPS L1 signal (1575.42 ± 20 MHz) and GLONASS L1 FDMA signals (1597.5 – 1605.8 MHz), with 50Ω connection to CON2 (U.FL). The following GPS Performance is ***expected performance*** and not based on measurement.

Table 7: GPS performance

Parameter	Conditions	Typical Value
Sensitivity	Cold Start	-146 dBm
	Hot Start	-152 dBm
	Tracking	-161 dBm
TTFF	Cold Start, Input Power -130 dBm	35 s
	Hot Start, Input Power -130 dBm	2 s
2D Position Error	Input Power -130 dBm	2.5 m
Module Current	Input Power -130 dBm	63.8 mA

Note: The GPS receiver shares the same RF resources as the 4G receiver. The end-device target should allow GPS positioning for asset management applications where infrequent and no real-time position updates are required.

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3.5 BAT_RTC

The HL7800 has an input to connect a Real Time Clock power supply. This pin is used as a back-up power supply for the internal Real Time Clock. The RTC is supported when VIN is available, but a back-up power supply is needed to save date and hour when VIN is switched off.

Table 8 RTC battery parameters

Parameter	Min	Typical	Max	Unit
Input voltage	2.2	-	4.35	V
Input current consumption	-	-	10	µA

Note: This pin is input only and is not capable of charging a backup capacitor.

This signal will be available in future firmware

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4 BLE HARDWARE SPECIFICATIONS

Table 9: nRF BLE parameters

General		
Frequency	2.402 - 2.480 GHz	
Raw Data Rates	1 Mbps BLE (over-the-air) 2 Mbps BLE (over-the-air) 125 kbps BLE (over-the-air) 500 kbps BLE (over-the-air)	
Maximum Transmit Power Setting	+8 dBm	Conducted 453-00010 (Integrated LTE & BLE antennas)
	+8 dBm	Conducted 453-00011 (3 U. FL, external antenna)
Minimum Transmit Power Setting	-40 dBm	
Additional Transmit Power Settings	-20 dBm, -16 dBm, -12 dBm, -8 dBm, -4 dBm, 0 dBm, 2 dBm, 3 dBm, 4 dBm, 5 dBm, 6 dBm, 7 dBm	
Receive Sensitivity (≤37byte packet)	BLE 1 Mbps (BER=1E-3)	-93 dBm typical
	BLE 2 Mbps	-92 dBm typical
	BLE 500 kbps	-97 dBm typical
	BLE 125 kbps	-101 dBm typical
Link Budget (conducted)	99 dB	@ BLE 1 Mbps
	107 dB	@ BLE 125 kbps
NFC		
NFC-A Listen mode compliant	**Based on NFC forum specification** ▪ 13.56 MHz ▪ Date rate 106 kbps ▪ NFC Type2 and Type 4 emulation **Modes of Operation:** ▪ Disable ▪ Sense ▪ Activated **Use Cases:** ▪ Touch-to-Pair with NFC ▪ Standard Tag to exchange; EX: url Laucher **NFC enabled Out-of-Band Pairing**	
System Wake-On-Field function	▪ Proximity Detection	
Host Interfaces and Peripherals		
Total	**18 x multifunction I/O lines**	
UART	▪ 1 UART (second UART interface connected to HL7800 internally) ▪ Tx, Rx, CTS, RTS ▪ Default 115200, n, 8, 1 ▪ From 1,200 bps to 1 Mbps	
USB	▪ USB 2.0 FS (Full Speed, 12Mbps). ▪ CDC driver / Virtual UART	
GPIO	Up to 18, configurable by firmware: ▪ I/O direction ▪ O/P drive strength (standard 0.5 mA or high 3 mA) ▪ Pull-up /pull-down ▪ Input buffer disconnect	

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ADC	▪ Seven 8/10/12-bit channels ▪ 0.6 V internal reference ▪ Configurable 4, 2, 1, 1/2, 1/3, 1/4, 1/5, 1/6 (default) pre-scaling ▪ Configurable acquisition time 3uS, 5uS, 10uS (default), 15uS, 20uS, 40uS ▪ One-shot mode
PWM Output	PWM outputs on 16 GPIO output pins. ▪ PWM output duty cycle: 0%-100% PWM output frequency: Up to 500 kHz
I2C	▪ Two I2C interface (up to 400 kbps)
SPI	Four SPI Master Slave interface (up to 4 Mbps)
QSPI	Not Available, Modem contains 8Mbit x 4 (64 Mbit) IC
Temperature Sensor	▪ One temperature sensor ▪ Temperature range equal to the operating temperature range ▪ Resolution 0.25°, Accuracy +/- 5°C
RSSI Detector	▪ One RF received signal strength indicator ▪ ±2 dB accuracy (valid over -90 to -20 dBm) ▪ One dB resolution
I2S	One inter-IC sound interface
PDM	One pulse density modulation interface
External 32.768 kHz crystal	For more accurate timing
Profiles	
Services supported	▪ Central mode ▪ Peripheral mode ▪ Mesh (with custom models) Custom and adopted profiles
Programmability	
Zephyr or AT command Set	via SWD
Operating Modes	
Zephyr or AT command Set	Per examples
Power Consumption	
Active Modes Average Current (for maximum Tx power +8 dBm)	14.4 mA peak Tx @ 3.7V
Active Modes Average Current (for Tx power -40 dBm)	6.8 mA peak Tx @ 3.7V

4.1 Programmability

4.1.1 Bootloader

The modem comes with a secure bootloader.

4.1.2 Zephyr Hostless Firmware

The Zephyr firmware provides a hostless example code used for the Out of Box demo (OOB). The modem is capable of taking readings from external BLE sensor and sending data to AWS.

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4.1.3 Hosted Firmware

The Hosted firmware provides a hosted example code.

4.2 Electrical Specifications

4.2.1 Recommended Operating Parameters

Table 10: Signal levels for interface, SIO

Parameter	Min	Typical	Max	Unit
V_{IH} Input high voltage	0.7 x 1.8V		1.8V	V
V_{IL} Input low voltage	VSS		0.3 x 1.8V	V
V_{OH} Output high voltage				
(std. drive, 0.5mA)	1.8V -0.4		1.8V	V
(high drive, 3mA)	1.8V -0.4		1.8V	V
V_{OL} Output low voltage				
(std. drive, 0.5mA)	VSS		VSS+0.4	V
(high drive, 3mA)	VSS		VSS+0.4	V
V_{OL} Current at VSS+0.4V, Output set low				
(std. drive, 0.5mA)	1	2	4	mA
(high drive, 3mA)	3	-	-	mA
V_{OL} Current at 1.8V -0.4, Output set low				
(std. drive, 0.5mA)	1	2	4	mA
(high drive, 3mA)	3	-	-	mA
Pull up resistance	11	13	16	kΩ
Pull down resistance	11	13	16	kΩ
Pad capacitance		3		pF
Pad capacitance at NFC pads		4		pF

Table 11: SIO pin alternative function AIN (ADC) specification

Parameter	Min	Typical	Max	Unit
Maximum sample rate			**200**	**kHz**
ADC Internal reference voltage	-1.5%	0.6 V	+1.5%	%
ADC pin input internal selectable scaling		4, 2, 1, 1/2, 1/3, 1/4, 1/5, 1/6		scaling
ADC input pin (AIN) voltage maximum without damaging ADC w.r.t (see Note 1)				
VCC Prescaling				
0V-1.8V 4, 2, 1, ½, 1/3, ¼, 1/5, 1/6		1.8V+0.3		V
Configurable Resolution	8-bit mode	10-bit mode	12-bit mode	bits
Configurable (see Note 2)				
Acquisition Time, source resistance ≤10 kΩ		3		uS
Acquisition Time, source resistance ≤40 kΩ		5		uS
Acquisition Time, source resistance ≤100 kΩ		10		uS
Acquisition Time, source resistance ≤200 kΩ		15		uS
Acquisition Time, source resistance ≤400 kΩ		20		uS
Acquisition Time, source resistance ≤800 kΩ		40		uS
Conversion Time (see Note 3)		<2		uS

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Parameter	Min	Typical	Max	Unit
Maximum sample rate			**200**	**kHz**
ADC input impedance (during operation) (see Note 3)				
Input Resistance		>1		MOhm
Sample and hold capacitance at maximum gain		2.5		pF

Recommended Operating Parameters Notes:

Note 1	Stay within internal 0.6 V reference voltage with given pre-scaling on AIN pin and do not violate ADC maximum input voltage 1.8V (for damage).
Note 2	Firmware allows configurable resolution (8-bit, 10-bit, or 12-bit mode) and acquisition time. Pinnacle™ 100 ADC is a Successive Approximation type ADC (SSADC), as a result no external capacitor is needed for ADC operation. Configure the acquisition time according to the source resistance that customer has. The sampling frequency is limited by the sum of sampling time and acquisition time. The maximum sampling time is 2us. For acquisition time of 3us the total conversion time is therefore 5us, which makes maximum sampling frequency of 1/5us = 200kHz. Similarly, if acquisition time of 40us chosen, then the conversion time is 42us and the maximum sampling frequency is 1/42us = 23.8kHz.
Note 3	ADC input impedance is estimated mean impedance of the ADC (AIN) pins.

4.3 BLE Power Consumption

Table 12: BLE Power consumption

Parameter	2.2V Typ	3.7V Typ	5.5V Typ	Unit
Active mode 1Mbps 'avg' current (Note 1) **(Advertising or Connection)**	DCDC [LDO]	DCDC [LDO]	DCDC [LDO]	
Tx only run peak current @ Pwr Step = +8 dBm	25.4 [50.3]	14.4 [28.5]	12.0 [23.0]	mA
Tx only run peak current @ Pwr Step= +7 dBm	23.5 [46.5]	13.5 [27.0]	11.4 [21.3]	mA
Tx only run peak current @ Pwr Step= +6 dBm	22.4 [44.3]	12.7 [25.1]	11.0 [20.1]	mA
Tx only run peak current @ Pwr Step= +5 dBm	20.5 [40.7]	11.7 [22.8]	10.2 [18.8]	mA
Tx only run peak current @ Pwr Step= +4 dBm	19.7 [38.9]	11.6 [21.6]	9.9 [17.7]	mA
Tx only run peak current @ Pwr Step= +3 dBm	18.8 [36.7]	10.9 [20.3]	9.2 [17.1]	mA
Tx only run peak current @ Pwr Step= +2 dBm	17.6 [34.2]	10.2 [18.8]	8.8 [15.7]	mA
Tx only run peak current @ Pwr Step = 0 dBm	14.2 [25.7]	8.5 [14.4]	7.5 [12.0]	mA
Tx only run peak current @ Pwr Step = -4 dBm	13.1 [22.7]	7.4 [12.9]	7.0 [11.3]	mA
Tx only run peak current @ Pwr Step = -8 dBm	12.5 [21.5]	7.3 [12.6]	6.8 [10.4]	mA
Tx only run peak current @ Pwr Step = -12 dBm	12.2 [20.5]	7.2 [11.9]	6.7 [10.3]	mA
Tx only run peak current @ Pwr Step = -16 dBm	11.8 [19.8]	7.2 [11.1]	6.6 [9.9]	mA
Tx only run peak current @ Pwr Step = -20 dBm	11.7 [19.4]	7.1 [11.2]	6.4 [9.4]	mA
Tx only run peak current @ Pwr Step = -40 dBm	11.2 [17.9]	6.8 [10.5]	6.3 [9.2]	mA
Active mode 2Mbps 'avg' current (Note 1) **(Advertising or Connection)**	DCDC [LDO]	DCDC [LDO]	DCDC [LDO]	
Tx only run peak current @ Pwr Step = +8 dBm	17.5 [32.0]	10.3 [18.3]	8.9 [15.3]	mA
Tx only run peak current @ Pwr Step= +7 dBm	16.7 [30.0]	9.5 [17.2]	8.6 [14.2]	mA
Tx only run peak current @ Pwr Step= +6 dBm	15.9 [28.9]	9.3 [16.2]	8.2 [13.6]	mA
Tx only run peak current @ Pwr Step= +5 dBm	15.0 [27.0]	8.9 [15.2]	7.9 [12.9]	mA
Tx only run peak current @ Pwr Step= +4 dBm	14.7 [25.9]	8.7 [14.6]	7.7 [12.3]	mA
Tx only run peak current @ Pwr Step= +3 dBm	14.0 [24.7]	8.1 [14.1]	7.6 [12.1]	mA
Tx only run peak current @ Pwr Step= +2 dBm	13.3 [23.4]	7.9 [13.2]	7.1 [11.5]	mA

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Parameter	2.2V Typ	3.7V Typ	5.5V Typ	Unit
Tx only run peak current @ Pwr Step = 0 dBm	11.5 [19.3]	6.9 [11.0]	6.4 [9.5]	mA
Tx only run peak current @ Pwr Step = -4 dBm	10.8 [17.5]	6.3 [10.0]	6.1 [9.1]	mA
Tx only run peak current @ Pwr Step = -8 dBm	10.8 [17.0]	6.5 [9.7]	6.1 [8.8]	mA
Tx only run peak current @ Pwr Step = -12 dBm	10.5 [16.3]	6.3 [9.9]	6.0 [8.5]	mA
Tx only run peak current @ Pwr Step = -16 dBm	10.4 [16.0]	6.3 [9.2]	6.0 [8.3]	mA
Tx only run peak current @ Pwr Step = -20 dBm	10.4 [15.9]	6.2 [9.2]	5.9 [8.4]	mA
Tx only run peak current @ Pwr Step = -40 dBm	10.0 [14.9]	6.1 [9.0]	5.9 [8.0]	mA
Active mode 500Kbps 'avg' current (Note 1) **(Advertising or Connection)**	DCDC [LDO]	DCDC [LDO]	DCDC [LDO]	
Tx only run peak current @ Pwr Step = +8 dBm	23.4 [46.1]	13.1 [26.2]	11.1 [21.2]	mA
Tx only run peak current @ Pwr Step= +7 dBm	21.3 [42.7]	12.2 [24.0]	10.6 [19.8]	mA
Tx only run peak current @ Pwr Step= +6 dBm	20.4 [40.8]	11.5 [22.8]	10.4 [18.7]	mA
Tx only run peak current @ Pwr Step= +5 dBm	18.6 [37.2]	10.9 [20.8]	9.6 [17.0]	mA
Tx only run peak current @ Pwr Step= +4 dBm	17.9 [36.0]	10.2 [19.7]	9.0 [16.0]	mA
Tx only run peak current @ Pwr Step= +3 dBm	17.0 [33.9]	10.0 [18.8]	8.8 [16.0]	mA
Tx only run peak current @ Pwr Step= +2 dBm	16.1 [31.5]	9.3 [17.3]	8.3 [14.5]	mA
Tx only run peak current @ Pwr Step = 0 dBm	12.8 [23.6]	7.5 [13.4]	7.0 [11.4]	mA
Tx only run peak current @ Pwr Step = -4 dBm	11.7 [20.8]	7.2 [11.9]	6.5 [10.3]	mA
Tx only run peak current @ Pwr Step = -8 dBm	11.1 [19.9]	6.8 [11.0]	6.5 [9.7]	mA
Tx only run peak current @ Pwr Step = -12 dBm	11.0 [18.7]	6.6 [10.9]	6.3 [9.4]	mA
Tx only run peak current @ Pwr Step = -16 dBm	10.7 [18.4]	6.6 [10.7]	6.2 [9.3]	mA
Tx only run peak current @ Pwr Step = -20 dBm	10.6 [17.8]	6.4 [10.4]	6.1 [9.2]	mA
Tx only run peak current @ Pwr Step = -40 dBm	10.0 [16.5]	6.2 [9.7]	6.0 [8.7]	mA
Active mode 125Kbps 'avg' current (Note 1) **(Advertising or Connection)**	DCDC [LDO]	DCDC [LDO]	DCDC [LDO]	
Tx only run peak current @ Pwr Step = +8 dBm	30.7 [61.3]	17.2 [34.7]	14.2 [27.8]	mA
Tx only run peak current @ Pwr Step= +7 dBm	27.9 [56.6]	15.8 [31.7]	13.1 [24.8]	mA
Tx only run peak current @ Pwr Step= +6 dBm	26.4 [53.6]	14.8 [29.8]	12.5 [23.7]	mA
Tx only run peak current @ Pwr Step= +5 dBm	24.1 [48.8]	13.6 [27.1]	11.4 [21.6]	mA
Tx only run peak current @ Pwr Step= +4 dBm	22.9 [46.5]	12.9 [25.8]	11.1 [20.8]	mA
Tx only run peak current @ Pwr Step= +3 dBm	21.5 [44.0]	12.3 [24.0]	10.5 [19.7]	mA
Tx only run peak current @ Pwr Step= +2 dBm	20.1 [40.6]	11.5 [22.1]	10.1 [17.8]	mA
Tx only run peak current @ Pwr Step = 0 dBm	15.7 [29.0]	9.1 [16.1]	8.0 [13.5]	mA
Tx only run peak current @ Pwr Step = -4 dBm	14.0 [25.2]	8.2 [13.9]	7.3 [11.8]	mA
Tx only run peak current @ Pwr Step = -8 dBm	13.4 [23.4]	8.0 [13.6]	7.1 [11.4]	mA
Tx only run peak current @ Pwr Step = -12 dBm	12.7 [21.2]	7.7 [12.7]	6.8 [10.7]	mA
Tx only run peak current @ Pwr Step = -16 dBm	12.8 [21.2]	7.6 [12.2]	6.8 [10.5]	mA
Tx only run peak current @ Pwr Step = -20 dBm	12.4 [20.8]	7.5 [11.8]	6.6 [10.0]	mA
Tx only run peak current @ Pwr Step = -40 dBm	11.8 [19.0]	7.2 [10.8]	6.3 [9.1]	mA
Active Mode	DCDC [LDO]	DCDC [LDO]	DCDC [LDO]	
Rx only 'avg' current, BLE 1Mbps (Note 1)	8.5[14.2]	9.6[16.9]	16.4[30.5]	mA
Rx only 'avg' current, BLE 2Mbps (Note 2)	9.0[15.2]	10.1[18.2]	17.4[33.0]	mA
Rx only 'avg' current, BLE 500Kbps (Note 2)	8.6[14.0]	9.4[16.6]	16.1[29.9]	mA
Rx only 'avg' current, BLE 125Kbps (Note 2)	8.3[14.0]	9.5[16.6]	16.2[29.8]	mA
Ultra-Low Power Mode 1 (Note 2) Standby Doze, 256k RAM retention				uA

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Parameter	2.2V Typ	3.7V Typ	5.5V Typ	Unit
Ultra-Low Power Mode 2 (Note 3)				
Deep Sleep (no RAM retention)				uA
Active Mode Average current (Note 4)				
Advertising Average Current draw				
Max, with advertising interval (min) 20 mS		Note 4		uA
Min, with advertising interval (max) 10240 mS		Note 4		uA
Connection Average Current draw				
Max, with connection interval (min) 7.5 mS		Note 4		uA
Min, with connection interval (max) 4000 mS		Note 4		uA

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Power Consumption Notes:

Note 1	This is for avg Radio Current only.

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Power Consumption Notes:

Note 2	Pinnacle™ 100 BLE chipset Standby Doze is 100 uA typical. Depending on active peripherals, current consumption ranges from 100 µA to 370 uA (when UART is ON). The Pinnacle™ 100 Standby Doze current consists of the below nRF52840 blocks:

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Power Consumption Notes:

Note 3	In Deep Sleep, everything is disabled and the only wake-up sources (including NFC to wakeup) are reset and changes on SIO or NFC pins on which sense is enabled. The current consumption seen is ~65 uA typical in Pinnacle™ 100 modems. ▪ Coming out from Deep Sleep to Standby Doze through the reset vector.

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Power Consumption Notes:

Note 4	Average current consumption depends on several factors (including Tx power, VCC, and accuracy of 32MHz and 32.768 kHz crystals). With these factors fixed, the largest variable is the advertising or connection interval set. Advertising Interval range: ▪ 20 milliseconds to 10240 mS (10485759.375 mS in BT5.0) in multiples of 0.625 milliseconds. For an advertising event: ▪ The minimum average current consumption is when the advertising interval is large 10240 mS (10485759.375 mS (in BT5.0) although this may cause long discover times (for the advertising event) by scanners ▪ The maximum average current consumption is when the advertising interval is small 20 mS Other factors that are also related to average current consumption include the advertising payload bytes in each advertising packet and whether it's continuously advertising or periodically advertising. Connection Interval range (for a peripheral): ▪ 7.5 milliseconds to 4000 milliseconds in multiples of 1.25 milliseconds. For a connection event (for a peripheral device): ▪ The minimum average current consumption is when the connection interval is large 4000 milliseconds ▪ The maximum average current consumption is with the shortest connection interval of 7.5 ms; no slave latency. Other factors that are also related to average current consumption include: ▪ Number packets per connection interval with each packet payload size ▪ An inaccurate 32.768 kHz master clock accuracy would increase the average current consumption. Connection Interval range (for a central device): ▪ 2.5 milliseconds to 40959375 milliseconds in multiples of 1.25 milliseconds.

4.4 Clocks and Timers

4.4.1 Clocks

The integrated high accuracy 32 MHz (±10 ppm) crystal oscillator helps with radio operation and reducing power consumption in the active modes.

A 32.768 kHz (±20 ppm) crystal is also available for more accurate real time clock.

4.5 Radio Frequency (RF)

- 2402–2480 MHz Bluetooth Low Energy radio BT5.0 – 1 Mbps, 2 Mbps, and Long-range (125 kbps and 500 kbps) over-the-air data rate.
- Tx output programmable power steps include 8 dBm, 7dBm, 6dBm, 5dBm, 4dBm, 3dBm, 2dBm, 0dBm and further down to -20 dBm in steps of 4 dB and final TX power level of -40 dBm. The Pout of the modem will be 1-2 dB lower than the Power setting due to the Insertion Loss of a Bandpass filter.
- Receiver (with integrated channel filters) to achieve maximum sensitivity: -93 dBm @ 1 Mbps BLE, -92 dBm @ 2 Mbps, -97 dBm @ 500 kbps long-range, and -101 dBm @ 125 kbps long-range).
- RF conducted interface available with 453-00011 modem via the U.FL RF connectors: LTE, GPS, and BLE

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- Antenna options:
  - Integrated PCB trace antenna on the 453-00010
  - External antenna connected with 3 U.FL connectors on the 453-00011
- Received Signal Strength Indicator (RSSI)
- RSSI accuracy (valid range -90 to -20 dBm) is ±2 dB typical
- RSSI resolution 1 dB typical

4.6 NFC

NFC support:

- Based on the NFC forum specification
  - 13.56 MHz
  - Date rate 106 kbps
  - NFC Type2 and Type4 tag emulation
- Modes of operation
  - Disable
  - Sense
  - Activated

4.6.1 Use Cases

- Touch-to Pair with NFC
- Launch a smartphone app (on Android)
- NFC enabled Out-of-Band Pairing
- System Wake-On-Field function
- Proximity Detection

Table 13: NFC interface

Signal Name	M2 Pin No	I/O	Comments
NFC1/SIO_09	22	I/O	The NFC pins are by default GPIO and must be configured in firmware.
NFC2/SIO_10	20	I/O	

4.6.2 NFC Antenna Coil Tuning Capacitors

From Nordic's *nRF52840 Objective Product Specification v1.0*: http://infocenter.nordicsemi.com/pdf/nRF52840_PS_v1.0.pdf

The NFC antenna coil must be the connected differential between the NFC1 and NFC2 pins of the Pinnacle™ 100. Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz (*Figure 4*).

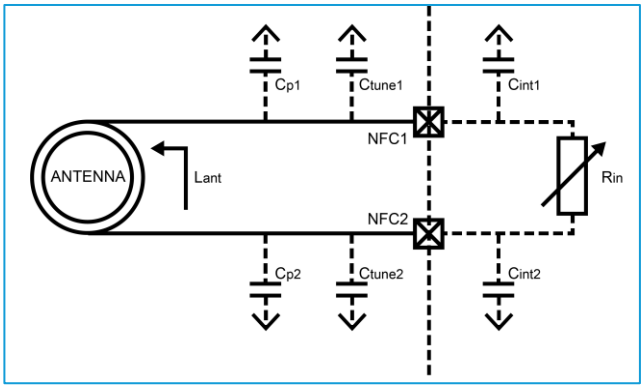

Figure 4: NFC antenna coil tuning capacitors

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The required external tuning capacitor value is given by the following equations:

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} - C_{tune} - C_{int}$$

An antenna inductance of L_{ant} = 0.72 uH provides tuning capacitors in the range of 300 pF on each pin. The total capacitance on NFC1 and NFC2 must be matched. C_{int} and C_p are small usually (C_{int} is 4pF), so can omit from calculation.

Battery Protection Note: If the NFC coil antenna is exposed to a strong NFC field, the supply current may flow in the opposite direction due to parasitic diodes and ESD structures.

If the used battery does not tolerate a return current, a series diode must be placed between the battery and the Pinnacle™ 100 to protect the battery.

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4.7 Primary UART Interface

Note: The Pinnacle™ 100 has two UARTs.

The Universal Asynchronous Receiver/Transmitter (UART) offers fast, full-duplex, asynchronous serial communication with built-in flow control support (UART_CTS, UART_RTS) in HW up to one Mbps baud. Parity checking and generation for the ninth data bit are supported.

UART_TX, UART_RX, UART_RTS, and UART_CTS form a conventional asynchronous serial data port with handshaking. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signaling levels are nominal 0 V and 1.8 V and are inverted with respect to the signaling on an RS232 cable.

Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and UART_CTS is an input. Both are active low.

These signals operate according to normal industry convention. UART_RX, UART_TX, UART_CTS, and UART_RTS are all 1.8V level logic. For example, when RX and TX are idle they sit at 1.8 V. Conversely for handshaking pins, CTS and RTS, at 0 V is treated as an assertion.

The modem communicates with the customer application using the following signals:

- Port/TxD of the application sends data to the modem's UART_RX signal line
- Port/RxD of the application receives data from the modem's UART_TX signal line

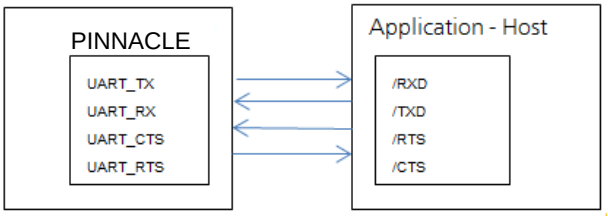

Figure 5: UART signals

Note: The Pinnacle™ 100 serial modem output is at 1.8V logic levels. Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS other than for testing and prototyping. If these pins are linked and the host sends data at the point that the Pinnacle™ 100 de-asserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This will drop the connection and may require a power cycle to reset the modem. We recommend that the correct CTS/RTS handshaking protocol be adhered to for proper operation.

Table 14: UART interface

Signal Name	M2 Pin No	I/O	Comments
SIO_06 / HOST_UART_Tx	34	I	SIO_06 (alternative function HOST_UART_Tx) is an input, set high (in firmware).
SIO_08 / HOST_UART_Rx	32	O	SIO_08 (alternative function HOST_UART_Rx) is an output, set with internal pull-up (in firmware).
SIO_05 / HOST_UART_RTS	38	I	SIO_05 (alternative function HOST_UART_RTS) is an input, set low (in firmware).
SIO_07 / HOST_UART_CTS	36	O	SIO_07 (alternative function HOST_UART_CTS) is an output, set with internal pull-down (in firmware).

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4.8 HL7800 to nRF52840 UART interface

The UART between the HL7800 and NRF52840 consists of the flowing signals: TXD, RXD, CTS, RTS, DTR, DSR, DCD & RI. The signals are available on a non-populated header J2. The Digi-Key Part number: S9014E-06-ND, which is a Sullins Connector Solutions; GRPB061VWVN-RC; CONN HEADER VERT 6POS 1.27MM, that can be solder to the modem to provide access to the UART lines.

Table 15: UART interface

J2 Pin # net	HL7800	nRF52840	Comments
1	UART1_DCD	-	
2	UART1_DTR	P0.24	SIO_24 is an output, set high (in firmware).
3	UART1_RX	P0.16	SIO_16 is an input, set with internal pull-up (in firmware).
4	UART1_TX	P0.14	SIO_14 is an output, set high (in firmware).
5	UART1_CTS	P0.15	SIO_15 is an input, set with internal pull-down (in firmware).
6	UART1_RTS	P0.13	SIO_13 is an output, set low (in firmware).
-	UART1_DSR	P0.25	SIO_25 is an input, set with internal pull-up (in firmware).
-	UART1_RI	-	TP1 on Top of Pinnacle™100 next to J2

4.9 USB interface

Pinnacle™ 100 has USB2.0 FS (Full Speed, 12Mbps) hardware capability.

Table 16: USB interface

Signal Name	M2 Pin No	I/O	Comments
D+	3	I/O	
D-	5	I/O	
VBUS	9		When using the Pinnacle™ 100 VBUS pin (which is mandatory when USB interface is used), **MUST** connect externally a 4.7uF capacitor to ground. ***Note: MUST power the rest of Pinnacle™ 100 modem circuitry through the Vin = 2.2 - 5.5V***

4.10 SPI Bus

The SPI interface is an alternate function on SIO pins.

The modem is a master device that uses terminals SPI_MOSI, SPI_MISO, and SPI_CLK. SPI_CS is implemented using any spare SIO digital output pins to allow for multi-dropping.

The SPI interface enables full duplex synchronous communication between devices. It supports a 3-wire (SPI_MOSI, SPI_MISO, SPI_SCK,) bi-directional bus with fast data transfers to and from multiple slaves. Individual chip select signals are necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of SIO signals. I/O data is double buffered.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

Table 17: SPI interfaces

Signal Name	M2 Pin No	I/O	Comments
SIO_40/SPI_MOSI	60	O	
SIO_12/SPI_MISO	62	I	
SIO_11/SPI_CLK	64	O	
Any_SIO/SPI_CS	-	I	SPI_CS is implemented using any spare SIO digital output pins to allow for multi-dropping.

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4.11 I2C Interface

The I2C interface is an alternate function on SIO pins.

The two-wire interface can interface a bi-directional wired-OR bus with two lines (SCL, SDA) and has master /slave topology. The interface is capable of clock stretching. Data rates of 100 kbps and 400 kbps are supported.

An I2C interface allows multiple masters and slaves to communicate over a shared wired-OR type bus consisting of two lines which normally sit at 1.8V. The SCL is the clock line which is always sourced by the master and SDA is a bi-directional data line which can be driven by any device on the bus.

IMPORTANT: It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the modem and **MUST** be provided external to the modem.

Table 18: I2C interface

Signal Name	M2 Pin No	I/O	Comments
SIO_26/I2C_SDA	12	I/O	This interface is an alternate function on each pin.
SIO_27/I2C_SCL	10	I/O	

4.12 General Purpose I/O, ADC, & PWM

4.12.1 GPIO

The 19 SIO pins are configurable via firmware. They can be accessed individually. Each has the following user configured features:

- Input/output direction
- Output drive strength (standard drive 0.5 mA or high drive 3mA)
- Internal pull-up and pull-down resistors (13 K typical) or no pull-up/down or input buffer disconnect
- Wake-up from high or low-level triggers on all pins including NFC pins

4.12.2 ADC

The ADC is an alternate function on SIO pins, configurable by firmware.

The Pinnacle™ 100 provides access to 8-channel 8/10/12-bit successive approximation ADC in one-shot mode. This enables sampling up to 8 external signals through a front-end MUX. The ADC has configurable input and reference pre-scaling and sample resolution (8, 10, and 12 bit).

4.12.2.1 Analog Interface (ADC)

Table 19: Analog interface

Signal Name	M2 Pin No	I/O	Comments
SIO_02/AIN0 – Analog Input	59	I	This interface is an alternate function of each pin, Configurable 8, 10, 12-bit resolution. Configurable voltage scaling 4, 2, 1/1, 1/3, 1/3, 1/4, 1/5, 1/6 (default). Configurable acquisition time 3uS, 5uS, 10uS (default), 15uS, 20uS, 40uS. Full scale input range (1.8V)
SIO_03/AIN1 – Analog Input	61	I	
SIO_04/AIN2 – Analog Input	23	I	
SIO_05/AIN3 – Analog Input	36	I	
SIO_28/AIN4 – Analog Input	55	I	
SIO_29/AIN5 – Analog Input	53	I	
SIO_30/AIN6 – Analog Input	40	I	
SIO_31/AIN7 – Analog Input	16	I	

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4.12.3 PWM Signal Output on Up to 16 SIO Pins

The PWM output is an alternate function on ALL (GPIO) SIO pins, configurable by firmware.

The **PWM output** signal has a frequency and duty cycle property. Frequency is adjustable (up to 1 MHz) and the duty cycle can be set over a range from 0% to 100%.

PWM output signal has a frequency and duty cycle property. PWM output is generated using dedicated hardware in the chipset. There is a trade-off between PWM output frequency and resolution.

For example:

- PWM output frequency of 500 kHz (2 uS) results in resolution of 1:2.
- PWM output frequency of 100 kHz (10 uS) results in resolution of 1:10.
- PWM output frequency of 10 kHz (100 uS) results in resolution of 1:100.
- PWM output frequency of 1 kHz (1000 uS) results in resolution of 1:1000

4.13 nRESET pin

Table 20: nRESET pin

Signal Name	M2 Pin No	I/O	Comments
nRESET	73	I	Pinnacle™ 100 HW reset (active low). Pull the nRESET pin low for minimum 100mS for the Pinnacle™ 100 to reset.

4.14 Two-Wire Interface SWD

Table 21: SWD pins

Signal Name	M2 Pin No	I/O	Comments
SWDIO	13	I/O	Internal pull-up resistor
SWDCLK	11	I	Internal pull-down resistor

The Laird Connectivity development board incorporates an on-board SWD programmer for this purpose. There is also the following SWD connector which allows on-board SWD debug and programming signals to be routed off the development board. The only requirement is that you should use the following SWD connector on the host PCB.

The SWD connector Manufacture Part number is as follows:

Table 22 Programing Header

Reference	Part	Description and MPN (Manufacturers Part Number)
J14	FTSH-105	Header, 1.27mm, SMD, 10-way, FTSH-105-01-L-DV Samtech

Note: Reference on the Pinnacle™ 100 development board schematic (Figure 6) shows the DVK development schematic wiring only for the JTAG connector and the Pinnacle™ 100 modem JTAG pins.

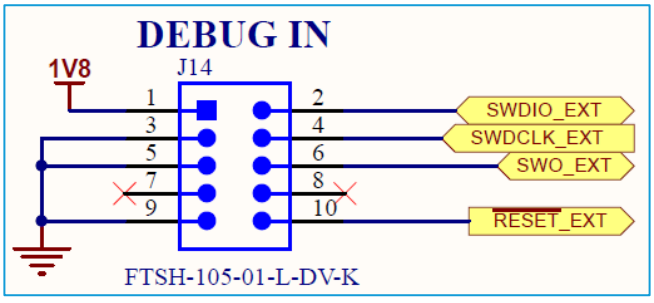

Figure 6: Pinnacle™ 100 development board schematic

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Note: The Pinnacle™ 100 development board allows Laird Connectivity on-board SWD programmer signals to be routed off the development board by connector J14

We highly recommend that you place the SWD header to handle future Pinnacle™ 100 modem firmware upgrades. You **MUST** wire out the SWD interface on your host design (see Figure 6, Required Signals SWDIO, SWDCLK, 1V8, & GND).

The SWO signal (SIO_32. M2.60) is a Trace output (called SWO, Serial Wire Output) and is **not** necessary for programming Pinnacle™ 100 over the SWD interface.

nRESET_BLE is **not** necessary for programming Pinnacle™ 100 over the SWD interface.

4.15 Pinnacle™ 100 Wakeup

4.15.1 Waking Up Pinnacle™ 100 from Host

The Pinnacle™ 100 can be woke up from the host using wake-up pins (any SIO pin). Pins may be configured in the firmware:

- Wake up when signal is low
- Wake up when signal is high
- Wake up when signal changes

4.16 Low Power Modes

The Pinnacle™ 100 support Low Power Mode, but current software is not optimized.

4.17 Security/Privacy

4.17.1 Random Number Generator

For Nordic related functionality, visit Nordic infocenter.nordicsemi.com

4.17.2 AES Encryption/Decryption

For Nordic related functionality, visit Nordic infocenter.nordicsemi.com

4.17.3 ARM Cryptocell

ARM Cryptocell incorporates a true random generator (TRNG) and support for a wide range of asymmetric, symmetric and hashing cryptographic services for secure applications.

4.17.4 Readback Protection

The Pinnacle™100 supports readback protection capability that disallows the reading of the memory on the nrf52840 using a JTAG interface.

4.17.5 Elliptic Curve Cryptography

The Pinnacle™100 offers a range of functions for generating public/private keypair, calculating a shared secret, as well as generating an authenticated hash.

4.18 External 32.768 kHz crystal

The Pinnacle™ 100 includes modem operation.

The Pinnacle™ 100 can use either the on-chip 32.76 kHz RC oscillator (LFCLK) by default (which has an accuracy of ±500 ppm) which requires regulator calibration (every eight seconds) to within ±500 ppm.

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Or can use (Default) the external high accuracy (±20 ppm) 32.768 kHz crystal (and associated load capacitors) that are connected to the nRF. Table 23 compares the current consumption difference between RC and crystal oscillator.

Table 23: Comparing current consumption difference between Pinnacle™ 100 on-chip RC 32.76 kHz oscillator and external crystal (32.768 kHz) based oscillator

	Pinnacle™ 100 On-chip 32.768 kHz RC Oscillator (±500 ppm) LFRC	Optional External Higher Accuracy (±20 ppm) 32.768 kHz Crystal-based Oscillator LFXO
Current Consumption of 32.768 kHz Block	0.7 uA	0.23 uA
Standby Doze Current (SYSTEM ON IDLE + full RAM retention + RTC run current + LFRC or LFXO)	3.1 uA	2.6 uA
Calibration	Calibration required regularly (default eight seconds interval). Calibration takes 33 ms; with DC-DC used, the total charge of a calibration event is 16 uC. The average current consumed by the calibration depends on the calibration interval and can be calculated using the following formula: **CAL_charge/CAL_interval –** The lowest calibration interval (0.25 seconds) provides an average current of (DC-DC enabled): **16uC/0.25s = 64uA** To get the 500-ppm accuracy, the BLE stack specification states that a calibration interval of eight seconds is enough. This gives an average current of: **16uC/8s = 2 uA** Added to the LFRC run current and Standby Doze (IDLE) base current shown above results in a total average current of: **LFRC + CAL = 3.1 + 2 = 5.1 uA**	Not applicable
Total	5.1 uA	2.6 uA
Summary	▪ Low current consumption ▪ Accuracy 500 ppm	▪ Lowest current consumption ▪ Needs external crystal ▪ High accuracy (depends on the crystal, usually 20 ppm)

5 Hardware Integration Suggestions

5.1 Circuit

The Pinnacle™ 100 is easy to integrate, requiring no external components on your board apart from those which you require for development and in your end application.

The following are suggestions for your design for the best performance and functionality.

Checklist (for Schematic):

- **Pinnacle™ 100 power supply:**
  Provide 2.2 -5.5 V to M2 Pins 2, 4, 72,74 with a power supply that can supply up to 1A @ 2.2V.
- **AIN (ADC) and SIO pin IO voltage levels**
  Pinnacle™ 100 SIO voltage levels are at 1.8V. Ensure input voltage levels into SIO pins are at 1.8V.

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- **AIN (ADC) impedance and external voltage divider setup**
  If you need to measure with ADC a voltage higher than 1.8V, you can connect a high impedance voltage divider to lower the voltage to the ADC input pin.
- **SWD**
  This is interface is used to load firmware.
  Laird Connectivity recommends you use SWD (2-wire interface) to handle future Pinnacle™ 100 modem firmware upgrades. You MUST wire out the SWD(2-wire interface) on your host design (see *Figure 6*, where four lines should be wired out, namely SWDIO, SWDCLK, GND and VCC).
- **UART**
  Required for modem communication and HL7800 communication.
- **UART_RX and UART_CTS**
  SIO_08 (alternative function UART_RX) is an input, set with internal weak pull-up (in firmware). The pull-up prevents the modem from going into deep sleep when UART_RX line is idling.
  SIO_07 (alternative function UART_CTS) is an input, set with internal weak pull-down (in firmware). This pull-down ensures the default state of the UART_CTS will be asserted which means can send data out of the UART_TX line. Laird Connectivity recommends that UART_CTS be connected.
- **nAutoRUN pin and operating mode selection (Hosted Mode Only)**
  nAutoRUN pin needs to be externally held high or low to select between the two Pinnacle™ 100 operating modes at power-up:
  - Self-contained Run mode (nAutoRUN pin held at 0V).
  - Interactive/development mode (nAutoRUN pin held at 1.8V).
    Make provision to allow operation in the required mode. Add jumper to allow nAutoRUN pin to be held high or low (Pinnacle™ 100 has internal 13K pull-down by default) OR driven by host GPIO.
- **I2C**
  It is essential to remember that pull-up resistors on both I2C_SCL and I2C_SDA lines are not provided in the Pinnacle™ 100 modem and MUST be provided external to the modem as per I2C standard.
- **SPI**
  Implement SPI chip select using any unused SIO pin within your application then SPI_CS is controlled from the software application allowing multi-dropping.
- **SIO pin direction**
  Pinnacle™ 100 modems SIO pins (with default function of DIO) are mostly digital inputs (see Table 2). Remember to change the direction SIO pin if that particular pin is wired to a device that expects to be driven by the Pinnacle™ 100 SIO pin configured as an output. Also, these SIO pins have the internal pull-up or pull-down resistor-enabled by default in firmware (see Table 2). This was done to avoid floating inputs, which can cause current consumption in low power modes (e.g. StandbyDoze) to drift with time. You can disable the PULL-UP or Pull-down through their Nordic application.

Note: Internal pull-up, pull down takes current from 1.8V.

- **NFC antenna connector**
  To make use of the Laird Connectivity flexi-PCB NFC antenna, fit connector:
  - Description – FFC/FPC Connector, Right Angle, SMD/90d, Dual Contact,1.2 mm Mated Height
  - Manufacturer – Molex
  - Manufacturers Part number – 512810594

  Add tuning capacitors of 300 pF on NFC1 pin to GND and 300 pF on NFC2 pins to GND if the PCB track length is similar as development board.
- **nRESET pin (active low)**
  Hardware reset. Wire out to push button or drive by host.
  By default modem is out of reset when power applied to Vin pins.

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5.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate Pinnacle™ 100 modem M2 connector and Standoffs per the reference design. The positioning on the Intergerned Antenna host PCB must overhang the PCB edge matching the reference design (mandatory for the 453-00010 for on-board PCB trace antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All modem GND pins MUST be connected to host PCB GND.
- Place GND vias close to modem GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect the copper flood to the inner GND plane. If GND flood copper is on the bottom of the modem, then connect it with GND vias to the inner GND plane.
- Route traces to avoid noise being picked up on VIN, 1V8, VBUS supply and AIN (analogue) and SIO (digital) traces.
- 453-00010 has an integrated PCB trace antenna and its performance is sensitive to host PCB. It is critical to locate the 453-00010 on the edge of the host PCB exactly like the reference design to allow the antenna to radiate properly.
- Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
  - For best antenna performance, place the 453-00010 modem on the edge of the host PCB, preferably in the edge centers, similar to the Reference Design
  - The Pinnacle™ 100 development board has the 453-00010 modem on the edge of the board (not in the corner).
  - The 453-00010 LTE Bent Metal and BLE PCB integrated antenna is tuned to a maximum host board size of 150mm x 100mm, and a minimum host board size of 42mm x 80 mm.

Note: The Pinnacle™ 100 modem is placed on the edge, preferably edge centre of the host PCB.

5.2.1 Antenna Keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the 453-00010 PCB trace monopole antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of that degradation is entirely system dependent, meaning you will need to perform some testing with your host application.
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic).

5.3 BLE Antenna Integration

The Pinnacle™ 100 modem has been designed to operate with the following internal and external antennas (with a maximum gain of 2.0 dBi). The required antenna impedance is 50 ohms. See Table 24. External antennas improve radiation efficiency.

Table 24: External antennas for the Pinnacle™ 100

Manufacturer	Model	Laird Connectivity Part Number	Type	Connector	Peak Gain
					2400-2500 MHz
Laird Connectivity	NanoBlue	MAF94045	PCB Dipole	IPEX U.FL	2 dBi
Laird Connectivity	FlexPIFA	001-0014	Patch	U.FL	2 dBi
Laird Connectivity	Dipole	001-0001		RP-SMA	2 dBi

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Note: The OEM is free to choose another vendor's antenna of like type and equal or lesser gain as an antenna appearing in the table and still maintain compliance. Reference FCC Part 15.204(c)(4) for further information on this topic.

To reduce potential radio interference to other users, the antenna type and gain should be chosen so that the equivalent isotropic radiated power (EIRP) is not more than that permitted for successful communication.

5.4 LTE Antenna Integration

The Pinnacle™ 100 family has been designed to operate with the below internal and external antennas (with a maximum gain of 3.7 dBi). The required antenna impedance is 50 ohms. See Table 24. External antennas improve radiation efficiency.

Table 25: External antennas for the Pinnacle™ 100

Manufacturer	Model	Laird Connectivity Part Number	Type	Connector	Peak Gain	
					698-875 MHz	1710-2500 MHz
Laird Connectivity	Revie Flex	EFF6925A3S-15MHF1	PCB Dipole	IPEX U.FL	1.9 dBi	3.7 dBi
Laird Connectivity	Dipole Blade	DBA6927C1-FSMAM	Dipole	SMA	0.5 dBi	2.2 dBi
Laird Connectivity	Pinnacle™ 100 Bent Metal	110-00665	Bent Metal	N/A	1.3 dBi	2.6 dBi

Note: Laird Connectivity is the manufacturer for the antennas listed below.

Model	Man. PN	Type	Conn.	Peak Gain											
				600-698	698-806	806-894	880-960	1350-1580	1550-1610	1690-1880	1850-1990	1910-2180	2300-2700	3300-4200	4900-6000
Revie Flex 600	EFF6060A3S-10MHF1	PCB Dipole	IPEX U.FL	2.0	2.5	2.7	3.2	3.8	3.8	3.7	2.8	2.9	3.8	4.7	6.9

Model	Man. PN	Type	Conn.	Peak Gain											
				698-824	824-894	880-960	1350-1550	1550-1690	1690-1880	1850-1990	1910-2170	2300-2500	2500-2700	3300-4200	4900-6000
Revie Flex 700	EFF6989A3S-19MHF1	PCB Dipole	IPEX U.FL	0.9	1.4	2.7	3.2	4.2	4.1	3.7	3.9	3.7	3.5	3.3	4.5

Note: The OEM is free to choose another vendor's antenna of like type and equal or lesser gain as an antenna appearing in the table and still maintain compliance. Reference FCC Part 15.204(c)(4) for further information on this topic.

To reduce potential radio interference to other users, the antenna type and gain should be chosen so that the equivalent isotropic radiated power (EIRP) is not more than that permitted for successful communication.

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6 MECHANICAL DETAILS

6.1 Pinnacle™ 100 Mechanical Details

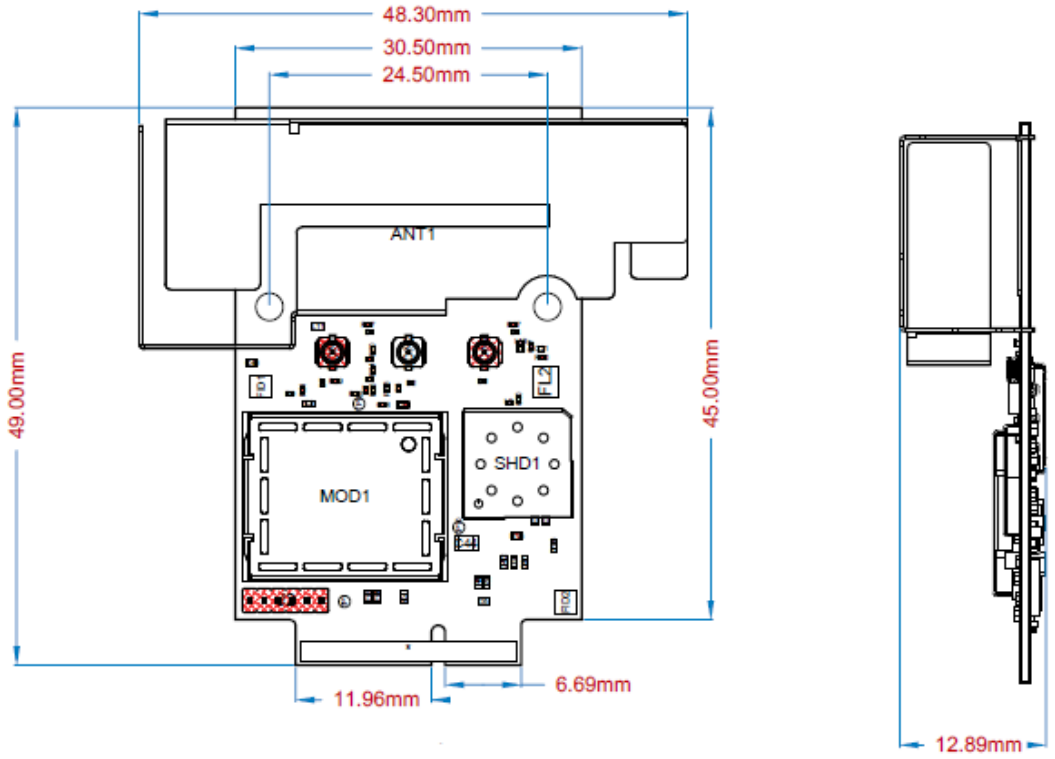

Figure 7: Pinnacle™ 100 453-00010 mechanical drawings

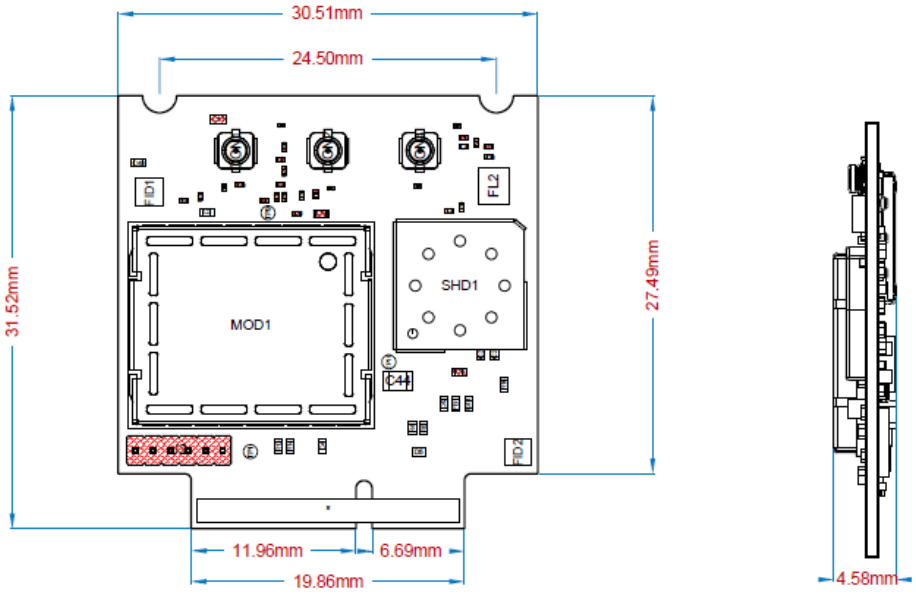

Figure 8: Pinnacle™ 100 453-00011 mechanical drawings

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6.2 PCI Express M2 Connector and Standoffs

The Pinnacle™ 100 modem is connected to a host board using an TE Connectivity 2199230-4, 67 Position Female M.2 connector. The Pinnacle™ 100 uses a custom pin out and does not follow the M2 standard pin out. The modem also requires two PEM threaded standoffs and two screws to hold the modem. A PCB footprint is providing the reference dimension of the connector to stand-off distances, as well as, the distance from PCB board edge.

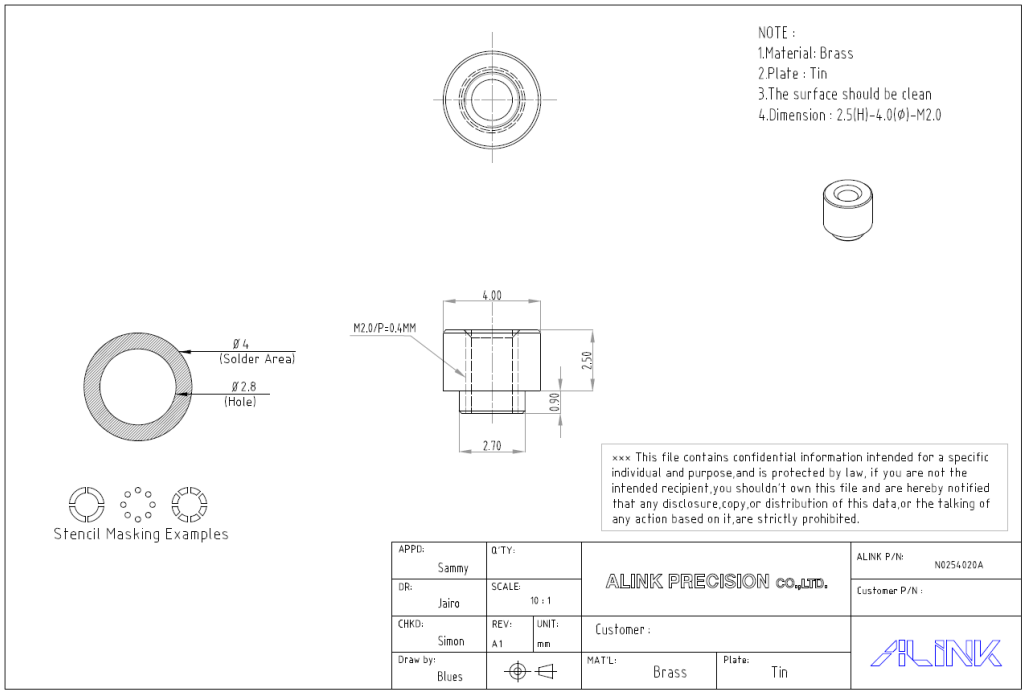
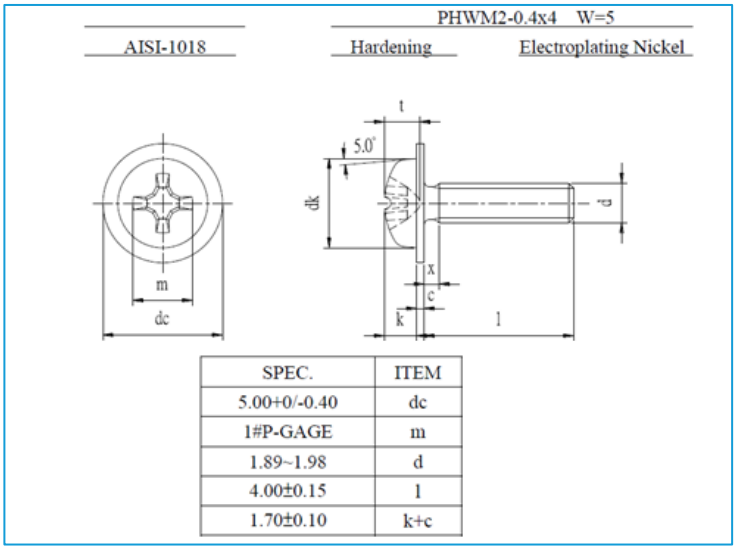


Figure 9: PEM Threaded Standoff mechanical drawings

6.3 Mounting Screw



SPEC.	ITEM
5.00+0/-0.40	dc
1#P-GAGE	m
1.89~1.98	d
4.00±0.15	l
1.70±0.10	k+c

Figure 10: Mounting Screw mechanical drawing

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6.4 Shipping

All modems are shipped in trays and sealed in ESD Bags.

453-00010T ship a quantity of 25 per tray.

453-00011T ship a quantity of 50 per tray.

6.4.1 Tray Dimensions

453-00010T:

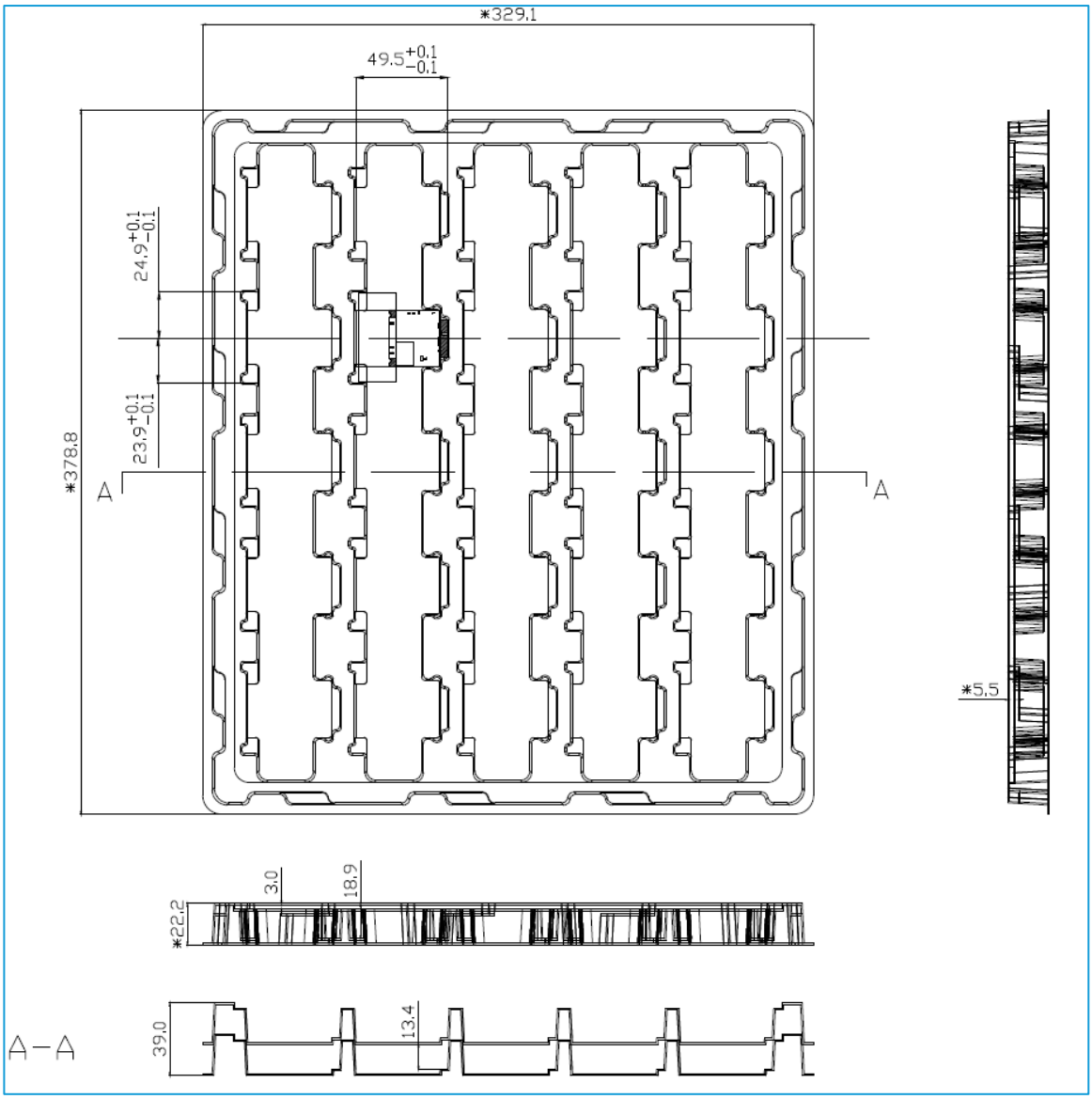

Figure 11: 453-00010 modem tray (mm) 25 per tray

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453-00011T:

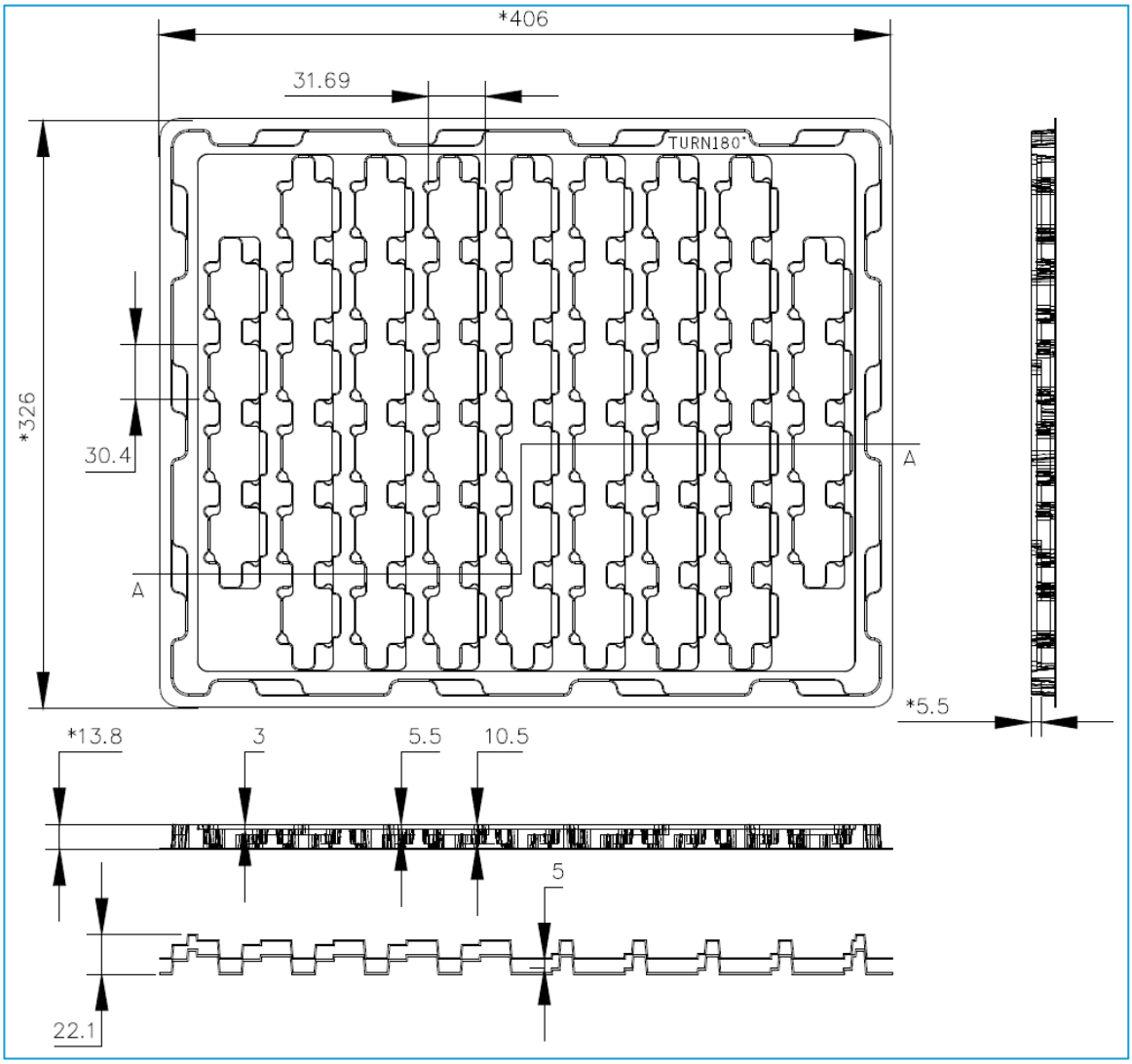

Figure 12: 453-00011 modem tray (mm) 50 per tray

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6.5 Modem Labeling

6.5.1 453-00010

Initial Release (Rev 4)

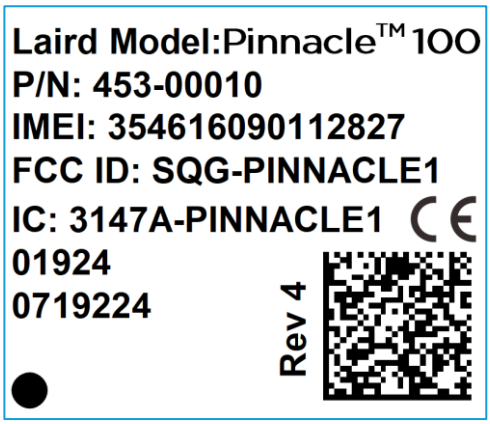

Figure 13: 453-00010 modem label

6.5.2 453-00011

Initial Release (Rev 4)

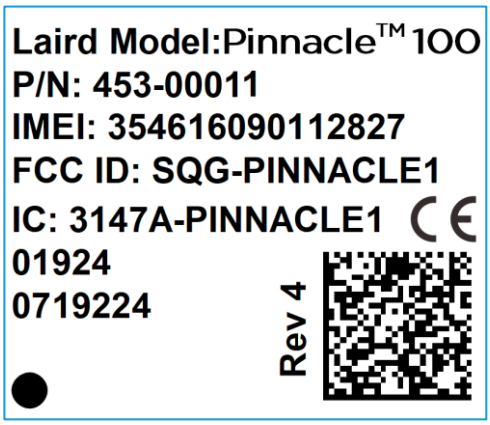

Figure 14: 453-00011 modem label

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7 REGULATORY

Note: For complete regulatory information, refer to the Pinnacle 100 Regulatory Information document which is also available from the Pinnacle 100 product page.

The Pinnacle™ 100 (453-00010/453-00011) holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-PINNACLE1
Canada (ISED)	3147A-PINNACLE1
EU	N/A

8 ORDERING INFORMATION

Table 26: Order Info

Part Number	Product Description
453-00010	LTE/Bluetooth v5/NFC modem – Integrated antenna LTE & BLE
453-00011	LTE/Bluetooth v5/NFC modem – External antenna
453-00010-K1	Development Kit for 453-00010 modem – Integrated antenna
453-00011-K1	Development Kit for 453-00011 modem – External antenna

9 BLUETOOTH SIG QUALIFICATION

9.1 Overview

The Pinnacle™ 100 modem is listed on the Bluetooth SIG website as a qualified End Product.

Table 27: BLE SIG

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
Pinnacle™ 100	Laird Connectivity	D046329	145483	https://launchstudio.bluetooth.com/ListingDetails/102649

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to registered as a member of the Bluetooth SIG – www.bluetooth.org

The following link provides a link to the Bluetooth Registration page: https://www.bluetooth.org/login/register/

For each Bluetooth Design, it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document:

https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

9.2 Qualification Steps When Referencing a Laird Connectivity End Product Design

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To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

To start the new Design listing select 'Start the Bluetooth Qualification Process with **No Required Testing**"

In step 1, select the option, **Reference a Qualified Design** with the link above and enter D046329 in the End Product table entry. You can then select your pre-paid Declaration ID from the drop-down menu or go to the Purchase Declaration ID page. Please note that unless the Declaration ID is pre-paid or purchased with a credit card, it will not be possible to proceed until the SIG invoice is paid.

Once all the relevant sections of step 1 are finished, complete steps 2, 3, and 4 as described in the help document. Your new Design will be listed on the SIG website and you can print your Certificate and Declaration of Conformity.

For further information, please refer to the following training material:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

9.3 Qualification Steps When Deviating from a Laird Connectivity End Product Design

If you wish to deviate from the standard End Product design listed under D046329, the qualification process follows the Traditional Project route, creating a new design. When creating a new design, it is necessary to complete the full qualification listing process and also maintain a compliance folder for the new design.

The Pinnacle™ 100 design under D046329 incorporates the following components:

Listing reference	Design Name	Core Spec Version
D046329	Controller – Pinnacle 100	5.1
D047806	Host Subsystem – Zephyr 1.14	5.1
D047833	Profile Subsystem	N/A

If your design is based on un-modified Pinnacle™ 100 hardware it is possible use the following process;

1. Reference the existing RF-PHY test report from the Pinnacle™ 100 listing.
2. Combine the relevant Nordic Link Layer (LL) – check QDID with Nordic.
3. Combine in a Host Component (covering L2CAP, GAP, ATT, GATT, SM) - check QDID with Nordic.
4. Test any standard SIG profiles that are supported in the design (customs profiles are exempt).

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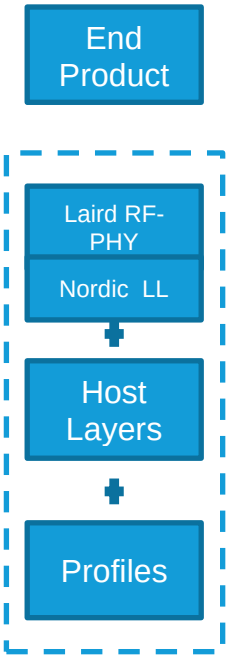

Figure 15: Scope of the qualification for an end product design

When creating a new design, you must chose “Start the Bluetooth Qualification Process with **Required Testing**”

The first step is to generate a project on the TPG (Test Plan Generator) system. This determines which test cases apply to demonstrate compliance with the Bluetooth Test Specifications. If you are combining pre-tested and qualified components in your design and they are within their three-year listing period, you are not required to re-test those layers covered by these components.

If the design incorporates any standard SIG LE profiles (such as Heart Rate Profile), it is necessary to test these profiles using PTS or other tools where permitted; the results are added to the compliance folder.

You are required to upload your test declaration and test reports (where applicable) and then complete the final listing steps on the SIG website. Remember to purchase your Declaration ID before you start the qualification process, as it’s impossible to complete the listing without it.

10 PTCRB

Pinnacle 100 Modem – Integrated Antenna (453-00010)

https://www.ptcrb.com/certified-devices/device-details/?model=43744

Pinnacle 100 Modem – External Antenna (453-00011)

https://www.ptcrb.com/certified-devices/device-details/?model=43743

11 Global Certification Forum (GFC)

Pinnacle 100 Modem – Integrated Antenna (453-00010)

https://www.globalcertificationforum.org/pub_product/8933.html

Pinnacle 100 Modem – External Antenna (453-00011)

https://www.globalcertificationforum.org/pub_product/8934.html

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2762 4823

12 Carrier Certification

12.1 AT&T

The following are links to AT&T carrier approval listings.

- Carrier Approval - AT&T, Pinnacle 100/453-00010 Listing
- Carrier Approval - AT&T, Pinnacle 100/453-00011 Listing

12.2 Verizon

The following are links to Verizon carrier approval listings.

- Carrier Approval - Verizon, Pinnacle 100/453-00010 Listing
- Carrier Approval - Verizon, Pinnacle 100/453-00011 Listing

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2762 4823

13 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

Laird Connectivity Products Business Unit
Support Centre: http://ews-support.lairdconnect.com
Email: wireless.support@lairdtconnect.com
Phone: Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610
Web: www.lairdconnect.com/products