Laird™
CONNECTIVITY

Datasheet

Sterling™ LWB5+

Version 3.0

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
1.0	07 Dec 2020	Initial version	Andrew Chen	Jonathan Kaye
1.1	01 Feb 2021	Updated Bluetooth v5.0 to v5.2	Sue White	Jonathan Kaye
1.2	12 Feb 2021	Fixed references to DDR50 mode	John Nosky	Dave Drogowski
2.0	21 Feb 2021	Transferred detailed regulatory information to a separate document	Sue White	Jonathan Kaye
2.1	03 Mar 2021	Added Bluetooth current consumption tables	Maggie Teng	Jonathan Kaye
2.2	18 Mar 2021	Added VBAT note to Pin Definitions table	Ferdie Brillantes	Andrew Chen
2.3	31 Mar 2021	Updated mechanical drawings	Connie Linn	Andrew Chen
2.4	21 Jun 2021	Added sleep current data	Sue White	Andrew Chen
2.5	30 Jun 2021	Updated mechanical drawing	Connie Linn	Andy Ross
2.6	11 Aug 2021	Added Peak PHY Calibration Current table (Table 18) Added Power-Up Sequence and Timing Requirements	Andrew Chen	Andy Ross
2.7	22 Dec 2021	Updated Mechanical Specifications	Dave Drogowski	Andrew Chen
2.8	2 Mar 2022	Updated Pin 34 in Pin Definitions	Dave Drogowski	Andrew Chen
2.9	21 Apr 2022	Updated ramp down specifications in 16.6.1 Soldering	Dave Drogowski	Maggie Teng
3.0	27 Oct 2022	Added note on maximum EIRP for Bluetooth in Specifications.	Dave Drogowski Connie Lin	Andy Ross

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1 SCOPE

This document describes key hardware aspects of the Laird Connectivity Sterling™ LWB5+ series wireless modules providing either SDIO or USB2.0 interface for WLAN connection and UART/PCM, USB2.0/PCM for Bluetooth® connection. This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from several sources and includes information found in the Cypress CYW4373EUBGT data sheet issued in July 2020 along with other documents provided from Cypress.

Note: **The information in this document is subject to change.** Please contact Laird Connectivity to obtain the most recent version of this document.

2 INTRODUCTION

2.1 General Description

The LWB5+ series wireless module is an integrated, small form factor 1x1 SISO 802.11 a/b/g/n/ac WLAN plus dual-mode Bluetooth® 5.2 Low Energy module that is optimized for low-power mobile devices. The integration of all WLAN and Bluetooth functionality in a single package supports low cost and simple implementation along with flexibility for platform-specific customization.

This device is pre-calibrated and integrates the complete transmit/receive RF paths including diplexer, switches, reference crystal oscillator, and power management units (PMU). The integrated ceramic chip antenna, MHF4 RF connector, and RF trace pad are selectable from different variants.

The LWB5+ series device supports IEEE 802.11ac 1x1 SISO with data rates up to MCS9 (433.3 Mbps). An internal Wi-Fi and Bluetooth coexistence scheme provides optimized connectivity while Wi-Fi and Bluetooth are working simultaneously. The device's low power consumption radio architecture and power management unit (PMU) proprietary power save technologies allow for extended battery life.

In addition, its dual 802.11ac and Bluetooth radio includes full digital MAC and baseband engines that handle all 802.11 CCK/OFDM® 2.4/5 GHz and Bluetooth 5.2 (Basic Rate, Enhanced Data Rate, and Bluetooth Low Energy) baseband and protocol processing.

The LWB5+ series wireless modules include three product SKUs which have different RF path and antenna types. Please contact Laird Connectivity Sales/FAE for further information. Ordering information is listed in Table 1.

Table 1: Product ordering information

Part Number	Description
453-00045R	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 - Integrated antenna (tape and reel)
453-00046R	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – MHF4 (tape and reel)
453-00047R	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – Trace pin (tape and reel)
453-00045C	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – Integrated antenna (cut tape)
453-00046C	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – MHF4 (cut tape)
453-00047C	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – Trace pin (cut tape)
453-00045-K1	Development kit for 1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 - Integrated antenna
453-00046-K1	Development kit for 1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – MHF4

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3 LWB5+ Series Features Summary

The Laird Connectivity LWB5+ series device features are described in Table 2.

Table 2: LWB5+ series wireless module features

Feature	Description
Radio Front End	▪ Integrates the complete transmit/receive RF paths including diplexer, switches, reference crystal oscillator, and power manage unit (PMU) ▪ Supports 20/40/80 MHz channel bandwidth ▪ WLAN/Bluetooth share one antenna
The *Bluetooth*® word mark and logos are registered trademarks owned by Bluetooth SIG, Inc. Any use of such marks by Laird Connectivity is under license. Other trademarks and trade names are those of their respective owners.	
Power Management	One buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW4373E. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.
Pre-Calibration	RF system tested and calibrated in production
Sleep Clock	An external sleep clock of 32.768 kHz is required.
Host Interface	SDIO v3.0 interface that can operate in 4b or 1b mode and a USB 2.0 interface. The Bluetooth section supports USB 2.0, USB 1.1, SDIO, and a high-speed 4-wire UART interface. An on-chip USB 2.0 hub provides a shared single USB connection to both WLAN and Bluetooth target devices.
Advanced WLAN	▪ IEEE 802.11ac compliant ▪ Support for MCS8 VHT20 in 20 MHz channels for up to 86.7 Mbps data ▪ Single-stream spatial multiplexing up to 433.3 Mbps data rate ▪ Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation) ▪ Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance ▪ TX and RX low-density parity check (LDPC) support for improved range and power efficiency ▪ On-chip power amplifiers and low-noise amplifiers for both bands ▪ Support wide variety of WLAN encryption: WEP/WPA/TKIP/WPA2 AES-CCMP
Advanced Bluetooth	▪ Qualified for Bluetooth Core Specification 5.2 with all Bluetooth 4.2 optional features – QDID: 158628 – Declaration ID: D050382 ▪ Bluetooth Class 1 or Class 2 transmitter operation ▪ Support data rate: 1 Mbps (GFSK), 2 Mbps (π/4-DQPSK), 3 Mbps (8-DPSK) ▪ Supports extended synchronous connections (eSCO) for enhanced voice quality by allowing for retransmission of dropped packets ▪ Adaptive frequency hopping (AFH) for reducing radio frequency interference ▪ Interface support, host controller interface (HCI) using a highspeed UART or USB interface, and PCM for audio data ▪ Low power consumption improves battery life of IoT and embedded devices ▪ Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound ▪ Automatic frequency detection for standard crystal and TCXO values

Strap Value CONFIG_HOST [2-0]	WLAN	Bluetooth/Bluetooth LE	Notes
000	USB	USB	USB 2.0
101	SDIO	UART	SDIO 1.8V
100	SDIO	UART	SDIO 3.3V

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4 SPECIFICATIONS

Table 3: Specifications

Feature	Description
Physical Interface	68-pin LGA package (including 17 thermal ground pads under the package)
Wi-Fi Interface	1-bit or 4-bit Secure Digital I/O; USB 2.0
Bluetooth/BLE Interface	Host Controller Interface (HCI) using high speed UART, USB 2.0
Main Chip	Cypress CYW4373EUBGT
Input Voltage Requirements	Operational: VBAT is 3.2V to 4.8V ** EVM/harmonics are improved with VBAT ≥ 3.6V
I/O Signalling Voltage	Typical DC 3.2V to 3.6V or DC 1.8 V ± 10%
Operating Temperature	-40° to +85°C (-40° to +185°F)
Operating Humidity	10 to 90% (non-condensing)
Storage Temperature	-40° to +85°C (-40° to +185°F)
Storage Humidity	10 to 90% (non-condensing)
MSL (Moisture Sensitivity Level)	4
Maximum Electrostatic Discharge	Conductive 4KV; Air coupled 8KV (follow EN61000-4-2)
Size – mm (in.)	Length: 17 (0.67) Width: 12 (0.47) Thickness: 2.13 (0.08)
Weight – g (oz.)	~0.7 (~0.02)
Wi-Fi Media	Direct Sequence-Spread Spectrum (DSSS) Complementary Code Keying (CCK) Orthogonal Frequency Divisional Multiplexing (OFDM)
Bluetooth Media	Frequency Hopping Spread Spectrum (FHSS)
Wi-Fi Multimedia	WMM Wi-Fi Multimedia - PowerSave (WMM-PS with U-APSD) WMM-Sequential Access (WMM-SA with PCF)
Network Architecture Types	Infrastructure (client operation)
Wi-Fi Standards	IEEE 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, 802.11k*, 802.11n, 802.11r, 802.11v*, 802.11ac
Bluetooth Standards	Bluetooth 5.2 Core Spec
Wi-Fi Data Rates Supported	Support 802.11 ac/a/b/g/n 1x1 SISO. 802.11b (DSSS, CCK) 1, 2, 5.5, 11 Mbps 802.11a/g (OFDM) 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n (OFDM, HT20/HT40, MCS0-7) 802.11ac (OFDM, VHT20, MCS0-8; OFDM, VHT40/HT80, MCS0-9)
Modulation Table	BPSK, QPSK, CCK, 16-QAM, 64-QAM, and 256-QAM.

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Feature				Description							
802.11ac 802.11n	HT MCS Index	VHT MCS Index	Spatial Streams	Modulation	Coding	20 MHz		40 MHz		80 MHz	
						No SGI	SGI	No SGI	SGI	No SGI	SGI
	0	0	1	BPSK	1/2	6.5	7.2	13.5	15	29.3	32.5
	1	1	1	QPSK	1/2	13	14.4	27	30	58.5	65
	2	2	1	QPSK	3/4	19.5	21.7	40.5	45	87.8	97.5
	3	3	1	16-QAM	1/2	26	28.9	54	60	117	130
	4	4	1	16-QAM	3/4	39	43.3	81	90	175.5	195
	5	5	1	64-QAM	2/3	52	57.8	108	120	234	260
	6	6	1	64-QAM	3/4	58.5	65	121.5	135	263.3	292.5
	7	7	1	64-QAM	5/6	65	72.2	135	150	292.5	325
		8	1	256-QAM	3/4	78	86.7	162	180	351	390
		9	1	256-QAM	5/6	N/A	N/A	180	200	390	**433.3**

802.11ac/n Spatial Streams	1 (1x1 SISO)
Bluetooth Data Rates Supported	1, 2, 3 Mbps
Bluetooth Modulation	GFSK@ 1 Mbps Pi/4-DQPSK@ 2 Mbps 8-DPSK@ 3 Mbps
Regulatory Certifications	United States (FCC) EU - Member countries of European Union (ETSI) ISED (Canada) Australia Japan
2.4 GHz Frequency Bands	**EU:** 2.4 GHz to 2.483 GHz **FCC/ISED:** 2.4 GHz to 2.473 GHz **MIC:** 2.4 GHz to 2.495 GHz **RCM**: 2.4 GHz to 2.483 GHz
2.4 GHz Operating Channels (Wi-Fi)	**EU:** 13 (3 non-overlapping) **FCC/ISED:** 11 (3 non-overlapping) **MIC:** 14 (4 non-overlapping) **RCM**: 13 (3 non-overlapping)
5 GHz Frequency Bands	**EU** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/132/136/140) 5.725 GHz to 5.85 GHz (Ch 149/153/157/161/165) **FCC** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/132/136/140/144 5.725 GHz to 5.85 GHz (Ch 149/153/157/161/165) **ISED** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/132/136/140/144 5.725 GHz to 5.85 GHz (Ch 149/153/157/161/165) **MIC** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/132/136/140) **RCM** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/132/136/140 5.725 GHz to 5.85 GHz (Ch 149/153/157/161/165)

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Feature	Description	
5 GHz Operating Channels (Wi-Fi)	EU: 24 non-overlapping; FCC: 25 non-overlapping ISED: 22 non-overlapping; MIC: 19 non-overlapping RCM: 21 non-overlapping	
Transmit Power ***Note:*** *Transmit power on each channel varies per individual country regulations. All values are nominal with +/-2 dBm tolerance at room temperature.* *Tolerance could be up to +/-2.5 dBm across operating temperature.* ***Note:*** *HT20 – 20 MHz-wide channels* *HT40 – 40 MHz-wide channels* *HT80 – 80 MHz-wide channels*	**802.11a**	
	6 Mbps	16 dBm (40 mW)
	54 Mbps	15 dBm (31.6 mW)
	802.11b	
	1 Mbps	16.5 dBm (44.7 mW)
	11 Mbps	16.5 dBm (44.7 mW)
	802.11g	
	6 Mbps	16 dBm (40 mW)
	54 Mbps	15.5 dBm (35.5 mW)
	802.11n (2.4 GHz)	
	HT20; MCS0-7	13.5 dBm (22.4 mW)
	HT40; MCS0-7	13.5 dBm (22.4 mW)
	802.11n (5 GHz)	
	HT20; MCS0-5	16 dBm (40 mW)
	HT20; MCS6-7	15 dBm (31.6 mW)
	HT40; MCS0-7	13 dBm (20 mW)
	802.11ac (5 GHz)	
	VHT20; MCS0-5	16 dBm (40 mW)
	VHT20; MCS6-7	15 dBm (31.6 mW)
	VHT20; MCS8	13 dBm (20 mW)
	VHT40; MCS0-7	13 dBm (20 mW)
	VHT40; MCS8-9	11 dBm (12.6 mW)
	VHT80; MCS0-7	12 dBm (15.8 mW)
	VHT80; MCS8-9	11 dBm (12.6 mW)
	Bluetooth	
	1 Mbps (1DH5)	7 dBm max (5 mW)
	2 Mbps	3 dBm max (1.99 mW)
	3 Mbps	3 dBm max (1.99 mW)
	BLE (1 Mbps)	7 dBm max (5 mW)
	Note: The EIRP of Bluetooth transmissions may not exceed 10 dBm. This includes the radio output power and the antenna gain used in combination with the radio.	

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Feature	Description	
Typical Receiver Sensitivity (PER <= 10%) ***Note:*** *All values nominal, +/-3 dBm.*	**802.11a:**	
	6 Mbps	-92 dBm
	54 Mbps	-74 dBm
	802.11b:	
	1 Mbps	-96 dBm (PER < 8%)
	11 Mbps	-90 dBm (PER < 8%)
	802.11g:	
	6 Mbps	-93 dBm
	54 Mbps	-76 dBm
	802.11n (2.4 GHz)	
	6.5 Mbps (MCS0; HT20)	-93 dBm
	65 Mbps (MCS7; HT20)	-74 dBm
	13.5 Mbps (MCS0; HT40)	-91 dBm
	135 Mbps (MCS7; HT40)	-71 dBm
	802.11n (5 GHz)	
	6.5 Mbps (MCS0; HT20)	-91 dBm
	65 Mbps (MCS7; HT20)	-73 dBm
	13.5Mbps (MCS0; HT40)	-89 dBm
	135Mbps (MCS7; HT40)	-69 dBm
	802.11ac (5 GHz)	
	6.5 Mbps (MCS0; VHT20)	-90 dBm
	78 Mbps (MCS8; VHT20)	-67 dBm
	13.5 Mbps (MCS0; VHT40)	-89 dBm
	180 Mbps (MCS9; VHT40)	-63 dBm
	29.3 Mbps (MCS0; VHT80)	-85 dBm
	390 Mbps (MCS9; VHT80)	-60 dBm
	Bluetooth:	
	1 Mbps (1DH5)	-91 dBm
	2Mbps (2DH5)	-93 dBm
	3 Mbps (3DH5)	-87 dBm
	Bluetooth LE	-94 dBm
Operating Systems Supported	Linux Android	
Security	▪ WEP ▪ WPA and WPA2 (Personal) support for powerful encryption and authentication ▪ AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility ▪ Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS). ▪ CKIP	

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Feature	Description	
Compliance	**EU** EN 300 328 EN 301 489-1 EN 301 489-17 EN 301 893 **FCC** 47 CFR FCC Part 15.247 47 CFR FCC Part 15.407 47 CFR FCC Part 2.1091 **AS/NZS** AS/NZS 4268:2017	 EN 62368-1:2014 EN 300 440 2011/65/EU (RoHS) **ISED Canada** RSS-247 **MIC** ARIB STD-T66/RCR STD-33 (2.4 GHz) ARIB STD-T71 (5 GHz)
Certifications (Pending)	***Bluetooth*® SIG Qualification**	
Warranty	One Year Warranty	
All specifications are subject to change without notice		

5 WLAN Functional Description

5.1 Overview

The LWB5+ series wireless module is designed based on the Cypress CYW4373EUBGT 802.11ac/a/b/g/n chipset. It is optimized for high speed, reliability, and low-power embedded applications. It is integrated with dual-band WLAN (2.4/5 GHz) and Bluetooth 5.2. Its functionality includes the following:

- Improved throughput on the link due to frame aggregation, RIFS (reduced inter-frame spacing), and half guard intervals.
- Support for LDPC (Low Density Parity Check) codes.
- Improved 11n performance due to features such as 11n frame aggregation (TX A-MPDU) and low-overhead host-assisted buffering (RX A-MPDU). These techniques can improve performance and efficiency of applications involving large bulk data transfers such as file transfers or high-resolution video streaming.
- IEEE 802.11ac, 1x1 SISO with data rate up to MCS9 (433.3 Mbps).

Additional functionality is listed in Table 4.

Table 4: WLAN functions

Feature	Description
WLAN MAC	▪ Enhanced MAC for supporting IEEE 802.11ac features ▪ Transmission and reception of aggregated MPDUs (A-MPDUs) for very high throughput (VHT) ▪ Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation ▪ Support for immediate ACK and Block-ACK policies ▪ Interframe space timing support, including RIFS ▪ Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges ▪ Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification ▪ Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) ▪ generation in hardware and capturing the TSF timer on an external time synchronization pulse ▪ Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management ▪ Support for coexistence with Bluetooth and other external radios ▪ Programmable independent basic service set (IBSS) or infrastructure basic service set functionality

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Feature	Description
	▪ Statistics counters for MIB support
WLAN Security	▪ WLAN Encryption features supported include: – Temporal Key Integrity Protocol (TKIP)/Wired Equivalent Privacy (WEP) – Advanced Encryption Standard (AES)/Counter-Mode/CBC-MAC Protocol (CCMP) – WLAN Authentication and Private Infrastructure (WPAI)
WLAN Channel	Channel frequency supported.

20 MHz		40 MHz		80 MHz			
Channel	**Freq. (MHz)**	**Channel**	**Freq. (MHz)**	**Channel**	**Freq. (MHz)**	**Channel**	**Freq. (MHz)**
1	2412	36	5180	1-5	2422	42	5210
2	2417	40	5200	2-6	2427	58	5290
3	2422	44	5220	3-7	2432	74	5370
4	2427	48	5240	4-8	2437	90	5410
5	2432	52	5260	5-9	2422	106	5530
6	2437	56	5280	6-10	2447	122	5610
7	2422	60	5300	7-11	2452	138	5690
8	2447	64	5320	36-40	5190	155	5775
9	2452	100	5500	44-48	5230		
10	2457	104	5520	52-56	5270		
11	2462	108	5540	60-64	5310		
12	2467	112	5560	68-72	5350		
13	2472	116	5580	76-80	5390		
		120	5600	84-88	5430		
		124	5620	92-96	5470		
		128	5640	100-104	5510		
		132	5660	108-112	5550		
		136	5680	116-120	5590		
		140	5700	124-128	5630		
		144	5720	132-136	5670		
		149	5745	140-144	5710		
		153	5765	149-153	5755		
		157	5785	157-161	5795		
		161	5805				
▪		165	5825				

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6 Bluetooth Functional Description

The LWB5+ series wireless module includes a fully integrated Bluetooth baseband/radio. Several features and functions are listed in Table 5.

Table 5: Bluetooth functions

Feature	Description
Bluetooth Interface	▪ Voice interface: – Hardware support for continual PCM data transmission/reception without processor overhead. – Standard PCM clock rates from 64 kHz to 2.048 MHz with multi-slot handshake and synchronization. – A-law, U-law, and linear voice PCM encoding/decoding. ▪ High-Speed UART interface ▪ USB 2.0
Bluetooth Core functionality	▪ Bluetooth 5.2 ▪ Bluetooth Class 2/Bluetooth class 1 ▪ WLAN and Bluetooth share same LNA and antenna ▪ Digital audio interfaces with TDM interface for voice application ▪ Baseband and radio BDR and EDR package type: 1 Mbps, 2 Mbps, 3 Mbps ▪ Fully functional Bluetooth baseband: AFH, forward error correction, header error control, access code correction, CRC, encryption bit stream generation, and whitening. ▪ Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER) ▪ Interlaced scan for faster connection setup ▪ Simultaneous active ACL connection setup ▪ Automatic ACL package type selection ▪ Full master and slave piconet support ▪ Scatter net support ▪ SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement ▪ All standard SCO/eSCO voice coding ▪ All standard pairing, authentication, link key, and encryption operations ▪ Encryption (AES) support
Bluetooth Low Energy (BLE) Core functionality	▪ Bluetooth 5.2 Core Spec ▪ Bluetooth 4.2 features: ○ LE privacy 1.2 ○ LE Secure Connection ○ LE Data Length Extension ▪ Bluetooth 4.0 features: ○ Advertiser, scanner, initiator, master, and slave roles support (connects to 16 links) ○ WLAN/Bluetooth coexistence (BCA) protocol support. ○ Shared RF with BDR/EDR ○ Encryption (AES) support ○ Intelligent Adaptive Frequency Hopping (AFH)

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7 Block Diagram

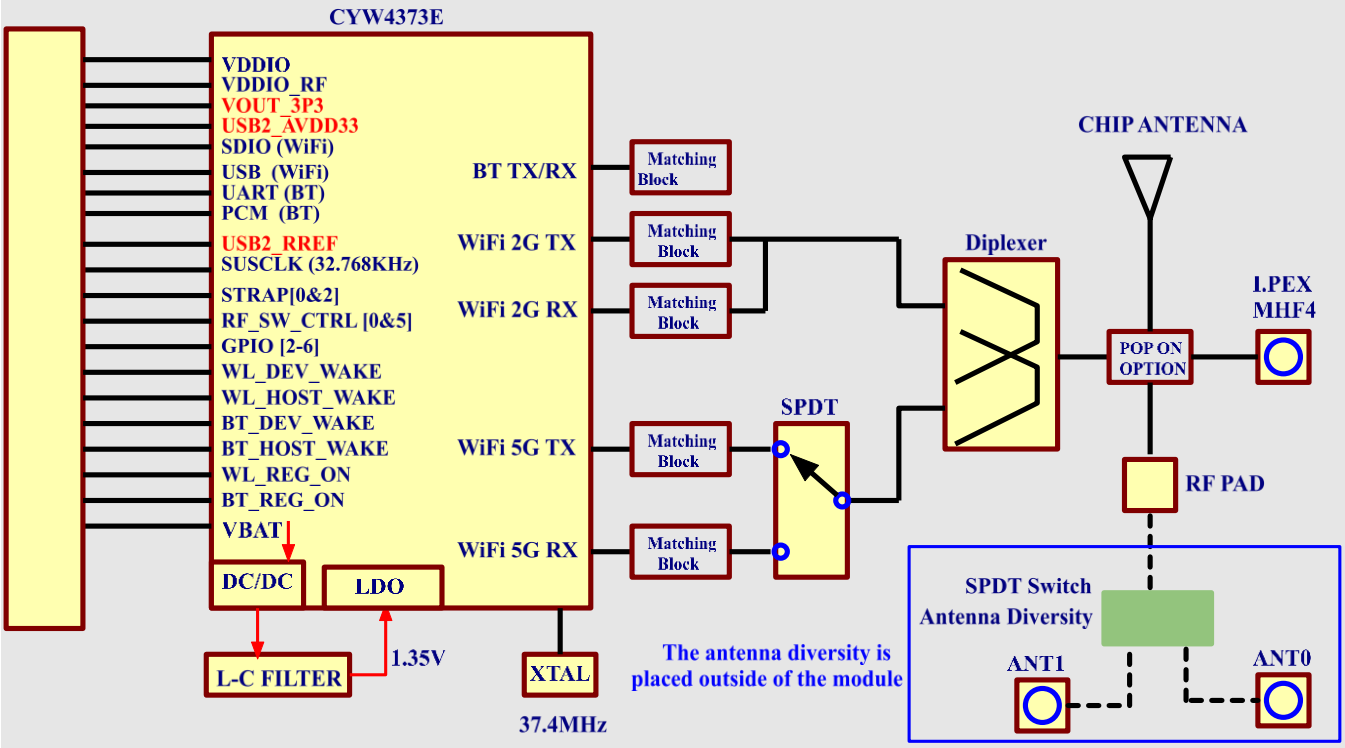

Figure 1: Block diagram

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 6 summarizes the absolute maximum ratings and Table 7 lists the recommended operating conditions for the LWB5+ series wireless module. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 6: Absolute maximum ratings

Symbol (Domain)	Parameter	Max Rating	Unit
VDDIO	WLAN host SDIO interface I/O supply (for 1.8V system) (for 3.3V system)	2.2 4.0	V
VDDIO_RF	I/O configuration power supply (for 3.3V system)	4.0	V
VBAT	External DC power supply	5.0	V
Storage	Storage temperature	-40 to +85	°C
Antenna	Maximum RF input (reference to 50-Ω input)	+10	dBm
ESD	Electrostatic discharge tolerance	2000	V

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8.2 Recommended Operating Conditions

Table 7: Recommended operating conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VDDIO	WLAN and Bluetooth host interface I/O supply	1.62/2.97	1.8/3.3	1.98/3.63	V
VDDIO_RF	I/O supply for the RF switch control pads	3.2	3.3	3.63	V
VBAT	External DC power supply	3.2	3.30	3.63	V
	EVM/harmonics are improved	3.6	—	4.8	V
T-ambient	Ambient temperature	-40	25	85	°C

8.3 DC Electrical Characteristics

Table 8 and Table 9 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 8: General DC electrical characteristics (For 1.8V operation VDDIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High Level Input Voltage	—	1.17	—	—	V
VIL	Low Level Input Voltage	—	—	—	0.63	V
VOH	Output high Voltage	—	1.35	—	—	V
VOL	Output low Voltage	—	—	—	0.45	V

Table 9: General DC electrical characteristics (For 3.3V operation VIO_SD; VIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High Level Input Voltage	—	2.0	—	—	V
VIL	Low Level Input Voltage	—	—	—	0.8	V
VOH	Output high Voltage	—	2.9	—	—	V
VOL	Output low Voltage	—	—	—	0.4	V

8.4 WLAN Radio Receiver Characteristics

Table 10 and Table 11 summarize the LWB5+ series wireless module receiver characteristics.

Table 10: WLAN receiver characteristics for 2.4 GHz single chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Frx	Receive input frequency range	—	2.412	—	2.484	GHz
Srf	Sensitivity					
	CCK, 1 Mbps	See Note[1]	—	-95	—	dBm
	CCK, 11 Mbps		—	-90	—	
	OFDM, 6 Mbps		—	-92	—	
	OFDM, 54 Mbps		—	-75	—	
	HT20, MCS0		—	-91	—	
	HT20, MCS7		—	-73	—	
	HT40, MCS0		—	-90	—	
	HT40, MCS7		—	-71	—	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Radj	Adjacent channel rejection					
	OFDM, 6 Mbps	See Note[1]	16	38	—	dB
	OFDM, 54 Mbps		-1	20.4	—	
	HT20, MCS0		16	33.3	—	
	HT20, MCS7		-2	13.7	—	

Table 11: WLAN receiver characteristics for 5 GHz single chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Frx	Receive input frequency range	—	5.15	—	5.825	GHz
Srf	Sensitivity					
	OFDM, 6 Mbps	See Note[1]	—	-92	—	dBm
	OFDM, 54 Mbps		—	-74	—	
	HT20, MCS0		—	-91	—	
	HT20, MCS7		—	-73	—	
	HT40, MCS0		—	-89	—	
	HT40, MCS7		—	-69	—	
	VHT20, MCS0		—	-90	—	
	VHT20, MCS8		—	-67	—	
	VHT40, MCS0		—	-89	—	
	VHT40, MCS9		—	-63	—	
	VHT80, MCS0		—	-85	—	
	VHT80, MCS9		—	-60	—	
Radj [Difference between interfering and desired signal (20 MHz apart)]	Adjacent channel rejection					
	OFDM, 6 Mbps	See Note[1]	16	31.7	—	dB
	OFDM, 54 Mbps		-1	13.8	—	
	OFDM, 65 Mbps		-2	8.4	—	
Radj. [Difference between interfering and desired sinal (40 MHz apart)]	OFDM, 6 Mbps	See Note[1]	32	44.7	—	dB
	OFDM, 54 Mbps		15	26.6	—	
	OFDM, 65 Mbps		14	26.8	—	

Note[1]: Performance data are measured under signal chain operation.

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8.5 WLAN Transmitter Characteristics

Table 12: WLAN transmitter characteristics for 2.4 GHz operation (SDIO=VDIO=3.3V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ftx	Transmit output frequency range	—	2.402	—	2.484	GHz
Pout	Output power	See Note[2]	—	—	—	—
	11b mask compliant	1-11Mbps	—	18	—	dBm
	11g mask compliant	6-36Mbps	—	18	—	
	11g EVM compliant	48-54Mbps	—	18	—	
	11n HT20 mask compliant	MCS0-6	—	18	—	
	11n HT20 EVM compliant	MCS7	—	17.5	—	
	11n HT40 mask compliant	MCS0-5	—	18	—	
	11n HT40 EVM compliant	MCS6-7	—	16.5	—	
ATx	Transmit power accuracy at 25 ℃	—	-2.0	—	+2.0	dB

Table 13: WLAN current consumption on 2.4 GHz (SDIO=VDIO=3.3V)

Freq.	Mode/Rate (Mbps)	Output Power (dBm)	Maximum Current Consumption (mA)[8]
2412 MHz	1 Mbps	18 dBm	369
	54 Mbps	18 dBm	365
2422 MHz	HT20 MCS7	17.5 dBm	351
	HT40 MCS7	16.5 dBm	342
2442 MHz	1 Mbps	18 dBm	369
	54 Mbps	17 dBm	365
	HT20 MCS7	17 dBm	351
	HT40 MCS7	16 dBm	342
2472 MHz	1 Mbps	18 dBm	369
	54 Mbps	17 dBm	365
2462 MHz	HT20 MCS7	17 dBm	351
	HT40 MCS7	16 dBm	342

Table 14: 2 GHz WLAN sleep mode current

Mode	^{V}BAT = 3.6V, V_{DDIO} = 1.8V, T_A = 25°C	
	^{V}BAT, mA	V_{IO}, uA[1]
Sleep Modes (SDIO Interface)		
OFF[2]	0.003	0.15
Sleep[3]	0.03	200
Sleep Modes (USB Interface)		
OFF[2]	0.003	0.057
Sleep[3]	0.49	230

[1] VIO is specified with all pins idle (not switching) and not driving any loads.
[2] WL_REG_ON and BT_REG_ON are both low. All supplies present.
[3] Idle, not associated, or inter-beacon.

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Table 15: WLAN transmitter characteristics for 5 GHz operation (SDIO=VDDIO=3.3V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ftx	Transmit output frequency range	—	5.15	—	5.925	GHz
Pout	Output power	See Note[2]	—	—	—	—
	11a mask compliant	6-36Mbps	—	17.5	—	dBm
	11a EVM compliant	48-54Mbps	—	17.5	—	
	11n HT20 mask compliant	MCS0-5	—	17.5	—	
	11n HT20 EVM compliant	MCS6-7	—	16.5	—	
	11n HT40 mask compliant	MCS0-5	—	17.5	—	
	11n HT40 EVM compliant	MCS6-7	—	16	—	
	11ac VHT20 mask compliant	MCS0-5	—	17.5	—	
	11ac VHT20 EVM compliant	MCS6-8	—	15	—	
	11ac VHT40 mask compliant	MCS0-5	—	17.5	—	
	11ac VHT40 EVM compliant	MCS6-7	—	16	—	
	11ac VHT40 EVM compliant	MCS8-9	—	13.5	—	
	11ac VHT80 mask compliant	MCS0-5	—	17.5	—	
	11ac VHT80 EVM compliant	MCS6-7	—	16	—	
	11ac VHT80 EVM compliant	MCS8-9	—	13.5	—	
ATx	Transmit power accuracy at 25 ℃	—	-2.0	—	+2.0	dB

Table 16: 5 GHz WLAN sleep mode current

Mode	^{V}BAT = 3.6V, V_{DDIO} = 1.8V, T_A = 25°C	
	^{V}BAT, mA	V_{IO}, µA[1]
Sleep Modes (SDIO Interface)		
OFF[2]	0.003	0.15
Sleep[3]	0.03	200
Sleep Modes (USB Interface)		
OFF[2]	0.003	0.057
Sleep[3]	0.49	230

[1] VIO is specified with all pins idle (not switching) and not driving any loads.
[2] WL_REG_ON and BT_REG_ON are both low. All supplies present.
[3] Idle, not associated, or inter-beacon.

Table 17: WLAN current consumption on 5 GHz (SDIO=VDDIO=3.3V)

Frequency (MHz)	Mode/Rate (Mbps)	Output Power (dBm)	Maximum Current Consumption (mA)
5180	6 Mbps	17.5	370
	54 Mbps	17.5	354
	HT20 MCS0	17.5	372
	HT20 MCS7	16.5	350
5190	HT40 MCS0	17.5	410
	HT40 MCS7	16	377
5210	VHT80 MCS0	17.5	441

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Frequency (MHz)	Mode/Rate (Mbps)	Output Power (dBm)	Maximum Current Consumption (mA)
	VHT80 MCS9	13.5	352
5500	6 Mbps	17.5	370
	54 Mbps	17.5	354
	HT20 MCS0	17.5	372
	HT20 MCS7	16.5	350
5510	HT40 MCS0	17.5	410
	HT40 MCS7	16	377
5530	VHT80 MCS0	17.5	441
	VHT80 MCS9	13.5	352
5825	6 Mbps	17.5	370
	54 Mbps	17.5	354
	HT20 MCS0	17.5	372
	HT20 MCS7	16.5	350
5795	HT40 MCS0	17.5	410
	HT40 MCS7	16	377
5775	VHT80 MCS0	17.5	441
	VHT80 MCS9	13.5	352

Note[2]: Final TX power values on each channel are limited by regulatory requirements

Table 18: Peak PHY Calibration Current

Mode	^{V}BAT = 3.3V V_{DDIO} = 1.8V T_A = 25°C	
	^{V}BAT, mA	^{V}IO, µA
Unassociated (2.4 GHz)	768	510
Associated (2.4 GHz)	748	560
Unassociated (5 GHz)	666	410
Associated (5 GHz)	664	390

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9 Bluetooth Radio Characteristics

Table 19 through Table 21 describe the basic rate transmitter performance, basic rate receiver performance, enhanced rate receiver performance, and current consumption conditions at 25°C.

Table 19: Basic rate transmitter performance temperature at 25°C (3.3V)

Test Parameter		Min	Typ	Max	BT Spec.	Unit
Maximum RF Output Power	GFSK	—	—	7	0 ~ +20	dBm
	π/4-DQPSK	—	3	—		
	8-DPSK	—	3	—		
Frequency Range		2.4	—	2.4835	2.4 ≤ f ≤ 2.4835	GHz
20 dB Bandwidth		—	919.5	—	≤ 1000	KHz
Δf1avg Maximum Modulation		140	155	175	140 < Δf1avg < 175	KHz
Δf2max Minimum Modulation		115	135	—	≥ 115	KHz
Δf2avg/Δf1avg		—	0.9	—	≥ 0.80	—
Initial Carrier Frequency		—	± 25	± 75	≤ ± 75	KHz
Frequency Drift (DH1 packet)		—	± 10	± 25	± 25	KHz
Frequency Drift (DH3 packet)		—	± 10	± 40	± 40	KHz
Frequency Drift (DH5 packet)		—	± 10	± 40	± 40	KHz
Drift rate		—	8	20	20	KHz/50us
Adjacent Channel Power	F ≥ ± 3 MHz	—	-50	—	< -40	dBm
	F = ± 2 MHz	—	-46	—	≤ -20	dBm
	F = ± 1 MHz	—	-15	—	N/A	dBm

Table 20: Basic rate receiver performance at (3.3V)

Test Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Sensitivity (1DH5)	BER ≤ 0.1%	—	-91	—	≤ -70	dBm
Maximum Input	BER ≤ 0.1%	—	—	-20	≥ -20	dBm
Interference Performance	Co-Channel	—	9	11	11	dB
	C/I 1 MHz adjacent channel	—	-5.5	0	0	dB
	C/I 2 MHz adjacent channel	—	-38	-30	-30	dB
	C/I ≥ 3 MHz adjacent channel	—	-46	-40	-40	dB
	C/I image channel	—	-25.5	-9	-9	dB
	C/I 1-MHz adjacent to image channel	—	-39	-20	-20	dB

Table 21: Enhanced data rate receiver performance (3.3V)

Test Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Sensitivity (BER ≤ 0.01%)	π/4-DQPSK	—	-93	—	≤ -70	dBm
	8-DPSK	—	-87	—	≤ -70	dBm
Maximum Input (BER ≤ 0.1%)	π/4-DQPSK	—	—	-20	≥ -20	dBm
	8-DPSK	—	—	-20	≥ -20	dBm
C/I Co-Channel (BER ≤ 0.1%)	π/4-DQPSK	—	10.5	13	≤ ±13	dB
	8-DPSK	—	17.5	21	≤ ±21	dB

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Test Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
C/I 1 MHz adjacent Channel	π/4-DQPSK	—	-6	0	≤ 0	dB
	8-DPSK	—	-3	5	≤5	dB
C/I 2 MHz adjacent Channel	π/4-DQPSK	—	-38.5	-30	≤ -30	dB
	8-DPSK	—	-37.5	-25	≤ -25	dB
C/I ≥ 3 MHz adjacent Channel	π/4-DQPSK	—	-47	-40	≤ -40	dB
	8-DPSK	—	-39.5	-33	≤ -33	dB
C/I image channel	π/4-DQPSK	—	-24.5	-7	≤ -7	dB
	8-DPSK	—	-17	0	≤ 0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK	—	-43	-20	≤ -20	dB
	8-DPSK	—	-37	-13	≤ -13	dB
Out-of-Band Blocking Performance (CW) BER ≤ 0.1%	30-2000MHz	—	-10	—	—	dBm
	2-2.399GHz	—	-27	—	—	dBm
	2.484-3GHz	—	-27	—	—	dBm
	3-12.75GHz	—	-10	—	—	dBm

Table 22: BLE RF Specifications (3.3V)

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	—	2402	—	2480	MHz
Rx sensitivity[3]	GFSK, 30.8% PER, 1Mbps	—	-94	—	dBm
Tx power[4]	—	—	—	7	dBm
Δf1 average	—	225	255	275	KHz
Δf2 maximum[5]	—	185	220	—	KHz
$\frac{\Delta f2\ avg}{\Delta f1\ avg}$ ratio	—	0.8	0.95	—	—

Notes

[3] Dirty Tx is Off.

[4] The Bluetooth LE TX power cannot exceed 10 dBm EIRP specification limit. The front-end losses and antenna gain/loss must be factored in so as not to exceed the limit.

[5] At least 99.9% of all Δf2 maximum frequency values recorded over 10 packets must be greater than 185 KHz.

Table 23: Bluetooth and Bluetooth LE sleep current

Operating Mode	VBAT	VDDIO	Unit
Sleep	3.9[1]	300.0	µA

[1] This sleep current consumption number and other average current consumption numbers in this table assume the UART interface for Bluetooth. Sleep current when using the USB interface is ~800 µA. Average current consumption numbers are therefore also expected to be higher when using the USB interface for Bluetooth.

Table 24: Bluetooth current consumption, VBAT=VDDIO=3.3V

Operating Mode	Tx	Rx	Unit
DH1	24.07	24.06	mA
DH3	29.23	29.03	mA
DH5	30.04	30.02	mA
2DH1	18.24	18.19	mA

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Operating Mode	Tx	Rx	Unit
2DH3	25.46	25.12	mA
2DH5	25.83	25.77	mA
3DH1	21.47	21.43	mA
3DH3	25.21	25.26	mA
3DH5	25.84	25.79	mA
LE	30.37	14.61	mA

Table 25: Bluetooth current consumption, VBAT=3.3V, VDDIO=1.8V

Operating Mode	Tx	Rx	Unit
DH1	23.62	23.57	mA
DH3	28.57	28.54	mA
DH5	29.62	29.62	mA
2DH1	17.65	17.77	mA
2DH3	24.06	24.07	mA
2DH5	25.11	25.12	mA
3DH1	20.91	20.87	mA
3DH3	24.42	24.72	mA
3DH5	25.34	25.29	mA
LE	30.04	14.19	mA

10 Host Interface Specifications

10.1 SDIO Specifications

The LWB5+ series wireless module SDIO host interface pins are powered from the VIO_SD voltage supply. The SDIO electrical specifications are identical for the 1-bit SDIO and 4-bit SDIO modes.

10.1.1 Default Speed, High-speed Modes

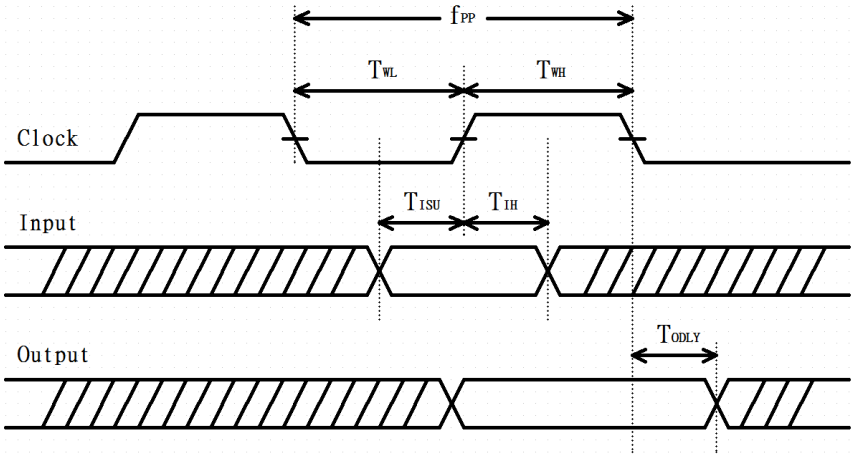

Figure 2: SDIO protocol timing diagram--- default mode (3.3V)

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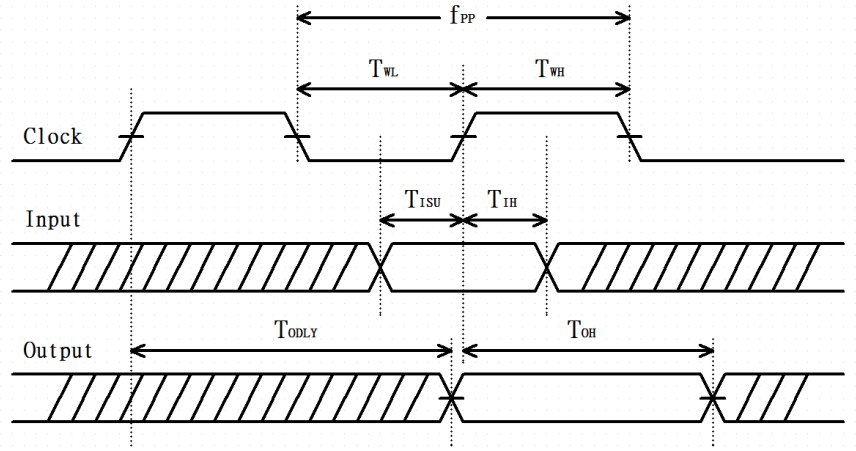

Figure 3: SDIO protocol timing diagram--- High-Speed mode (3.3V)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 26: SDIO timing requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fPP	Clock Frequency	Default Speed High-Speed	0 0	- -	25 50	MHz
TWL	Clock low time	Default Speed High-Speed	10 7	- -	- -	ns
TWH	Clock high time	Default Speed High-Speed	10 7	- -	- -	ns
TISU	Input Setup time	Default Speed High-Speed	5 6	- -	- -	ns
TIH	Input Hold time	Default Speed High-Speed	5 2	- -	- -	ns
TODLY	Output delay time CL≦40pF (1 card)	Default Speed High-Speed	- -	- -	14 14	ns
TOH	Output hold time	High-Speed	0	-	-	ns

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10.1.2 SDR12, SDR25, SDR50 Mode (up to 100 MHz) (1.8V)

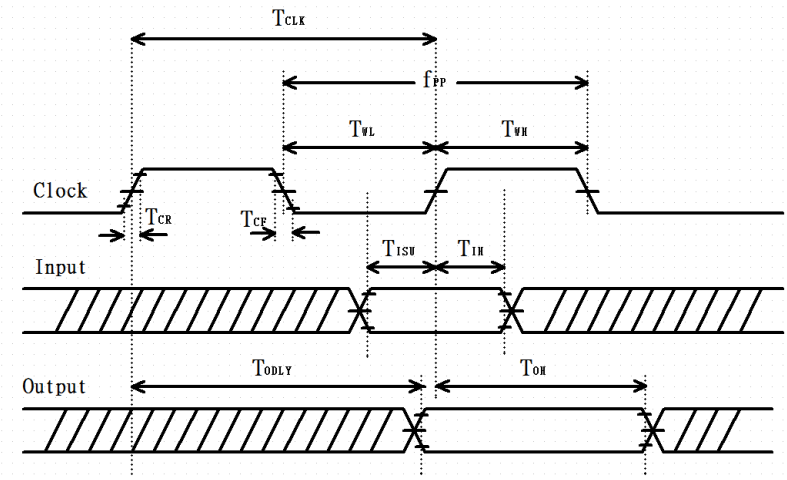

Figure 4: SDIO protocol timing diagram--- SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 27: SDIO timing requirements--- SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fPP	Clock Frequency	SDR12/25/50	25	-	100	MHz
TISU	Input setup time	SDR12/25/50	3	--	-	ns
TIH	Input Hold time	SDR12/25/50	0.8	-	-	ns
TCLK	Clock Time	SDR12/25/50	10	-	40	ns
TCR, TCF	Raise time, Fall time TCR, TCF <2ns (max) at 100MHz CCARD=10pF	SDR12/25/50	-	-	0.2*TCLK	ns
TODLY	Output delay time CL≦30pF	SDR12/25/50	-	-	7.5	ns
TOH	Output hold time CL=15pF	SDR12/25/50	1.5	-	-	ns

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10.1.3 SDR104 Mode (208 MHz) (1.8V)

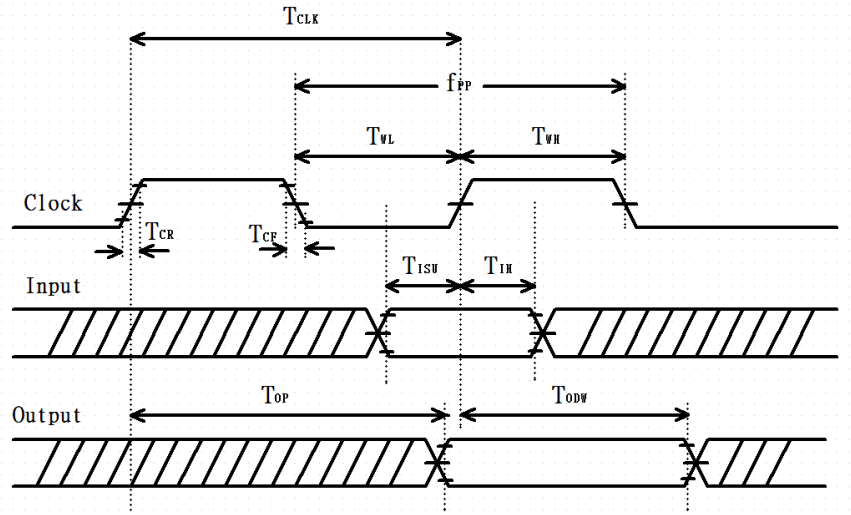

Figure 5: SDIO protocol timing diagram--- SDR104 modes (up to 208 MHz) (1.8V)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 28: SDIO timing requirements -- SDR104 modes (up to 208MHz) (1.8V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fPP	Clock Frequency	SDR104	0	-	208	MHz
TISU	Input setup time	SDR104	1.4	--	-	ns
TIH	Input Hold time	SDR104	0.8	-	-	ns
TCLK	Clock Time	SDR104	4.8	-	-	ns
TCR, TCF	Raise time, Fall time TCR, TCF <0.96ns (max) at 208MHz CCARD=10pF	SDR104	-	-	0.2*TCLK	ns
TOP	Card Output phase	SDR104	0	-	10	ns
TODW	Output timing pf variable data window	SDR12/25/SDR50	2.88	-	-	ns

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10.1.4 DDR50 Mode (50 MHz) (1.8V)

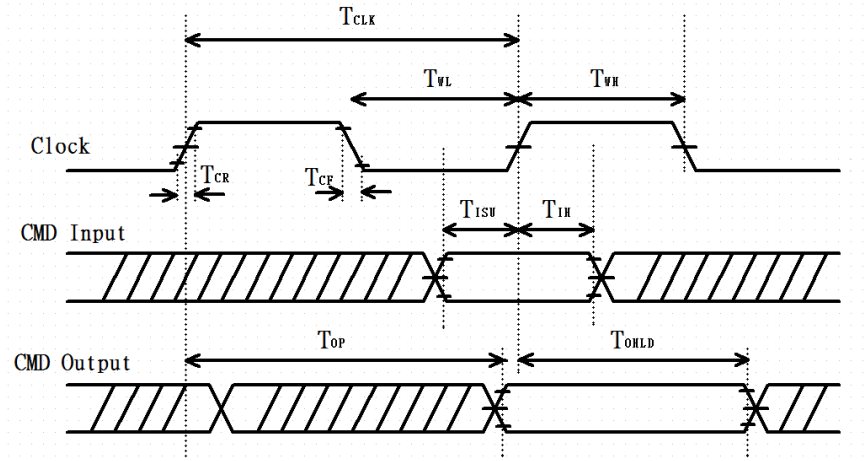

Figure 6: SDIO CMD timing diagram--- DDR50 modes (50 MHz) (1.8V)

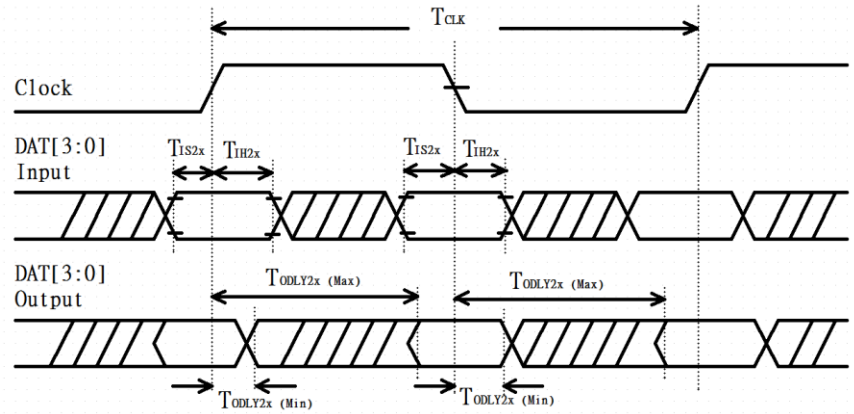

Figure 7: SDIO DAT[3:0] timing diagram--- DDR50 modes (50 MHz) (1.8V)

Note: In DDR50 mode, DAT[3:0] lines are samples on both edges of the clock (not applicable for CMD line)

Table 29: SDIO timing requirements – DDR50 modes (50 MHz)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Clock						
TCLK	Clock time 50MHz (max) between rising edge	DDR50	20	--	--	ns
TCR, TCF	Rise time, fall time TCR, TCF <4.00ns (max) at 50MHz. CCARD=10pF	DDR50	--	--	0.2*TCLK	ns
Clock Duty	--	DDR50	45	--	55	%
CMD Input (referenced to clock rising edge)						
TIS	Input setup time CCARD≦10pF (1 card)	DDR50	6	--	--	ns
TIH	Input hold time CCARD≦10pF (1 card)	DDR50	0.8	--	--	ns

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Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
CMD Output (referenced to clock rising and failing edge)						
TODLY	Output delay time during data transfer mode CL≦30pF (1 card)	DDR50	--	--	13.7	ns
TOHLD	Output hold time CL≥15pF (1 card)	DDR50	1.5	--	--	ns
DAT[3:0] Input (referenced to clock rising and failing edges)						
TIS2X	Input setup time CCARD≦10pF (1 card)	DDR50	3	--	--	ns
TIH2X	Input hold time CCARD≦10pF (1 card)	DDR50	0.8	--	--	ns
DAT[3:0] Output (referenced to clock rising and failing edges)						
TODLY2X (max)	Output delay time during data transfer mode CL≦25pF (1 card)	DDR50	--	--	7.0	ns
TODLY2X (min)	Output hold time CL≥15pF (1 card))	DDR50	1.5	--	--	ns

10.2 USB Specifications

10.2.1 USB LS Driver and Receiver Parameters

Notes: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

The load is 100Ω differential for these parameters, unless other specified.

Table 30: USB LS driver and receiver specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
BR	Baud rate	-	1.5	-	Mbps
BRPPM	Baud rate tolerance	-15000	-	15000	ppm
Driver Specifications					
VOH	Output signal ended high Defined with 1.425KΩ pull-up resistor to 3.6V	2.8	-	3.6	V
VOL	Output signal ended low Defined with 1.425KΩ pull-up resistor to ground	0.0	-	0.3	V
VCRS	Output signal crossover voltage	1.3		2.0	V
TLR	Data fall time Defined from 10% to 90% for raise time and 90% to 10% for fall time	75.0	-	300.0	ns
TLF	Data rise time Defined from 10% to 90% for raise time and 90% to 10% for fall time	75.0	-	300.0	ns
TLRFM	Rise and fall time matching	80.0	-	125.0	%

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Symbol	Parameter	Min.	Typ.	Max.	Unit
TUDJ1	Source jitter total: to next transition *Including frequency tolerance. Timing difference between the differential data signals. *Defined at crossover point of differential signals	-95	-	95	ns
TUDJ2	Source jitter total: for paired transitions *Including frequency tolerance. Timing difference between the differential data signals. *Defined at crossover point of differential signals	-150	-	150	ns
Receiver Specifications					
VIH	Input signal ended high	2.0	-	-	V
VIL	Input signal ended low	-	-	0.8	V
VDI	Differential input sensitivity	0.2	-	-	V

10.2.2 USB FS Driver and Receiver Parameters

Notes: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.
The load is 100Ω differential for these parameters, unless other specified.

Table 31: USB FS driver and receiver specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
BR	Baud rate	-	12.0	-	Mbps
BRPPM	Baud rate tolerance	-2500	-	2500	ppm
Driver Specifications					
VOH	Output signal ended high Defined with 1.425KΩ pull-up resistor to 3.6V	2.8	-	3.6	V
VOL	Output signal ended low Defined with 1.425KΩ pull-up resistor to ground	0.0	-	0.3	V
VCRS	Output signal crossover voltage	1.3		2.0	V
TFR	Output raise time Defined from 10% to 90% for raise time and 90% to 10% for fall time	-4.0	-	20.0	ns
TFL	Output fall time Defined from 10% to 90% for raise time and 90% to 10% for fall time	-4.0	-	20.0	ns
TDJ1	Source jitter total: to next transition *Including frequency tolerance. Timing difference between the differential data signals. *Defined at crossover point of differential signals	-3.5	-	3.5	ns
TDJ2	Source jitter total: for paired transitions *Including frequency tolerance. Timing difference between the differential data signals. *Defined at crossover point of differential signals	-4.0	-	4.0	ns

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Symbol	Parameter	Min.	Typ.	Max.	Unit
TFDEOP	Source jitter for differential transition to SE0 transition. Defined at crossover point of differential signals	-2.0	-	5.0	ns
Receiver Specifications					
VIH	Input signal ended high	2.0	-	-	V
VIL	Input signal ended low	-	-	0.8	V
VDI	Differential input sensitivity	0.2	-	-	V
TJR1	Receiver jitter: to next transition Defined at crossover point of differential data signals	-18.5	-	18.5	ns
TJR2	Receiver jitter: for paired transitions Defined at crossover point of differential data signals	-9.0	-	9.0	ns

10.2.3 USB HS Driver and Receiver Parameters

Notes: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.
The load is 100Ω differential for these parameters, unless other specified.

Table 32: USB HS driver and receiver specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
BR	Baud rate	-	480	-	Mbps
BRPPM	Baud rate tolerance	-500	-	500	ppm
Driver Specifications					
VHSOH	Data signal high	360	-	440	mV
VHSOL	Data signal low	-10	-	10	mV
THSR	Data rise time Defined from 10% to 90% for raise time and 90% to 10% for fall time	500	-	-	ns
THSF	Data fall time Defined from 10% to 90% for raise time and 90% to 10% for fall time	-500	-	-	ns
Receiver Specifications					
VHSCM	Input signal ended low	-50	-	500	mV

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10.3 PCM Interface Specifications

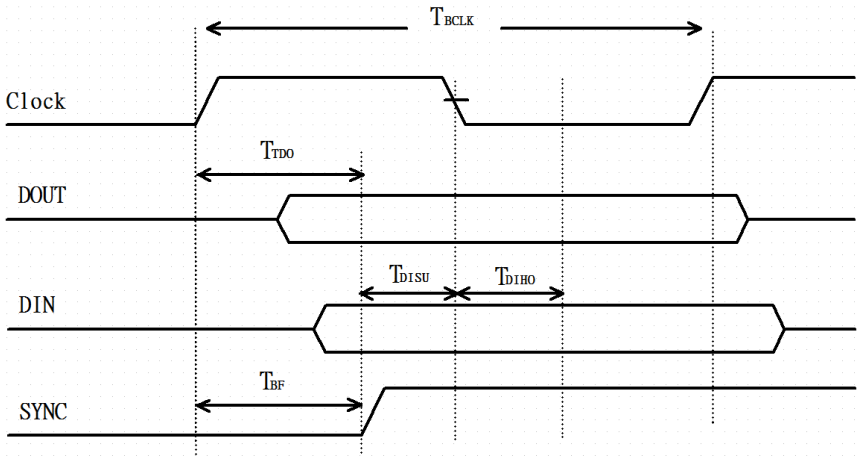

Figure 8: PCM timing specification – master mode

Table 33: PCM timing specification – master mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
FBCLK	-	-	2/2.048	-	MHz
Duty CycleBCLK	-	0.4	0.5	0.6	-
TBCLK rise/fall	-	-	3	-	ns
TDO	-	-	-	15	ns
TDISU	-	20	-	-	ns
TDIHO	-	15	-	-	ns
TBF	-	-	-	15	ns

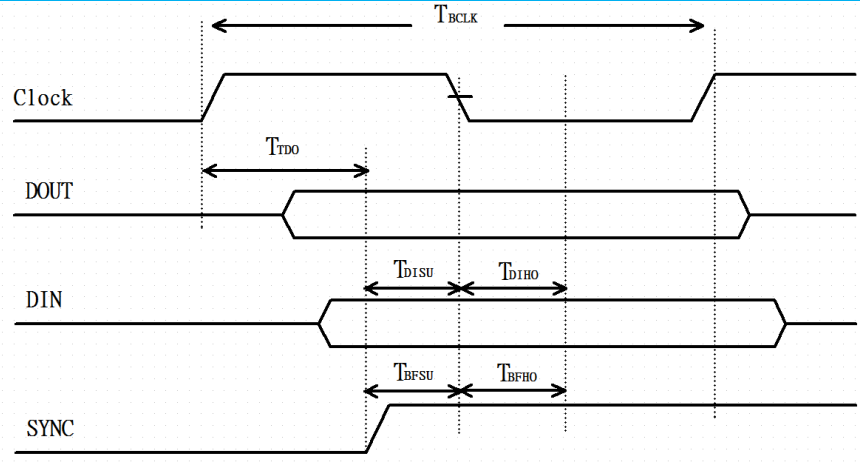

Figure 9: PCM timing specification – slave mode

Table 34: PCM timing specification – slave mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
FBCLK	-	-	2/2.048	-	MHz
Duty CycleBCLK	-	0.4	0.5	0.6	-

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Symbol	Parameter	Min.	Typ.	Max.	Unit
TBCLK rise/fall	-	-	3	-	ns
TDO	-	-	-	30	ns
TDISU	-	15	-	-	ns
TDIHO	-	10	-	-	ns
TBFSU	-	15	-	-	ns
TBFHO	-	10	-	-	ns

11 Power-Up Sequence and Timing Requirement

11.1 Description on Control Signal

- **WL_REG_ON** – Used by the PMU to power-up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- **BT_REG_ON** – Used by the PMU (OR-gated with WL_REG_ON) to power-up the internal regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Notes:

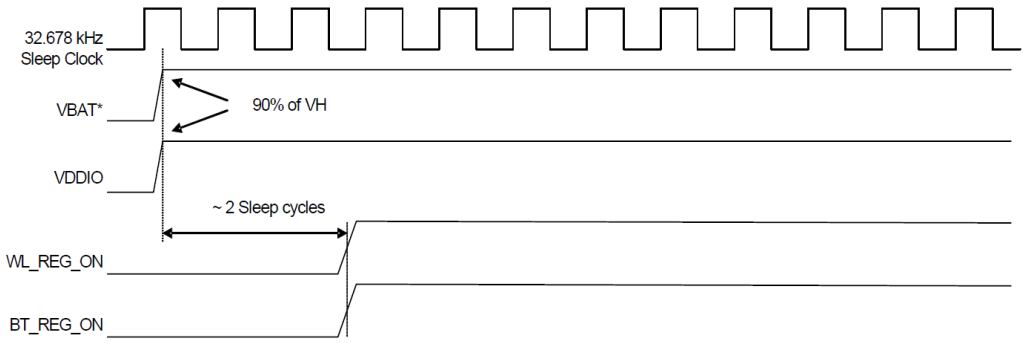
For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10-millisecond time delay between consecutive toggles (where both signals have been driven low). This allows time for the internal regulator to discharge. If this delay is not followed, there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

The CYW4373E has an internal power-on reset (POR) circuit. The device is held in reset for a maximum of 110 milliseconds after VDDC and VDDIO have passed the POR threshold. Wait at least 150 milliseconds after VDDC and VDDIO are available before initiating SDIO accesses.

VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

11.2 Control and Timing Diagrams

- **WLAN=ON; Bluetooth=ON**



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

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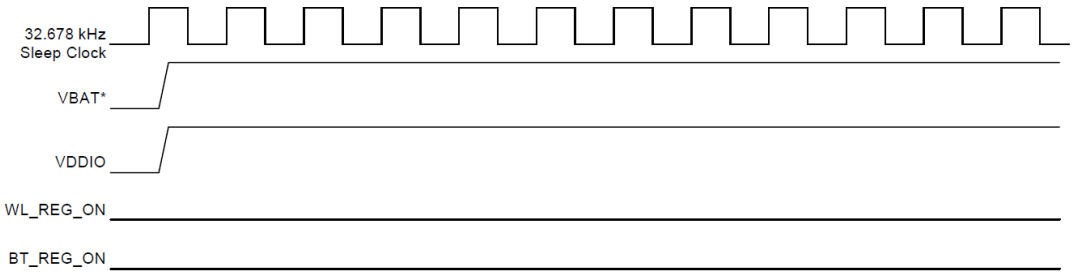
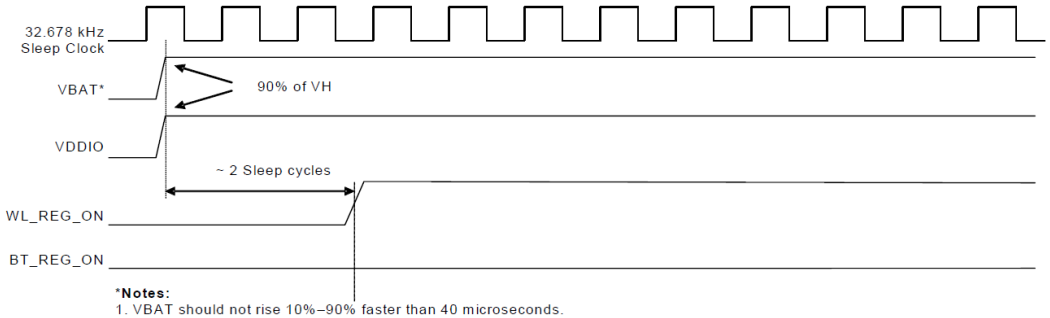
- **WLAN=OFF; Bluetooth=OFF**



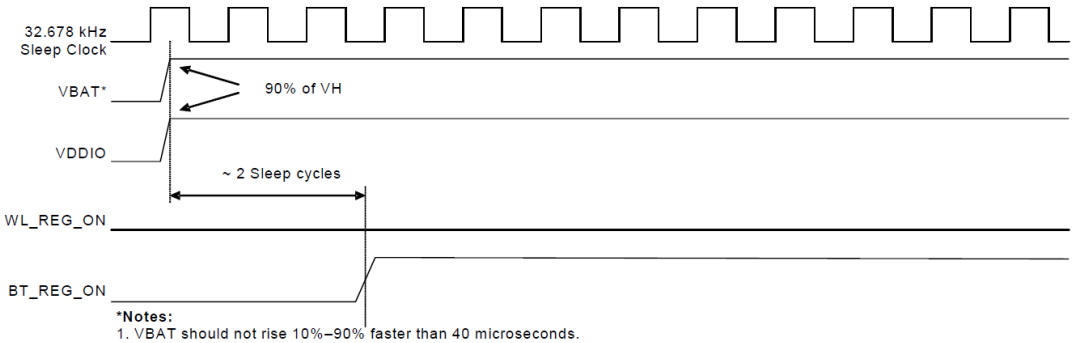
***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

- **WLAN=ON; Bluetooth=OFF**



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

- **WLAN=OFF; Bluetooth=ON**



***Notes:**
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

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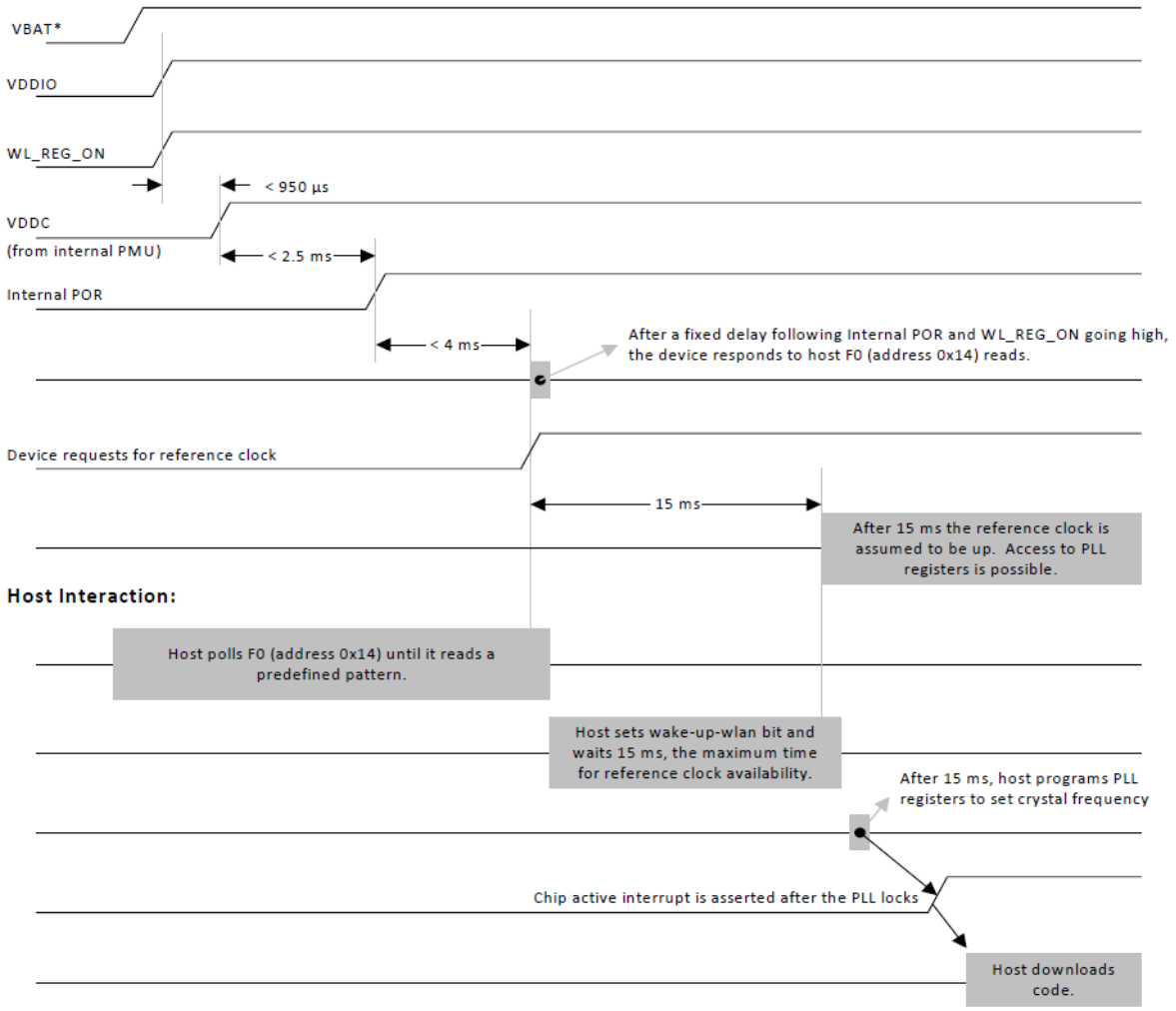
- **WLAN Boot up Sequence for SDIO Host**



***Notes:**
1. VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

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12 Pin Definitions

Table 35: Pin definitions of LWB5+ series wireless module

Pin #	Name	Type	Pins map to Chip	Voltage Ref.	Function	If Not Used
1	GND	-	-	-	Ground	GND
2	RF_SW_CTRL_5	O	F10	VDDIO _RF	RF switch control signal for Antenna diversity (only for trace pad variant)	NC
3	RF_SW_CTRL_0	O	D10	VDDIO _RF	RF switch control signal for Antenna diversity (only for trace pad variant)	NC
4	STRAP_2	I	G7	VDDIO	Strapping options to define Host interface, see Table 36	--
5	STRAP_0	I	F7	VDDIO	Strapping options to define Host interface, see Table 36	--
6	VOUT_3P3	PWR O/P	-	VOUT _3P3	Internal Regulator 3.3V output. If VBAT is 3.6V or greater, this power source should be used for VDDIO_RF, and USB2_AVDD33 if strapped for USB. Otherwise leave this pin disconnected.	NC
7	VDDIO_RF	PWR I/P	-	VDDIO _RF	DC supply voltage for RF switch IO's. If VBAT is 3.6V or greater, connect to VOUT_3P3. Otherwise connect to VBAT.	--
8	GND	-	-	-	Ground	GND
9	SDIO_DATA0	I/O	B8	VDDIO	SDIO data lin0	NC
10	SDIO_DATA1	I/O	C7	VDDIO	SDIO data lin1	NC
11	SDIO_DATA3	I/O	B7	VDDIO	SDIO data lin3	NC
12	SDIO_CMD	I/O	C6	VDDIO	SDIO command line	NC
13	SDIO_DATA2	I/O	B6	VDDIO	SDIO data lin2	NC
14	GND	-	-	-	Ground	GND
15	SDIO_CLK	I	A6	VDDIO	SDIO clock input	NC
16	GND	-	-	-	Ground	GND
17	VBAT	PWR I/P	-	VBAT	DC supply voltage for module. Operational: VBAT is 3.2V to 4.8V (See VDDIO_RF configuration) ** VBAT at 3.6V to 4.8V has the same TX power but a better EVM/harmonic emissions margin.	--

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Pin #	Name	Type	Pins map to Chip	Voltage Ref.	Function	If Not Used
18	VBAT	PWR I/P	-	VBAT	DC supply voltage for module. Operational: VBAT is 3.2V to 4.8V (See VDDIO_RF configuration) ** VBAT at 3.6V to 4.8V has the same TX power but a better EVM/harmonic emissions margin.	--
Note:	VBAT should not rise 10%-90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should ***not*** be present first or be held high before VBAT is high.					
G1	GND	-	-	-	Ground	GND
19	GPIO_4	I	D3	VDDIO	Reserved for feature support WCI-2 LTE coexistence Interface	NC
20	GPIO_6	O	E4	VDDIO	Reserved for feature support 3-wire external coexistence interface. TX_CONF: Grant of access indication to external device.	NC
21	GPIO_3	I	D2	VDDIO	Reserved for feature support 3-wire external coexistence interface. STATUS: Indicates priority and TX/RX.	NC
22	GPIO_2	I	E1	VDDIO	Reserved for feature support 3-wire external coexistence interface. RF_ACTIVE: Request indication from external device for access	NC
23	GPIO_5	O	E3	VDDIO	Reserved for feature support WCI-2 LTE coexistence Interface	NC
24	USB2_DM	I/O	F1	-	Data minus of shared USB 2.0 port	NC
25	USB2_DP	I/O	G1	-	Data plus of shared USB 2.0 port	NC
26	USB2_RREF	I/O	H1	-	Bandgap reference resistor. When in SDIO interface, leave open. When in USB interface, connect to ground through 4.75K Ohm 1%.	--
27	GND	-	-	-	Ground	GND
28	USB2_AVDD33	PWR	H2	VBAT	In SDIO interface, short to Ground. In USB interface, If VBAT is 3.6V or greater, connect to VOUT_3P3. Otherwise connect to VBAT.	--
29	GND	-	-	-	Ground	GND
30	VDDIO	PWR	-	-	WLAN/BT IO Voltage (1.8V/3.3V).	--

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Pin #	Name	Type	Pins map to Chip	Voltage Ref.	Function	If Not Used
31	GPIO_1	I/O	D1	VDDIO	Reserved for feature support Reserved for WL_DEVICE_WAKE. Input from Host to wake up WLAN module.	NC
32	BT_REG_ON	I	C3	VDDIO	Enables Bluetooth regulators. Internal 10K pull-up to enable Bluetooth by default. Ground to disable Bluetooth.	NC
33	WL_REG_ON	I	D4	VDDIO	Enables WLAN regulators. Internal 10K pull-up to enable WLAN by default. Ground to disable WLAN.	NC
G2	GND	-	-	-	Ground	GND
34	SUSCLK	I	J2	200mVp-p to 3300mVp-p	External Sleep Clock input (32.768KHz) Externally provided sleep clock is required	--
35	GND	-		-	Ground	GND
36	GPIO_0	I/O	F3	VDDIO	Reserved for feature support Reserved for WL_HOST_WAKE. Output signal to wake up host.	NC
37	BT_DEVICE _WAKE	I	L2	VDDIO	Reserved for feature support BT_DEVICE_WAKE. Input signal from Host.	NC
38	BT_PCM_IN	I	J1	VDDIO	PCM data input.	NC
39	BT_PCM_CLK	I/O	K1	VDDIO	PCM clock. Can be master (Output) or slave (Input)	NC
40	BT_PCM_SYNC	I/O	K3	VDDIO	PCM Sync. Can be master (Output) or slave (Input); Or SLIMbus data.	NC
41	BT_PCM_OUT	O	L3	VDDIO	PCM data output.	NC
42	GND	-		-	Ground	GND
43	BT_UART_TXD	O	M1	VDDIO	Serial data output for the HCI UART interface.	NC
44	BT_UART_CTSn	I	M2	VDDIO	Active-Low clear-to-send signal for the HCI UART interface.	NC
45	BT_UART_RXD	I	N2	VDDIO	Serial data input for the HCI UART interface.	NC
46	BT_UART_RTSn	O	N3	VDDIO	Active-Low request-to-send signal for the HCI UART interface.	NC

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Pin #	Name	Type	Pins map to Chip	Voltage Ref.	Function	If Not Used
47	BT_HOST_WAKE	O	M3	VDDIO	Reserved for feature support BT_HOST_WAKE. Output signal to wake up Host.	NC
48	GND	-	-	-	Ground	GND
49	GND	-	-	-	Ground	GND
50	RF_OUT	-	-	-	RF output pin for the LWB5+ “ST” variant. For “SA” or “SC” variants, it is no connection.	NC
51	GND	-	-	-	Ground	GND
G3-G17	GND	-	-	-	Ground	GND

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13 Host Configuration Options

LWB5+ series wireless module supports various host configurations for WLAN and Bluetooth. Its detail configurations are shown in Table 36.

Table 36: Wi-Fi host interface configuration table

Strap Value CONFIG_HOST [2-0]	WLAN	Bluetooth/BLE	Notes
000	USB	USB	USB2.0
101	SDIO	UART	SDIO 1.8V (Supports DS/HS and SDR speed modes)
100	SDIO	UART	SDIO 3.3V (Supports DS and HS speed modes only)

14 Mechanical Specifications

Module dimensions of LWB5+ series wireless module is 17 x 12 x 2.1 mm. Detail drawings are shown in Figure 10.

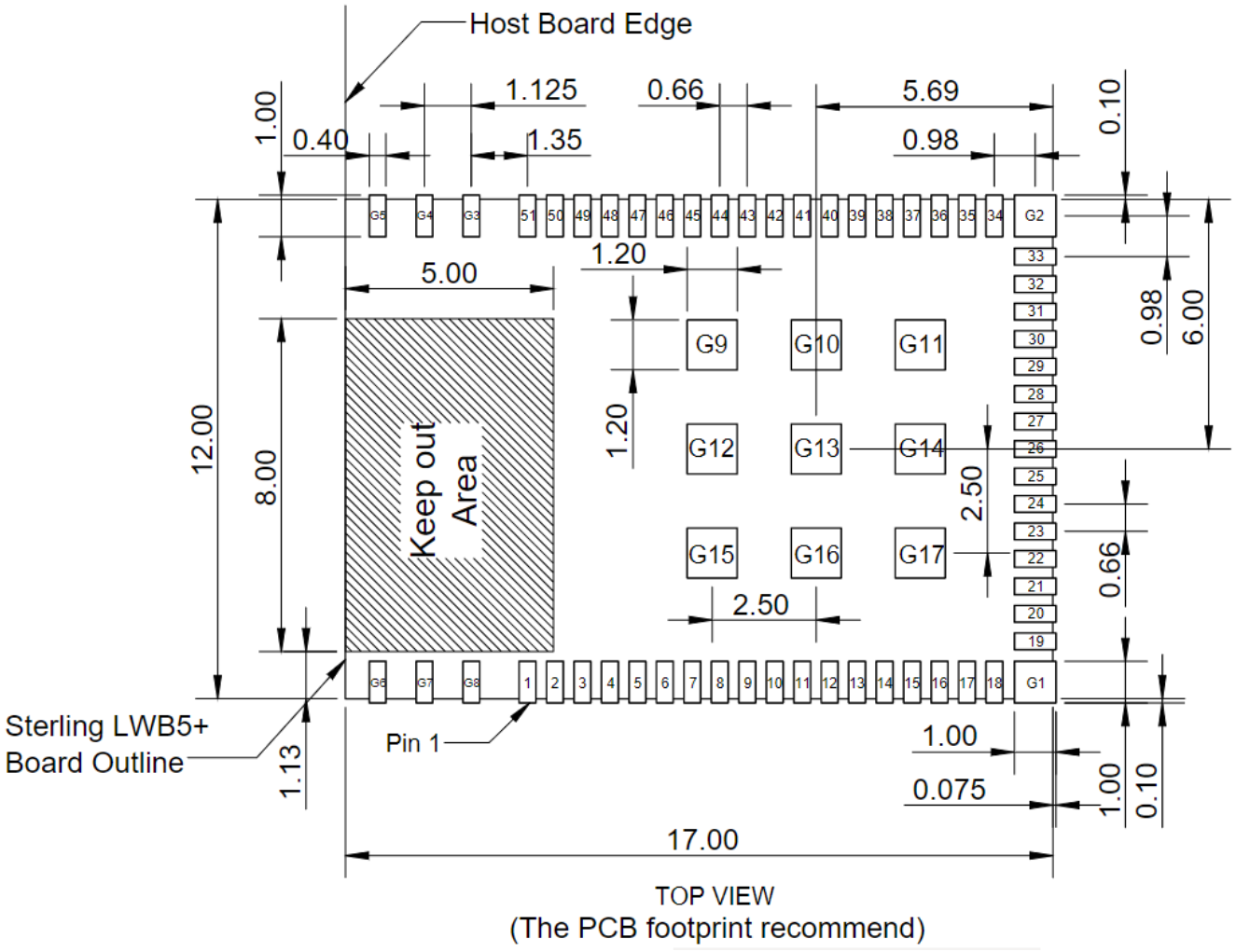

Figure 10: Mechanical drawing - LWB5+ series wireless module

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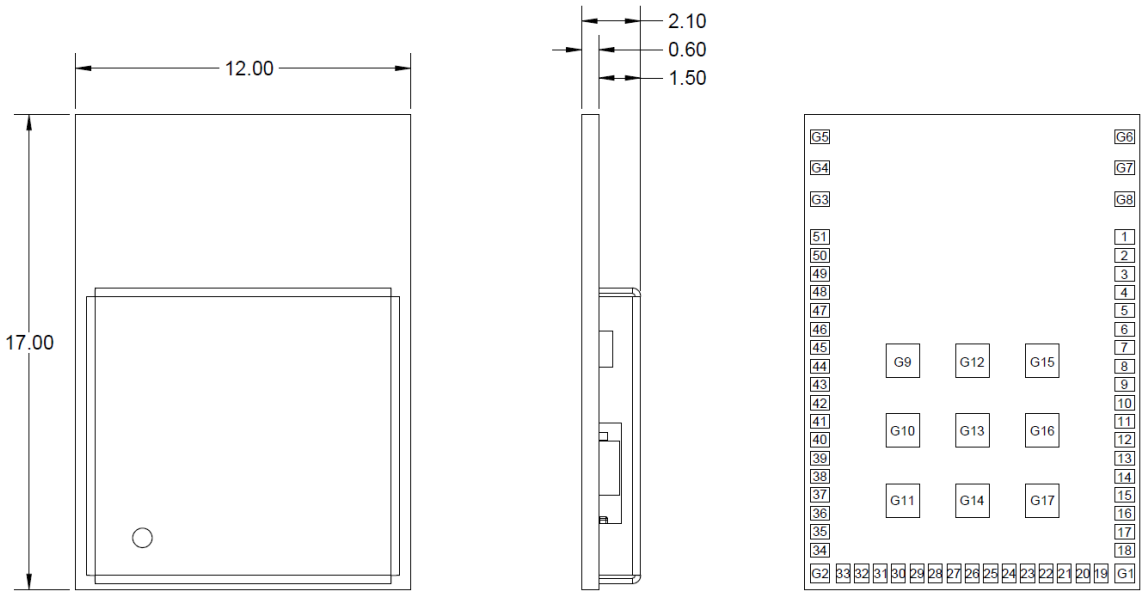
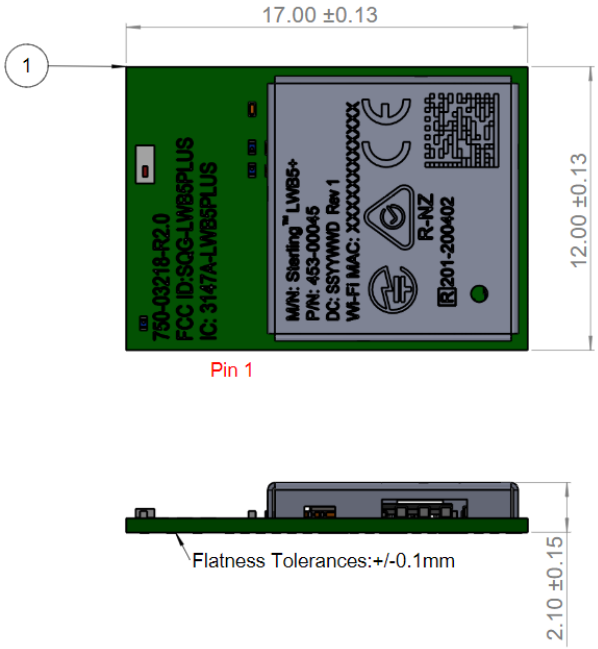
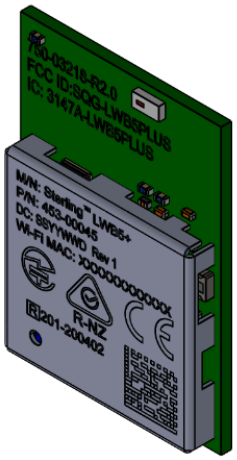


453-0045





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453-0046

453-0047

Figure 11: Module dimension of LWB5+ series wireless module – Top View

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Note: The Wi-Fi MAC address is located on the product label.
The last digit of Wi-Fi MAC address is assigned to either *0, 2, 4, 6, 8, A, C, E.*
The Bluetooth MAC address is the Wi-Fi MAC address plus 1.

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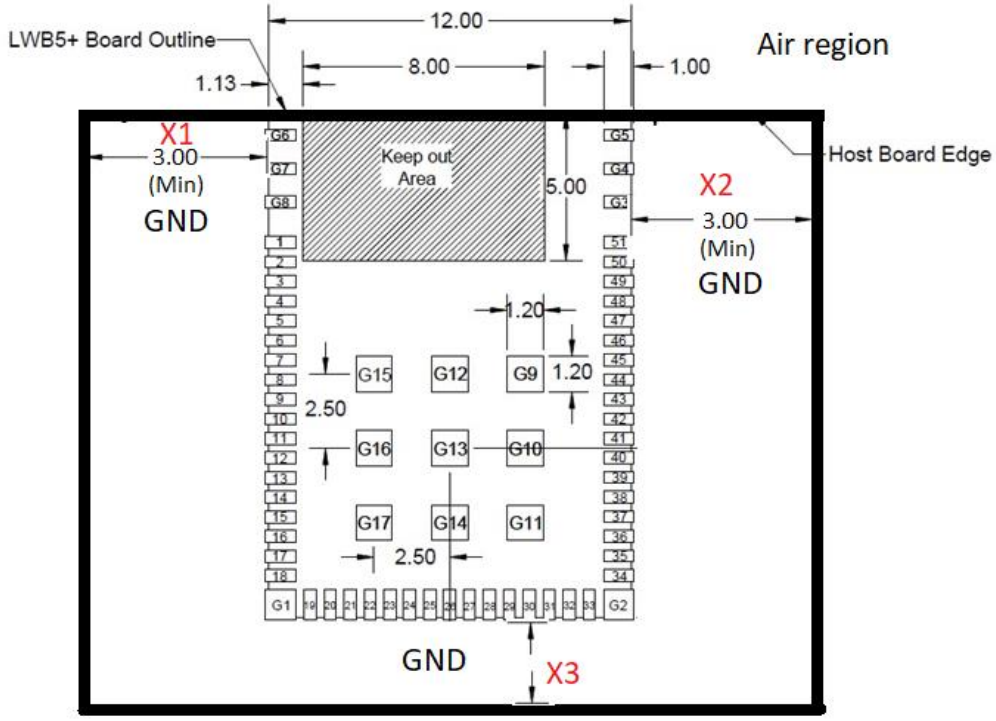
15 RF Layout Design Guidelines

The following is a list of RF layout design guidelines and recommendation when installing a Laird Connectivity radio into your device:

- Do not run antenna cables directly above or directly below the radio.
- Do not place any parts or run any high-speed digital lines below the radio.
- If there are other radios or transmitters located on the device (such as a Bluetooth radio), place the devices as far apart from each other as possible. Also, make sure there is at least 25 dB isolation between these two antennas.
- Ensure that there is the maximum allowable spacing separating the antenna connectors on the Laird Connectivity radio from the antenna. In addition, do not place antennas directly above or directly below the radio.
- Laird Connectivity recommends the use of a double-shielded cable for the connection between the radio and the antenna elements.
- Be sure to put a 10 µF capacitor on ***each*** 3.3V power pin. Also, place that capacitor to the pin as close as possible to make sure the internal PMU works correctly.
- Use proper electro-static-discharge (ESD) procedures when installing the Laird Connectivity radio module. To avoid negatively impacting Tx power and receiver sensitivity, do not cover the antennas with metallic objects or components
- The LWB5+ on-board antenna variant must be located at the edge of the host PCB surrounded by ground on three sides. A larger surround ground with X1, X2, X3 ≥ 15 millimeters has optimized performance. When X1, X2, X3 are reduced to 3 millimeters, the peak antenna gain drops to -3 dBi.



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16 Application Note for Surface Mount Modules

16.1 Introduction

Laird Connectivity's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

16.2 Shipping

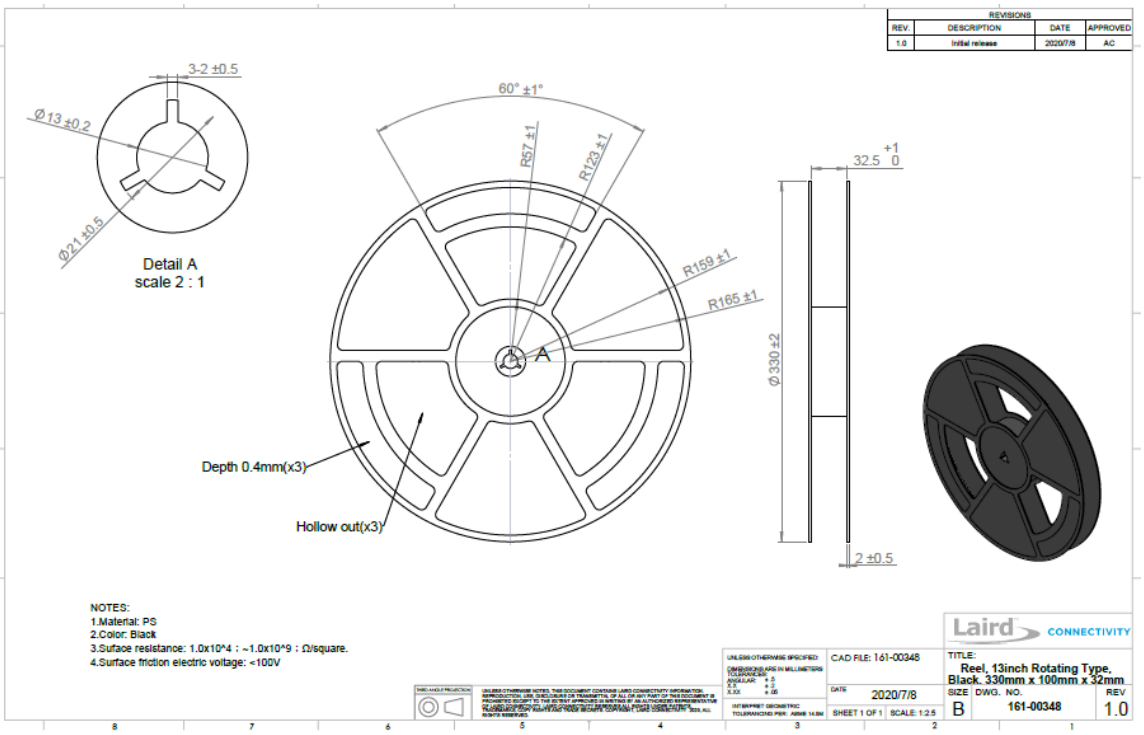

Figure 12: Reel specifications

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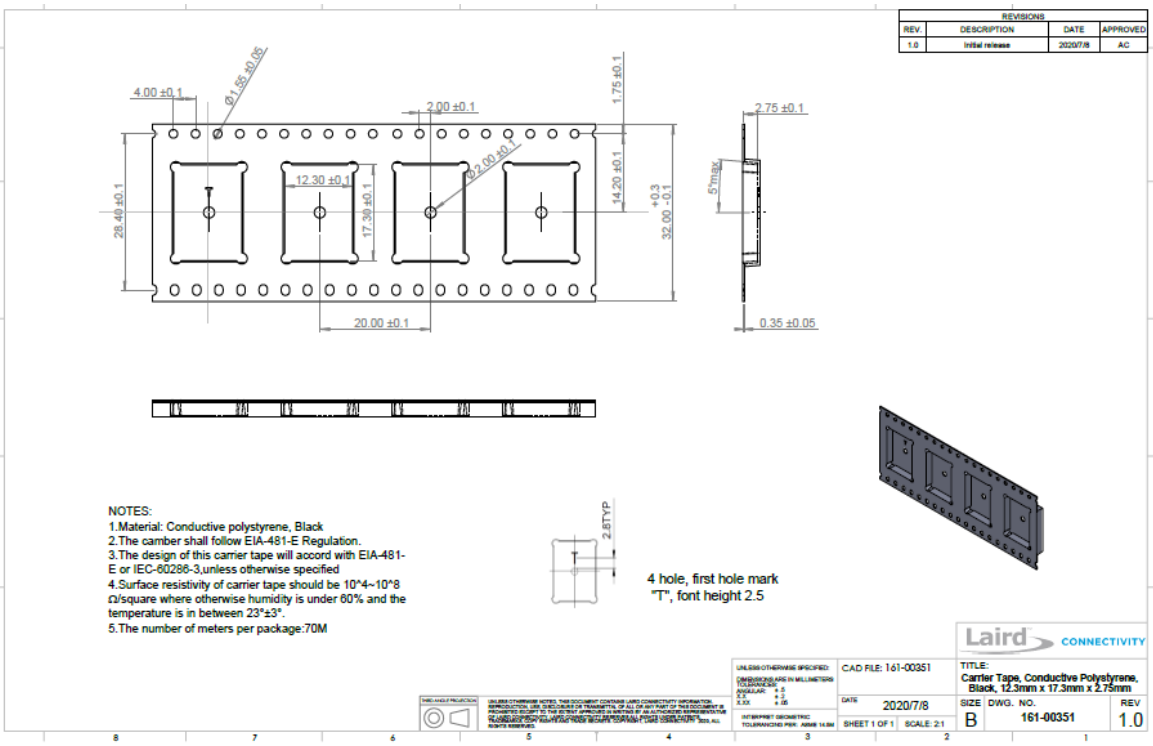

Figure 13: Tape specifications, 161-00351

There are 1,000 Sterling LWB5+ modules taped in a reel (and packaged in a pizza box) and two boxes per carton (2000 modules per carton). Reel, boxes, and carton are labeled with the appropriate labels.

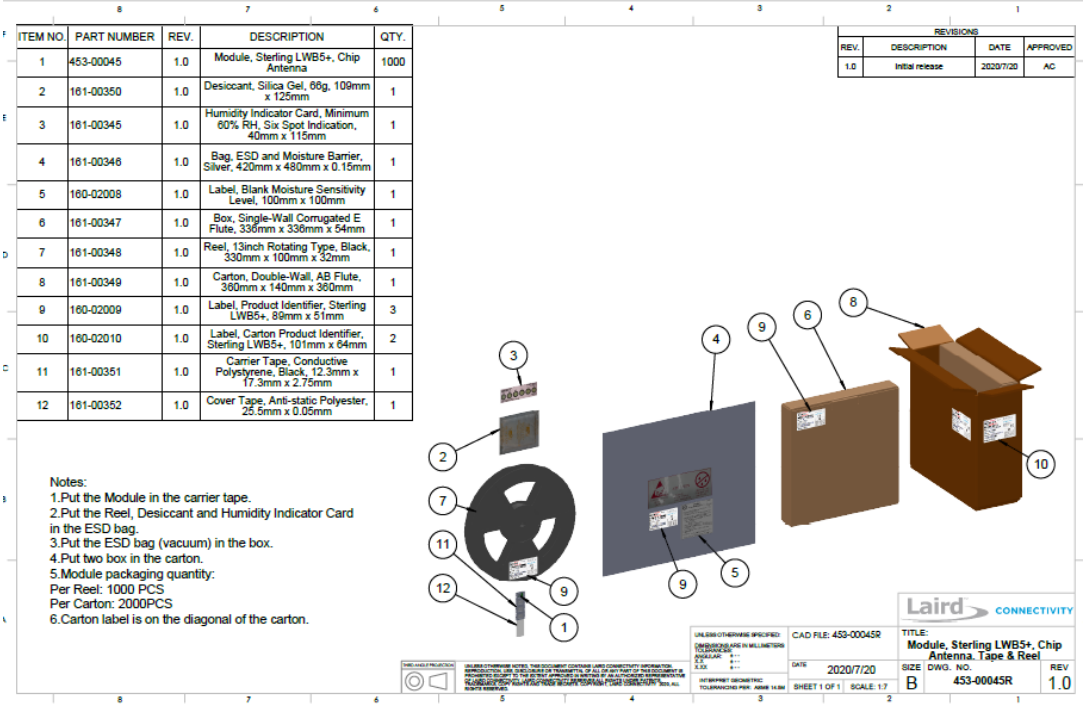

Figure 14: Sterling LWB5+ packaging process

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16.3 Labelling

The following labels are located on the antistatic bag.

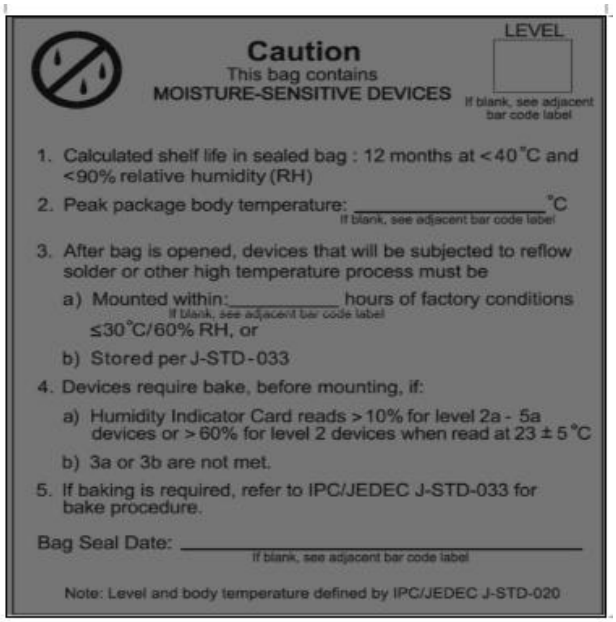

Figure 15: Anti-static bag label – 1

Figure 16: Anti-static bag label – 2

The following label is located on the pizza box.

Figure 17: Box label

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The following package label is located on adjacent sides of the master carton.

Figure 18: Master carton package label

16.4 Required Storage Conditions

16.4.1 Prior to Opening the Dry Packing

The following are required storage conditions ***prior* to opening the dry packing**:

- Normal temperature: 5~40˚C
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means relative humidity.

16.4.2 After Opening the Dry Packing

The following are required storage conditions ***after* opening the dry packing** (to prevent moisture absorption):

- Storage conditions for one-time soldering:
  - Temperature: 5-25°C
  - Humidity: 60% or less
  - Period: 72 hours or less after opening
- Storage conditions for two-time soldering
  - Storage conditions following opening and prior to performing the 1st reflow:
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: A hours or less after opening
  - Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: B hours or less after completion of the 1st reflow

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Note: Should keep A+B within 72 hours.

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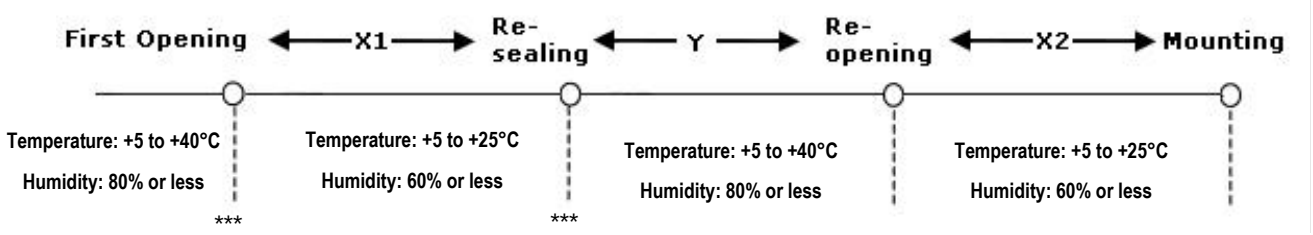
16.4.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices *once* prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

- Storage temperature and humidity:



*** - External atmosphere temperature and humidity of the dry packing

- Storage period:
  - X1+X2 – Refer to After Opening the Dry Packing storage requirements. Keep is X1+X2 within 72 hours.
  - Y – Keep within two weeks or less.

16.5 Baking Conditions

Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
- Once the packaging is opened, the SiP must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <30˚C and <60% relative humidity.
- If the SiP is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125 ˚C (±5 ˚C).

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16.6 Surface Mount Conditions

The following soldering conditions are recommended to ensure device quality.

16.6.1 Soldering

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point – IC package surface
- Temperature profile:

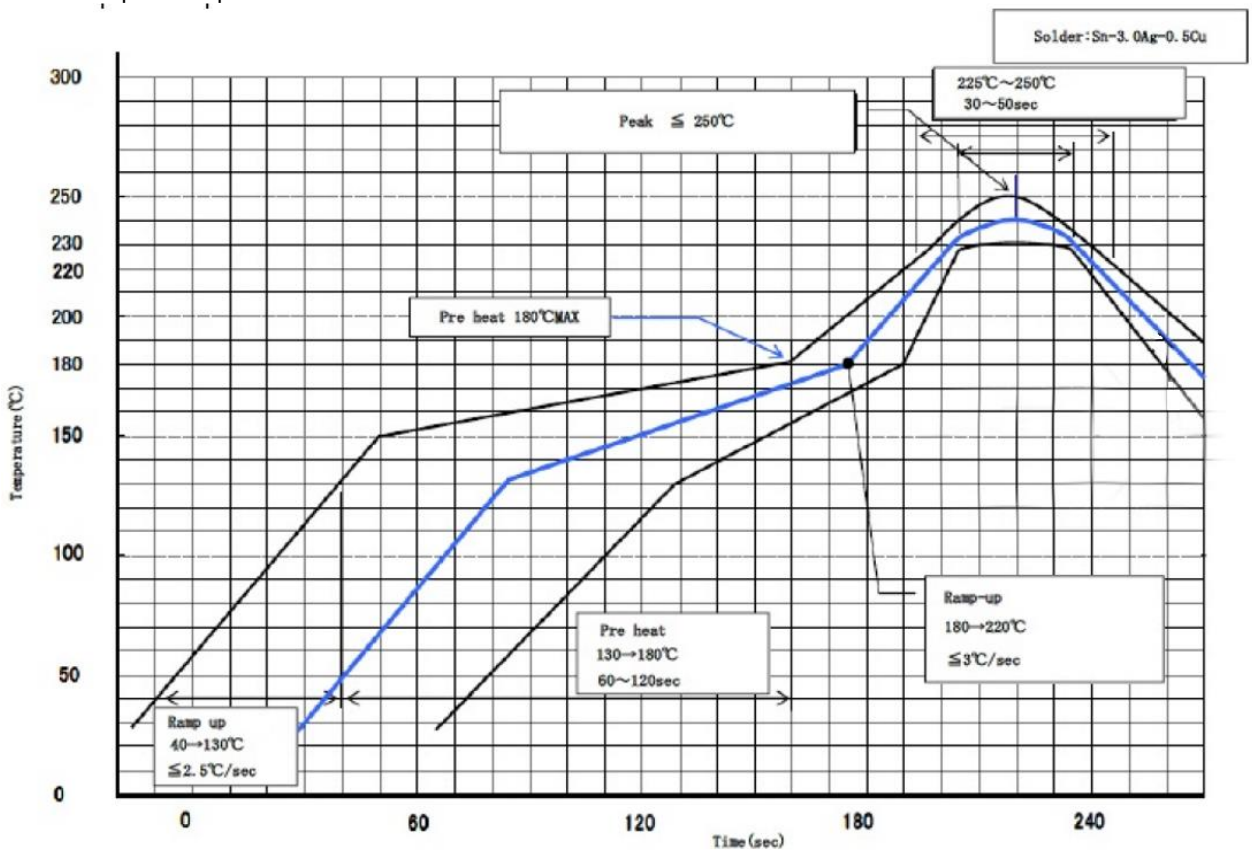

Figure 19: Temperature profile

- Ramp-up: 40-130˚C. Less than 2.5˚C/sec
- Pre heat: 130-180˚C 60-120 sec, 180˚C MAX
- Ramp-up: 180-220˚C. Less than 3˚C/sec
- Peak Temperature: MAX 250˚C
  - 225˚C ~ 250˚C, 30 ~ 50 sec
- Ramp-down: Maximum 6˚C/sec

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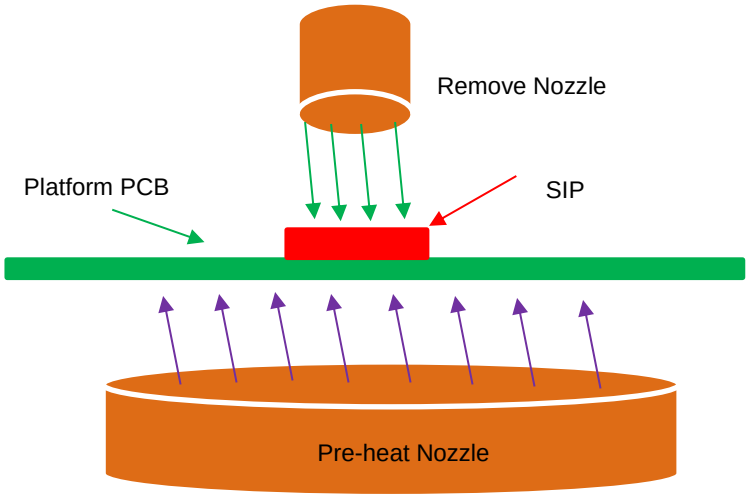
16.6.2 Cautions When Removing the SIP from the Platform for RMA

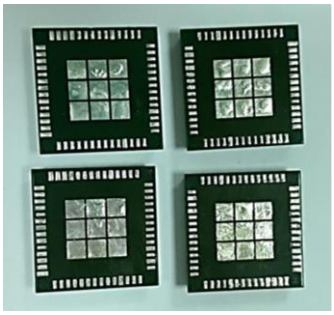
- Bake the platform before removing the SIP from the platform. Reference baking conditions.
- Remove the SIP by using a hot air gun. This process should be carried out by a skilled technician.

Suggestion conditions:

- One-side component platform:
  - Set the hot plate at 280°C.
  - Put the platform on the hot plate for 8~10 seconds.
  - Remove the SIP from platform.
- Two-side components platform:
  - Use two hot air guns
  - On the bottom side, use a pre-heated nozzle (temperature setting of 200~250°C) at a suitable distance from the platform PCB.
  - On the top side, apply a remove nozzle (temperature setting of 330°C). Heat the SIP until it can be removed from platform PCB.

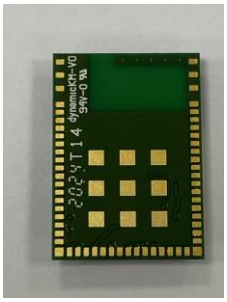


- Remove the residue solder under the bottom side of SIP. (Note: Alternate module pictured as an example)



(Not accepted for RMA)

Example SIP with residue solder on the bottom



(Accepted for RMA analysis)

Sterling LWB5+ module without residue solder o

- Remove and clean the residue flux as needed.

16.6.3 Precautions for Use

- Opening/handing/removing must be done on an anti-ESD treated workbench. All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.
- The LWB5+ modules are MSL level 4

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17 REGULATORY

Note: For complete regulatory information, refer to the Sterling LWB5+ Regulatory Information document which is also available from the Sterling LWB5+ product page.

The Sterling LWB5+ holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-LWB5PLUS
EU	N/A
Canada (ISED)	3147A-LWB5PLUS
Japan (MIC)	201-200402
Australia	N/A
New Zealand	N/A

18 ORDERING INFORMATION

Part Number	Description
453-00045R	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 - Integrated Antenna (Tape and Reel)
453-00046R	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – MHF4 (Tape and Reel)
453-00047R	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – Trace Pin (Tape and Reel)
453-00045C	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – Integrated Antenna (Cut Tape)
453-00046C	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – MHF4 (Cut Tape)
453-00047C	1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – Trace Pin (Cut Tape)
453-00045-K1	Development Kit for 1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 - Integrated Antenna
453-00046-K1	Development Kit for 1x1 802.11 a/b/g/n/ac + Bluetooth 5.2 – MHF4

18.1 General Comments

This is a preliminary datasheet. Please check with Laird Connectivity for the latest information before commencing a design. If in doubt, ask.

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19 BLUETOOTH SIG QUALIFICATION

19.1 Overview

The LWB5+ Series module is listed on the Bluetooth SIG website as a qualified Controller Subsystem.

Design Name	Owner	Declaration ID	Link to listing on the SIG website
Sterling LWB5+	Laird Connectivity	D050382	https://launchstudio.bluetooth.com/ListingDetails/119009

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to register as a member of the Bluetooth SIG – www.bluetooth.org

The following is a link to the Bluetooth Registration page: https://www.bluetooth.org/login/register/

For each Bluetooth Design, it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document, (login is required to views this document):

https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

19.2 Qualification Steps When Referencing a Laird Connectivity Controller Subsystem Design

To qualify your product when referencing a Laird Connectivity Controller Subsystem design, follow these steps:

1. To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

   Note: A username and password are required to access this site.

2. In step 1, select the option, New Listing and Reference a Qualified Design.
3. Enter D050382 in the Controller Subsystem table entry.
4. Enter your complimentary Host Subsystem and optional Profile Subsystem QDID in the table entry.
5. Select your pre-paid Declaration ID from the drop-down menu or go to the Purchase Declaration ID page.

   Note: Unless the Declaration ID is pre-paid or purchased with a credit card, you cannot proceed until the SIG invoice is paid.

6. Once all the relevant sections of step 1 are finished, complete steps 2, 3, and 4 as described in the help document accessible from the site.

   Your new design will be listed on the SIG website and you can print your Certificate and DoC.

For further information please refer to the following training material:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

If you require assistance with the qualification process please contact our recommended Bluetooth Qualification Expert (BQE), Steve Flooks, steve.flooks@eurexuk.com.

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20 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

Laird Connectivity
Support Centre: https://www.lairdconnect.com/resources/support
Email: wireless.support@lairdconnectivity.com
Phone: Americas: +1-800-492-2320
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Hong Kong: +852 2762 4823
Web: https://www.lairdconnect.com/products

Note: Information contained in this document is subject to change.