Datasheet

BL653µ Series

Version 2.1

Revision History

Version	Date	Notes	Contributor(s)	Approver
1.0	09 Dec 2020	Initial version	Raj Khatri	Jonathan Kaye
1.1	7 Jan 2021	Updated Bluetooth SIG Listing	Jonathan Kaye	Jonathan Kaye
1.2	19 Jan 2021	Transferred regulatory information to a separate document	Maggie Teng	Jonathan Kaye
1.3	03 Feb 2021	Correct tables section 5.11 and 5.12.	Raj Khatri	Jonathan Kaye
1.4	18 Feb 2021	Fixed equation in 5.5.2 NFC Antenna Coil Tuning Capacitors	Raj Khatri	Dave Drogowski
1.5	22 Apr 2021	Corrected all instances PCB trace antenna to chip antenna	Raj Khatri	Jonathan Kaye
1.6	26 Jul 2021	Added board image to polar plot in section 5.18 453-00059 On-board chip antenna characteristics	Raj Khatri	Dave Drogowski
1.7	14 Oct 2021	Updated Table 24 (removed unnecessary row)	Raj Khatri	Jonathan Kaye
1.8	22 Dec 2021	Updated Mechanical Details	Dave Drogowski	Andrew Chen
1.9	21 Mar 2022	Clarification: Development board for BL653µ is the BL653 DVK (no BL653µ DVK)	Mark Duncombe	Dave Drogowski
2.0	3 Oct 2022	Fixed incorrect module part number typos	Damien Fourcade	Raj Khatri
2.1	9 Nov 2022	Fixed incorrect pin references in Table 17: USB interface	Mark Duncombe	Raj Khatri

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CONTENTS

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Overview and Key Features

Every BL653µ Series module is designed to simplify OEMs enablement of Bluetooth Low Energy (Bluetooth LE) v5.1 and Thread (802.15.4) to small, portable, power-conscious devices. The BL653µ provides engineers with considerable design flexibility in both hardware and software programming capabilities. Based on the world-leading Nordic Semiconductor
1 nRF52833 chipset, the BL653µ modules provide ultra-low power consumption with outstanding wireless range via +8 dBm of transmit power and the Long Range (CODED PHY) Bluetooth 5 feature. The BL653µ is programmable via Laird Connectivity's *smart*BASIC language, AT command set, Zephyr RTOS, or Nordic's software development kit (SDK).

*smart*BASIC is an event-driven programming language that is highly optimized for memory-constrained systems such as embedded modules. It was designed to make Bluetooth LE development quicker and simpler, vastly cutting down time to market.

The Nordic SDK, on the other hand, offers developers source code (in C) and precompiled libraries containing Bluetooth LE and ANT+ device profiles, wireless communication, as well as application examples.

Note: BL653µ hardware provides all functionality of the nRF52833 chipset used in the module design. This is a hardware datasheet only – it does not cover the software aspects of the BL653µ.

For customers using *smart*BASIC, refer to the *smart*BASIC extensions guide (available from the BL653µ product page of the Laird Connectivity website. For customers using the Nordic SDK, refer to www.nordicsemi.com. For customers using Zephyr RTOS, refer to www.zephyrproject.org

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1.1 Features and Benefits

- Bluetooth v5.1 – Single mode
- NFC
- 802.15.4 (Thread) radio support (not certified)
- External or internal antennas
- Multiple programming options
  - *smart*BASIC
  - AT command set
  - Nordic SDK in C
  - Zephyr RTOS
- Compact footprint
- Programmable Tx power +8 dBm to -20 dBm, -40 dBm
- Rx sensitivity -96 dBm (1 Mbps), -103 dBm (125 kbps)
- Ultra-low power consumption
- Tx – 4.9 mA peak (at 0 dBm, DCDC on) (See Note 1 in the *Power Consumption* section)
- Rx: 4.6 mA peak (DCDC on) (See Note 1 in the *Power Consumption* section)
- Standby Doze – 2.6 uA typical
- Deep Sleep – 0.6 uA – (See Note 4 in the *Power Consumption* section)
- UART, GPIO, ADC, PWM, FREQ output, timers, I2C, SPI, I2S, PDM, and USB interfaces
- Fast time-to-market
- FCC, CE, ISED, RCM, Japan, and KC certified
- Full Bluetooth Declaration ID
- Other regulatory certifications on request
- No external components required
- Extended Industrial temperature range (-40° C to +105° C)

1.2 Application Areas

- Medical devices
- IoT sensors
- Appcessories
- Fitness sensors
- Location awareness
- Home automation

2 Specification

2.1 Specification Summary

Table 1: Specification Summary

Categories/Feature	Implementation	
Wireless Specification		
Bluetooth®	▪ BT 5.1 – Single mode ▪ Angle-of-arrival (AoA) and angle-of-departure (AoD) – BT 5.1 ▪ 4x Range (CODED PHY support) – BT 5.0 ▪ 2x Speed (2M PHY support) – BT 5.0 ▪ LE Advertising Extensions – BT 5.0 ▪ Concurrent master, slave ▪ Bluetooth LE Mesh capabilities ▪ Diffie-Hellman based pairing (LE Secure Connections) – BT 4.2 ▪ Data Packet Length Extension – BT 4.2 ▪ Link Layer Privacy (LE Privacy 1.2) – BT 4.2 ▪ LE Dual Mode Topology – BT 4.1 ▪ LE Ping – BT 4.1	
Frequency	2.402 - 2.480 GHz	
Raw Data Rates	1 Mbps Bluetooth LE (over-the-air) 2 Mbps Bluetooth LE (over-the-air) 125 kbps Bluetooth LE (over-the-air) 500 kbps Bluetooth LE (over-the-air)	
Maximum Transmit Power Setting	+8 dBm	Conducted 453-00059 (Integrated antenna)
	+8 dBm	Conducted 453-00060 (Trace pin–connecting to External antenna)
Minimum Transmit Power Setting	-40 dBm, -20 dBm (in 4 dB steps) -16 dBm, -12 dBm, - 8 dBm, - 4 dBm, 0 dBm, 2 dBm, 4 dBm, 5 dBm, 6 dBm, 7 dBm	
Receive Sensitivity (≤ 37-byte packet)	Bluetooth LE 1 Mbps (BER=1E-3)	-96 dBm typical
	Bluetooth LE 2 Mbps	-92 dBm typical
	Bluetooth LE 125 kbps	-103 dBm typical
	Bluetooth LE 500 kbps	-99 dBm typical
Link Budget (conducted)	@ Bluetooth LE 1 Mbps	104 dB
	@ Bluetooth LE 125 kbps	111 dB

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Categories/Feature	Implementation
NFC	
NFC-A Listen mode compliant	**Based on NFC forum specification** ▪ 13.56 MHz ▪ Date rate 106 kbps ▪ NFC Type 2 and Type 4 emulation **Modes of Operation:** ▪ Disable ▪ Sense ▪ Activated **Use Cases:** ▪ Touch-to-Pair with NFC ▪ NFC enabled Out-of-Band Pairing
System Wake-On-Field function	Proximity Detection
Host Interfaces and Peripherals	
Total	32 x multifunction I/O lines
UART	2 UARTs Tx, Rx, CTS, RTS DCD, RI, DTR, DSR (See Note 1 in the Module Specification Notes) Default 115200, n, 8, 1 From 1,200 bps to 1 Mbps
USB	USB 2.0 FS (Full Speed, 12 Mbps).
GPIO	Up to 32 with configurable: ▪ I/O direction ▪ O/P drive strength (standard 0.5 mA or high 3mA/5 mA) ▪ Pull-up /pull-down ▪ Input buffer disconnect
ADC	Eight 8/10/12-bit channels 0.6 V internal reference Configurable 4, 2, 1, 1/2, 1/3, 1/4, 1/5 1/6 (default) pre-scaling Configurable acquisition time 3uS, 5uS, 10uS (default), 15uS, 20uS, 40uS. One-shot mode
PWM Output	PWM outputs on 16 GPIO output pins ▪ PWM output duty cycle: 0%-100% ▪ PWM output frequency: Up to 500 kHz
FREQ Output	FREQ outputs on 16 GPIO output pins ▪ FREQ output frequency: 0 MHz-4 MHz (50% duty cycle)
I2C	Two I2C interface (up to 400 kbps) – See Note 2 in the Module Specification Notes
SPI	Four SPI master slave interface (up to 4 Mbps)
Temperature Sensor	▪ One temperature sensor ▪ Temperature range equal to the operating temperature range ▪ Resolution 0.25 degrees
RSSI Detector	▪ One RF received signal strength indicator ▪ ±2 dB accuracy (valid over -90 to -20 dBm) ▪ 1 dB resolution

Categories/Feature	Implementation
I2S	One inter-IC sound interface
PDM	One pulse density modulation interface
Optional (External to the BL653µ module)	
External 32.768 kHz crystal	For customer use, connect ±20 ppm accuracy crystal for more accurate protocol timing.
Profiles	
Supported Services	▪ Central mode ▪ Peripheral mode ▪ Mesh (with custom models) ▪ Custom and adopted profiles
Programmability	
*smart*BASIC	▪ FW upgrade via JTAG or UART ▪ Application download via UART or Via Over-the-Air (if SIO_02 pin is pulled high externally)
Nordic SDK	Via JTAG
Operating Modes	
*smart*BASIC	**Self-contained Run mode** Selected by nAutoRun pin status: LOW (0V). Then runs $autorun$ (*smart*BASIC application script) if it exists. **Interactive/Development mode** HIGH (VDD). Then runs via at+run (and *file name* of *smart*BASIC application script).
AT Command set	Comprehensive Hayes-style AT command set
Nordic SDK	As per Nordic SDK
Zephyr RTOS	As per www.zephyrproject.org
Supply Voltage	
Supply (VDD or VDD_HV) options	▪ Normal voltage mode VDD 1.7- 3.6 V – Internal DCDC converter or LDO (See Note 3 in the Module Specification Notes) OR ▪ High voltage mode VDD_HV 2.5V-5.5V Internal LDO (See Note 3 and Note 4 in the Module Specification Notes)
Power Consumption	
Active Modes Peak Current (for maximum Tx power +8 dBm) – Radio only	14.2 mA peak Tx (with DCDC)
Active Modes Peak Current (for Tx power -40 dBm) – Radio only	2.3 mA peak Tx (with DCDC)
Active Modes Average Current	Depends on many factors, see *Power Consumption*
Ultra-low Power Modes	Standby Doze 2.6 uA typical Deep Sleep 0.6 uA
Antenna Options	
Internal	Chip antenna – on-board **453-00059 variant**

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Categories/Feature	Implementation
External	▪ Dipole antenna (with IPEX connector) ▪ Dipole PCB antenna (with IPEX connector) ▪ Connection via RF connector (IPEX MH4) – **453-00060 variant (RF trace pin)** See the Antenna Information sections for FCC and ISED, MIC, RCM, KC and CE.
Physical	
Dimensions	6.3 mm x 8.6 mm x 1.6 mm 453-00059 (BL653u Micro module -Integrated antenna) 6.3 mm x 5.6 mm x 1.6 mm 453-00060 (BL653u Micro module -RF Trace pin) Pad Pitch – 0.658 mm Pad Type – Two rows of pads
Weight	<1 gram
Environmental	
Operating	-40 ˚C to +105 ˚C
Storage	-40 ˚C to +85 ˚C
Miscellaneous	
Lead Free	Lead-free and RoHS-compliant
Warranty	One-year warranty
Moisture Sensitivity Level (MSL)	4
Development Tools	
Development Kit	None. Please use development kit for BL653 per module SKU (453-00039-K1 and 453-00041-K1) and free software tools
Approvals	
Bluetooth®	Full Bluetooth SIG Declaration ID
FCC/IC/CE/MIC/RCM/KC	All BL653µ Series

Module Specification Notes:

Note 1	DSR, DTR, RI, and DCD can be implemented in the *smart*BASIC application or through the Nordic SDK.
Note 2	With I2C interface selected, pull-up resistors on I2C SDA and I2C SCL ***must*** be connected externally as per I2C standard.
Note 3	Use of the internal DCDC (REG1) convertor or LDO (REG1) is decided by the underlying Bluetooth LE stack.
Note 4	In High Voltage mode (VDD_HV), no external current draw (from VDD_NRF pin) is allowed (limitation of nRF52833 chipset).

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Hardware Specifications

3.1 Block Diagram and Pin-out

3

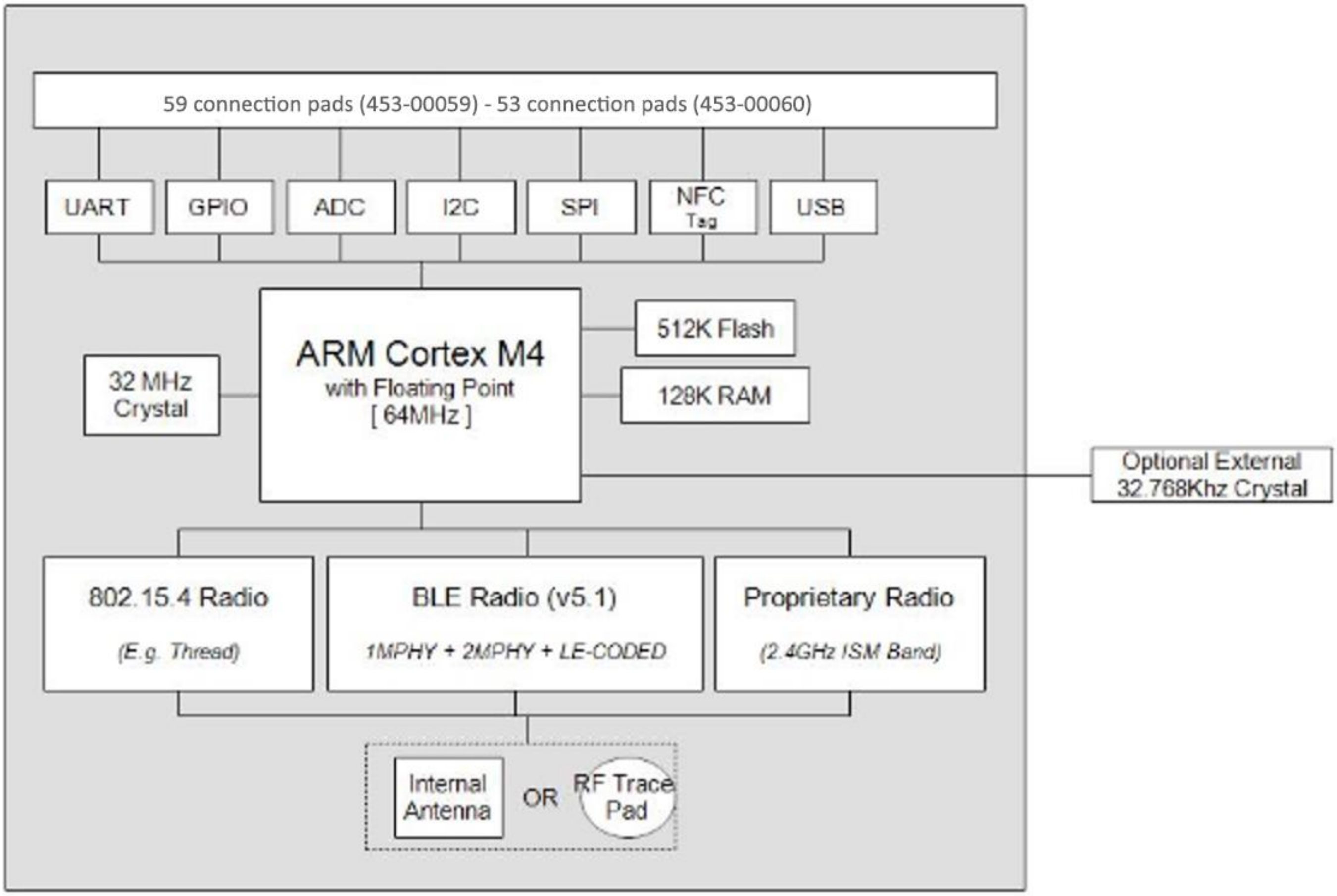

Figure 1: BL653µ block diagram

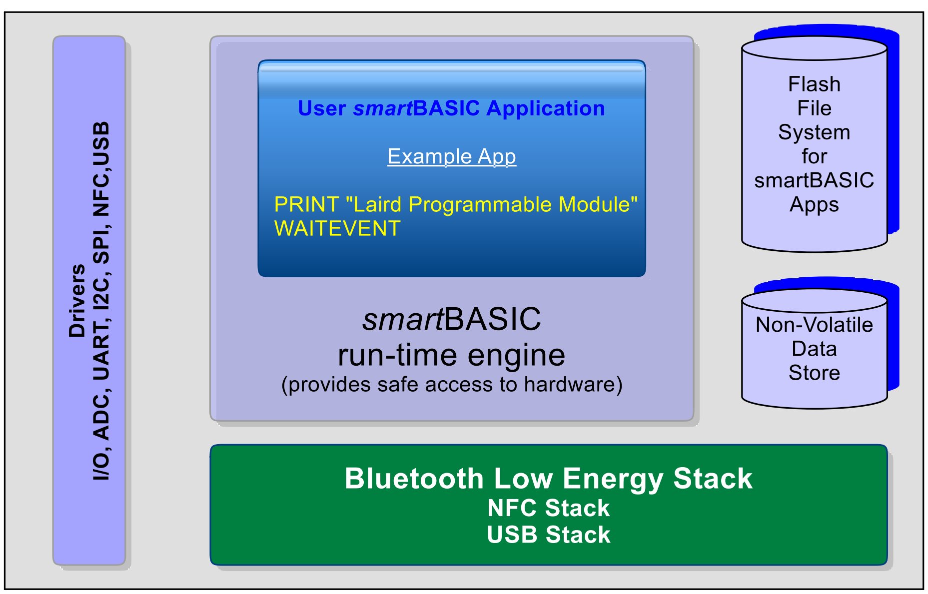

Figure 2: Functional HW and SW block diagram for BL653µ series Bluetooth LE module

BL653µ Schematic Symbols (Altium format) can be found on the BL653µ product page.

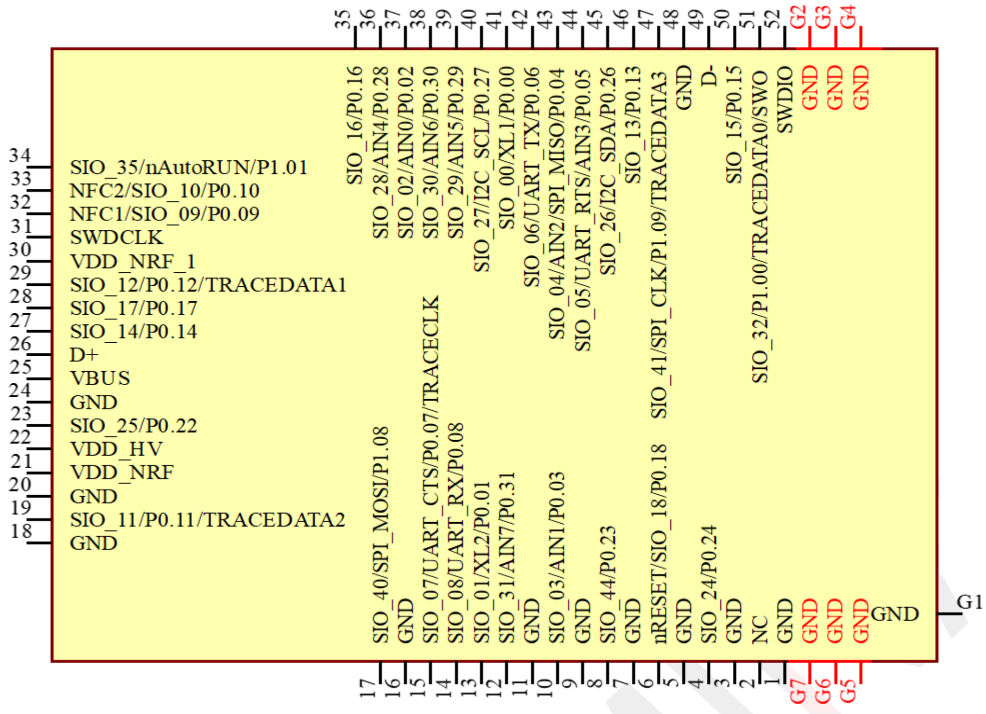

Figure 3: Top view – Schematic Symbol of 453-00059 BL653u Micro Bluetooth LE module (Nordic nRF52833) – Integrated antenna

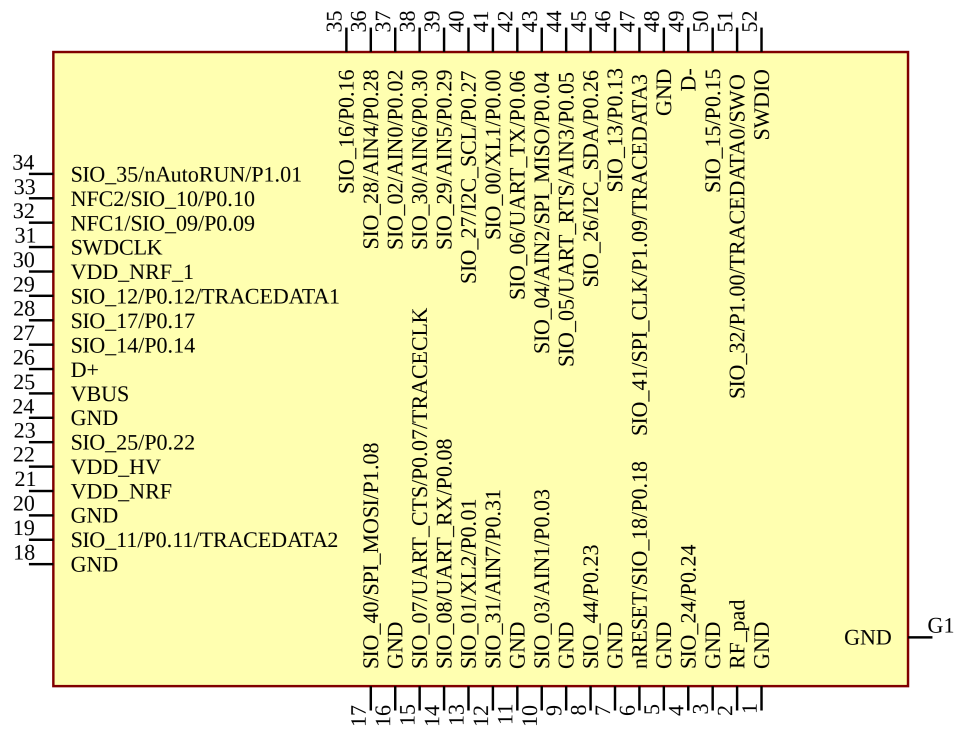

Figure 4:Top view - Schematic Symbol of 453-00060 BL653u Micro Bluetooth LE module (Nordic nRF52833) – Trace pin

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3.2 Pin Definitions

Table 2: Pin definitions

Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull-Up/ Down	nRF52833 WLCSP Pin	nRF52833 WLCSP Name	Comment
1	GND	-	-	-	-	-	VSS	-
2	RF pad (on 453-00060) or No Connect (on 453-00059)	-	-	-	-	-	-	Active on BL653µ RF pad module (453-00060) variant only, see Note11. On BL653u Integrated Antenna module variant, pad is a No Connect.
3	GND	-	-	-	-	-	VSS	-
4	SIO_24	SIO_24		In	Pull-up	G3	P0.24	**Laird Connectivity BL653 Devkit:** BUTTON3
5	GND	-	-	-	-	-	VSS	-
6	nRESET	nRESET	SIO_18	In	Pull-up	H4	P0.18/ nRESET	System Reset (Active Low)
7	GND	-	-	-	-	-	VSS	-
8	SIO_44	SIO_44	-	In	Pull-up	D7	P0.23	**Laird Connectivity BL653 Devkit:** SPI EEPROM SPI_Eeprom_CS, Input
9	GND	-	-	-	-	-	VSS	-
10	SIO_03/ AIN1	SIO_03	AIN1	In	Pull-up	A4	P0.03/AIN1	**Laird Connectivity BL653 Devkit:** Temp Sens Analog
11	GND	-	-	-	-	-	VSS	-
12	SIO_31/ AIN7	SIO_31	AIN7	In	Pull-up	B6	P0.31/AIN7	-
13	SIO_01/ XL2	SIO_01	XL2	In	Pull-up	B7	P0.01/XL2	**Laird Connectivity BL653 Devkit:** Optional 32.768kHz crystal pad XL2 and associated load capacitor
14	SIO_08/ UART_RX	SIO_08	UART_RX	In	Pull-up	E7	P0.08	UARTCLOSE() selects DIO functionality UARTOPEN() selects UART COMMS behavior
15	SIO_07/ UART_CTS	SIO_07	UART_CTS	IN	Pull-down	E8	P0.07/ TRACECLK	UARTCLOSE() selects DIO functionality UARTOPEN() selects UART COMMS behaviour
16	GND	-	-	-	-	-	VSS	-

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull-Up/ Down	nRF52833 WLCSP Pin	nRF52833 WLCSP Name	Comment
17	SIO_40/ SPI_MOSI	SIO_40	SPI_MOSI	In	Pull-up	F9	P1.08	**Laird Connectivity BL653 Devkit:** SPI EEPROM. SPI_Eeprom_MOSI, Output SPIOPEN() in *smart*BASIC selects SPI function, MOSI and CLK are outputs in SPI master.
18	GND	-	-	-	-	-	VSS	-
19	SIO_11	SIO_11	-	In	Pull-up	G8	P0.11/ TRACEDATA2	**Laird Connectivity BL653 Devkit:** BUTTON1
20	GND	-	-	-	-	-	VSS	-
21	VDD_NRF	-	-	-	-	G9, A9, B3	VDD	1.7V to 3.6V
22	VDD_HV	-	-	-	-	H9	VDDH	2.5V to 5.5V
23	SIO_25	SIO_25	-	In	Pull-up	J3	P0.22	**Laird Connectivity BL653 Devkit:** BUTTON4
24	GND	-	-	-	-	-	VSS	-
25	VBUS	-	-	-	-	H8	VBUS	4.35V – 5.5V
26	D+	D+	-	In		J7	D+	-
27	SIO_14	SIO_14	-	In	Pull-up	J6	P0.14	**Laird Connectivity BL653 Devkit:** LED2
28	SIO_17	SIO_17	-	In	Pull-up	J5	P0.17	-
29	SIO_12	SIO_12	-	In	Pull-up	H6	P0.12/ TRACEDATA1	-
30	VDD_NRF_1	-	-	-	-	J1, J4	VDD	1.7V to 3.6V
31	SWDCLK	SWDCLK	-	In	Pull-down	H2	SWDCLK	-
32	NFC1/ SIO_09	NFC1	SIO_09	In	-	F2	P0.09/NFC1	-
33	NFC2/ SIO_10	NFC2	SIO_10	In	-	E2	P0.10/NFC2	-
34	SIO_35/ nAutoRUN	nAutoRUN	SIO_35	In	Pull-down	F3	P1.01	**Laird Connectivity BL653 Devkit:** FTDI USB_DTR via jumper on J12 pin 1-2
35	SIO_16	SIO_16	-	In	Pull-up	G6	P0.16	**Laird Connectivity BL653 Devkit:** LED4
36	SIO_28/ AIN4	SIO_28	AIN4	In	Pull-up	C7	P0.28/AIN4	-

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Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull-Up/ Down	nRF52833 WLCSP Pin	nRF52833 WLCSP Name	Comment
37	SIO_02/ AIN0	SIO_02	AIN0	IN	Pull-down	C6	P0.02/AIN0	Pull High externally to enter VSP (Virtual Serial Port) Service.
38	SIO_30/ AIN6	SIO_30	AIN6	In	Pull-up	B5	P0.30/AIN6	-
39	SIO_29/ AIN5	SIO_29	AIN5	In	Pull-up	A5	P0.29/AIN5	-
40	SIO_27/ I2C_SCL	SIO_27	I2C_SCL	In	Pull-up	C8	P0.27	**Laird Connectivity BL653 Devkit:** I2C RTC chip I2C clock line
41	SIO_00/ XL1	SIO_00	XL1	In	Pull-up	B8	P0.00/XL1	**Laird Connectivity BL653 Devkit:** Optional 32.768kHz crystal pad XL1 and associated load capacitor
42	SIO_06/ UART_TX	SIO_06	UART_TX	Out	Set High in FW	E9	P0.06	UARTCLOSE() selects DIO functionality UARTOPEN() selects UART COMMS behaviour
43	SIO_04/ AIN2/ SPI_MISO	SIO_04	AIN2/ SPI_MISO	In	Pull-up	D8	P0.04/AIN2	**Laird Connectivity BL653 Devkit:** SPI EEPROM. SPI_Eeprom_MISO, Input SPIOPEN() in *smart*BASIC selects SPI function; MOSI and CLK are outputs when in SPI master mode
44	SIO_05/ UART_RTS/ AIN3	SIO_05	UART_RTS/ AIN3	Out	Set Low in FW	D9	P0.05/AIN3	UARTCLOSE() selects DIO functionality UARTOPEN() selects UART COMMS behavior
45	SIO_26/ I2C_SDA	SIO_26	I2C_SDA	In	Pull-up	C9	P0.26	**Laird Connectivity BL653 Devkit:** I2C RTC chip I2C data line
46	SIO_13	SIO_13	-	In	Pull-up	F7	P0.13	**Laird Connectivity BL653 Devkit:** LED1

Pin #	Pin Name	Default Function	Alternate Function	In/ Out	Pull-Up/ Down	nRF52833 WLCSP Pin	nRF52833 WLCSP Name	Comment
47	SIO_41/ SPI_CLK	SIO_41	SPI_CLK	In	Pull-up	F8	P1.09/ TRACEDATA3	**Laird Connectivity BL653 Devkit:** SPI EEPROM. SPI_Eeprom_CLK, Output: SPIOPEN() in *smart*BASIC selects SPI function, MOSI and CLK are outputs when in SPI master mode.
48	GND	-	-	-	-	-	VSS	-
49	D-	D-	-	In		H7	D-	-
50	SIO_15	SIO_15	-	In	Pull-up	H5	P0.15	**Laird Connectivity BL653 Devkit:** LED3
51	SIO_32	SIO_32	-	In	Pull-up	H3	P1.00/ TRACEDATA0	-
52	SWDIO	SWDIO	-	In	Pull-up	J2	SWDIO	-
G1	GND	-	-	-	-		VSS	BL653u GND paddle
G2	GND	-	-	-	-	-	-	G2 GND pad present on 453-00059 BL653µ Integrated Antenna module variant only.
G3	GND	-	-	-	-	-	-	G3 GND pad present on 453-00059 BL653µ Integrated Antenna module variant only.
G4	GND	-	-	-	-	-	-	G4 GND pad present on 453-00059 BL653µ Integrated Antenna module variant only.
G5	GND	-	-	-	-	-	-	G5 GND pad present on 453-00059 BL653µ Integrated Antenna module variant only.
G6	GND	-	-	-	-	-	-	G6 GND pad present on 453-00059 BL653µ Integrated Antenna module variant only.
G7	GND	-	-	-	-	-	-	G7 GND pad present on 453-00059 BL653µ Integrated Antenna module variant only.

Pin Definition Notes:

Note 1	SIO = Signal Input or Output. Secondary function is selectable in *smart*BASIC application or via Nordic SDK. I/O voltage level tracks VDD. AIN = Analog Input.
Note 2	At reset, all SIO lines are configured as the defaults shown above.

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Pin Definition Notes:

	SIO lines can be configured through the *smart*BASIC application script to be either inputs or outputs with pull-ups or pull-downs. When an alternative SIO function is selected (such as I2C or SPI), the firmware does not allow the setup of internal pull-up/pull-down. Therefore, when I2C interface is selected, pull-up resistors on I2C SDA and I2C SCL ***must*** be connected externally as per I2C standard.
Note 3	JTAG (two-wire SWD interface), pin 52 (SWDIO) and pin 31 (SWDCLK). JTAG is required because Nordic SDK applications can only be loaded using JTAG (*smart*BASIC firmware can be loaded using the JTAG as well as UART). We recommend that you use JTAG (2-wire interface) to handle future BL653µ module *smart*BASIC firmware upgrades. You MUST wire out the JTAG (2-wire interface) on your host design (see Figure 8, where four lines (SWDIO, SWDCLK, GND and VDD) should be wired out. *smart*BASIC firmware upgrades can still be performed over the BL653µ UART interface, but this is slower (60 seconds using UART vs. 10 seconds when using JTAG) than using the BL653µ JTAG (2-wire interface). Upgrading *smart*BASIC firmware or loading the *smart*BASIC applications is done using the UART interface.
Note 4	Pull the nRESET pin (pin 6) low for minimum 100 milliseconds to reset the BL653µ.
Note 5	The SIO_02 pin (pin 37) must be pulled high externally to enable VSP (Virtual Serial Port) which would allow OTA (over-the-air) *smart*BASIC application download. Refer to the latest firmware release documentation for details.
Note 6	Ensure that SIO_02 (pin 37) and AutoRUN (pin 34) are ***not both high*** (externally), in that state, the UART is bridged to Virtual Serial Port service; the BL653µ module does not respond to AT commands and cannot load *smart*BASIC application scripts.
Note 7	Pin 34 (nAutoRUN) is an input, with active low logic. In the development kit it is connected so that the state is driven by the host's DTR output line. The nAutoRUN pin must be externally held high or low to select between the following two BL653µ operating modes: ▪ Self-contained Run mode (nAutoRUN pin held at 0V –this is the default (internal pull-down enabled)) ▪ Interactive/Development mode (nAutoRUN pin held at VDD) The *smart*BASIC firmware checks for the status of nAutoRUN during power-up or reset. If it is low and if there is a *smart*BASIC application script named **$autorun$**, then the *smart*BASIC firmware executes the application script automatically; hence the name S*elf-contained Run Mode*.
Note 8	The *smartBASIC* firmware has SIO pins as Digital (Default Function) INPUT pins, which are set PULL-UP by default. This avoids floating inputs (which can cause current consumption to drive with time in low power modes (such as Standby Doze). You can disable the PULL-UP through your *smart*BASIC application. All of the SIO pins (with a default function of DIO) are inputs (apart from SIO_05 and SIO_06, which are outputs): ▪ SIO_06 (alternative function UART_TX) is an output, set High (in the firmware). ▪ SIO_05 (alternative function UART_RTS) is an output, set Low (in the firmware). ▪ SIO_08 (alternative function UART_RX) is an input, set with internal pull-up (in the firmware). ▪ SIO_07 (alternative function UART_CTS) is an input, set with internal pull-down (in the firmware). ▪ SIO_02 is an input set with internal pull-down (in the firmware). It is used for OTA downloading of *smart*BASIC applications. Refer to the latest firmware extension documentation for details. ▪ UART_RX, UART_TX, and UART_CTS are 3.3 V level logic (if VDD_NRF is 3.3 V; such as SIO pin I/O levels track VDD). For example, when Rx and Tx are idle, they sit at 3.3 V (if VDD_NRF is 3.3 V). Conversely, handshaking pins CTS and RTS at 0V are treated as assertions.
Note 9	Not required for BL653µ module normal operation. The on-chip 32.768kHz LFRC oscillator provides the standard accuracy of ±500 ppm, with calibration required every 8seconds (default) to stay within ±500 ppm. BL653µ also allows as an option to connect an external higher accuracy (±20 ppm) 32.768 kHz crystal to the BL653µ pins SIO_01/XL2/P0.01 (pin 13) and SIO_00/XL1/P0.00 (pin 41). This provides higher accuracy protocol timing and helps with radio power consumption in the system standby doze/deep sleep modes by reducing the time that the Rx window must be open.

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Pin Definition Notes:

Note 10	BL653µ power supply pin VDD_NRF_1 (pin30) MUST be connected to VDD_NRF(pin21) on customers design. BL653µ power supply pin VDD_NRF_1 (pin30) MUST have decoupling capacitor 100nF minimum connected (16V rating, X7R) placed next to VDD_NRF_1 (pin30). The two points above apply whether option 1 or option 2 below is used. BL653µ power supply options: ▪ **Option 1** – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD_NRF(and VDD_NRF1) and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 1.7V to 3.6V range to BL653µ VDD_NRF (and VDD_NRF1) and VDD_HV pins. OR ▪ **Option 2** – High voltage mode power supply mode (using BL653µ VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD_NRF pin is not connected to any external voltage supply. Connect external supply within range 2.5V to 5.5V range to BL653µ VDD_HV pin. BL653µ VDD_NRF pin left unconnected. No external current draw (from VDD_NRF pin) is allowed when using High Voltage mode (VDD_HV) (limitation of nRF52833 chipset). For either option, if you use USB interface then the BL653µ VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the BL653µ VBUS pin, you MUST externally fit a 4.7uF to ground.
Note 11	RF_pad (pin2) is for the BL653µ RF pad variant (453-00060) module only. If using the BL653µ module RF pad variant (453-00060), customer MUST copy the 50-Ohms GCPW RF track design, MUST add series 2nH RF inductor (Murata LQG15HN2N0B02# or Murata LQG15HS2N0B02) and RF connector IPEX MHF4 Receptacle (MPN: 20449-001E) Detailed in the following section: 6.4 - 50-Ohms RF Trace and RF Match Series 2nH RF Inductor on Host PCB for BL653µ RF Pad Variant (453-00060)
Note 12	BL653µ and BL653 modules have same GPIO mapping of Laird SIO_number to Nordic nRF52833 chipset PIO_number, hence smartBASIC applications developed on BL653 will operate on BL653µ. Due to BL653µ smaller size, the BL653µ has fewer GPIO's brought out than BL653. Compared to BL653, the BL653µ does not have the below 10 signals brought out:-

BL653 pin name (SmartBASIC BL653 FW) NOT brought out on BL653µ	nRF52833-CJAA chipset pin name NOT brought out on BL653µ
SIO_36	P1.04
SIO_34	P1.02
SIO_21	P0.21
SIO_20	P0.20
SIO_46	P1.03
SIO_47	P0.19
SIO_45	P1.05
SIO_42	P0.25
SIO_38	P1.06
SIO_39	P1.07

There is no Laird Connectivity development board for the BL653µ. Customer can develop their smartBASIC application script using Laird development board DVK-BL653 and that smartBASIC application script would run on BL653µ module (sitting on customers host board) and above table helps avoid those BL653 pins not available on BL653µ.

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3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed in the following table; exceeding these values causes permanent damage.

Table 3: Maximum current ratings

Parameter	Min	Max	Unit
Voltage at VDD_NRF (and VDD_NRF_1 pin)	-0.3	+3.9 (Note 1)	V
Voltage at VDD_HV pin	-0.3	+5.8	V
VBUS	-0.3	+5.8	V
Voltage at GND pin		0	V
Voltage at SIO pin (at VDD≤3.6V)	-0.3	VDD +0.3	V
Voltage at SIO pin (at VDD≥3.6V)	-0.3	3.9	V
NFC antenna pin current (NFC1/2)	-	80	mA
Radio RF input level	-	10	dBm
Environmental			
Storage temperature	-40	+85	ºC
MSL (Moisture Sensitivity Level)	-	4	-
ESD (as per EN301-489) Conductive Air Coupling		 4 8	 KV KV
Flash Memory (Endurance) (Note 2)	-	10000	Write/erase cycles
Flash Memory (Retention) at 85°C	10	-	years
Flash Memory (Retention) at 105°C (Limited to 1000 write /read cycles)	3		years
Flash Memory (Retention) at 105°C to 85°C, execution split (Limited to 1000 write /read cycles, 75% execution time at 85°C or less)	6.7		years
Thermal characteristics (Junction temperature)		110	ºC

Maximum Ratings Notes:

Note 1	The absolute maximum rating for VDD_NRF pin (max) is 3.9V for the BL653µ.
Note 2	Wear levelling is used in file system.

3.3.2 Recommended Operating Parameters

Table 4: Power supply operating parameters

Parameter	Min	Typ	Max	Unit
VDD_NRF and VDD_NRF_1 (independent of DCDC enable)[1,4] supply range	1.7	3.3	3.6	V
VDD_{POR} supply voltage needed during power on reset	1.75			V
VDD_HV supply range[4]	2.5	3.7	5.5	V
VBUS USB supply range	4.35	5	5.5	V
VDD Maximum ripple or noise[2]	-	-	10	mV
VDD supply rise time (0V to 1.7V)[3]	-	-	60	mS
VDD_HV supply rise time (0V to 3.7V) [3]			100	mS
Operating temperature range	-40	-	+85	ºC
Extended operating temperature range[5]	+85		+105	ºC

Recommended Operating Parameters Notes:

Note 1	4.7 uF internal to module on VDD. The VDD_NRF internal DCDC (REG1) convertor or LDO (REG1) is decided by the underlying Bluetooth LE stack depending on the load current. Through a smartBASIC command can also tell softdevice to use DCDC always or LDO always.
Note 2	This is the maximum VDD or VDD_HV ripple or noise (at any frequency) that does not disturb the radio.
Note 3	The on-board power-on reset circuitry may not function properly for rise times longer than the specified maximum.
Note 4	BL653µ power supply pin VDD_NRF_1 (pin30) MUST be connected to VDD_NRF(pin21) on customers design. BL653µ power supply pin VDD_NRF_1 (pin30) MUST have decoupling capacitor 100nF minimum connected (16V rating, X7R) placed next to VDD_NRF_1 (pin30). The two points above apply whether option 1 or option 2 below is used. BL653µ power supply options: ▪ **Option 1** – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD_NRF(and VDD_NRF1) and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 1.7V to 3.6V range to BL653µ VDD_NRF (and VDD_NRF1) and VDD_HV pins. OR ▪ **Option 2** – High voltage mode power supply mode (using BL653µ VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD_NRF pin is not connected to any external voltage supply. Connect external supply within range 2.5V to 5.5V range to BL653µ VDD_HV pin. BL653µ VDD_NRF pin left unconnected. No external current draw (from VDD_NRF pin) is allowed when using High Voltage mode (VDD_HV) (limitation of nRF52833 chipset). For either option, if you use USB interface then the BL653µ VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the BL653µ VBUS pin, you MUST externally fit a 4.7uF to ground.
Note 5	To avoid surpassing the maximum die temperature (110 ºC), it is important to minimize current consumption when operating in the extended operating temperature conditions (+85 ºC to +105ºC). It is therefore recommended to use the module device on Normal Voltage mode with DCDC (REG1) enabled.

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Table 5: Signal levels for interface, SIO

Parameter	Min	Typ	Max	Unit
V_{IH} Input high voltage	0.7 VDD		VDD	V
V_{IL} Input low voltage	VSS		0.3 x VDD	V
V_{OH} Output high voltage				
(std. drive, 0.5mA) (Note 1)	VDD -0.4		VDD	V
(high-drive, 3mA) (Note 1)	VDD -0.4		VDD	V
(high-drive, 5mA) (Note 2)	VDD -0.4		VDD	
V_{OL} Output low voltage				
(std. drive, 0.5mA) (Note 1)	VSS		VSS+0.4	V
(high-drive, 3mA) (Note 1)	VSS		VSS+0.4	V
(high-drive, 5mA) (Note 2)	VSS		VSS+0.4	
V_{OL} Current at VSS+0.4V, Output set low				
(std. drive, 0.5mA) (Note 1)	1	2	4	mA
(high-drive, 3mA) (Note 1)	3	-	-	mA
(high-drive, 5mA) (Note 2)	6	10	15	mA
V_{OL} Current at VDD -0.4, Output set low				
(std. drive, 0.5mA) (Note 1)	1	2	4	mA
(high-drive, 3mA) (Note 1)	3	-	-	mA
(high-drive, 5mA) (Note 2)	6	9	14	mA
Pull up resistance	11	13	16	kΩ
Pull down resistance	11	13	16	kΩ
Pad capacitance		3		pF
Pad capacitance at NFC pads		4		pF

Signal Levels Notes:

Note 1	For VDD_NRF≥1.7V. The firmware supports high drive (3 mA, as well as standard drive).
Note 2	For VDD_NRF (and VDD_NRF_1) ≥2.7V. The firmware supports high drive (5 mA (since VDD≥2.7V), as well as standard drive). The GPIO (SIO) high reference voltage always equals the level on the **VDD_NRF** pin. ▪ Normal voltage mode – The GPIO high level equals the voltage supplied to the VDD_NRF (and VDD_NRF_1) pin. ▪ High voltage mode – The GPIO high level equals the level specified (is configurable to 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. The default voltage is 1.8V). In High voltage mode, the VDD_NRF pin becomes an output voltage pin. The VDD_NRF output voltage and hence the GPIO is configurable from 1.8V to 3.3V with possible settings of 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V.

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Table 6: SIO pin alternative function AIN (ADC) specification

Parameter		Min	Typ	Max	Unit
Maximum sample rate				**200**	**kHz**
ADC Internal reference voltage		-1.5%	0.6 V	+1.5%	%
ADC pin input internal selectable scaling			4, 2, 1, 1/2, 1/3, 1/4, 1/5 1/6		scaling
ADC input pin (AIN) voltage maximum without damaging ADC w.r.t (see Note 1) VCC 0V-VDD_NRF	 Prescaling 4, 2, 1, ½, 1/3, ¼, 1/5, 1/6		VDD_NRF+0.3		V
Configurable Resolution		8-bit mode	10-bit mode	12-bit mode	bits
Configurable (see Note 2) Acquisition Time, source resistance ≤10kΩ Acquisition Time, source resistance ≤40kΩ Acquisition Time, source resistance ≤100kΩ Acquisition Time, source resistance ≤200kΩ Acquisition Time, source resistance ≤400kΩ Acquisition Time, source resistance ≤800kΩ			 3 5 10 15 20 40		 uS uS uS uS uS uS
Conversion Time (see Note 3)			<2		uS
ADC input impedance (during operation) (see Note 3) Input Resistance Sample and hold capacitance at maximum gain			 >1 2.5		 MOhm pF

Recommended Operating Parameters Notes:

Note 1	Stay within internal 0.6 V reference voltage with given pre-scaling on AIN pin and do not violate ADC maximum input voltage (for damage) for a given VCC, e.g. If VDD_NRF is 3.6V, you can only expose AIN pin to VDD_NRF+0.3 V. Default pre-scaling is 1/6 which configurable via smartBASIC.
Note 2	Firmware allows configurable resolution (8-bit, 10-bit or 12-bit mode) and acquisition time. BL653µ ADC is a Successive Approximation type ADC (SSADC), as a result no external capacitor is needed for ADC operation. Configure the acquisition time according to the source resistance that customer has. The sampling frequency is limited by the sum of sampling time and acquisition time. The maximum sampling time is 2us. For acquisition time of 3us the total conversion time is therefore 5us, which makes maximum sampling frequency of 1/5us = 200kHz. Similarly, if acquisition time of 40us chosen, then the conversion time is 42us and the maximum sampling frequency is 1/42us = 23.8kHz.
Note 3	ADC input impedance is estimated mean impedance of the ADC (AIN) pins.

3.4 Programmability

3.4.1 BL653µ Default Firmware

The BL653µ module comes loaded with *smart*BASIC firmware but does not come loaded with any *smart*BASIC application script (as that is dependent on customer-end application or use). Laird Connectivity provides many sample *smart*BASIC application scripts via a sample application folder on GitHub – https://github.com/LairdCP/BL653-Applications

Therefore, it boots into AT command mode by default.

3.4.2 BL653µ Special Function Pins in *smart*BASIC

Refer to the *smart*BASIC extension manual for details of functionality connected to this:

- nAutoRUN pin (SIO_35), see Table 7 for default
- VSP pin (SIO_02), see Table 8 for default

Table 7: nAutoRUN pin

Signal Name	Pin #	I/O	Comments
nAutoRUN /(SIO_35)	34	I	Input with active low logic. Internal pull down (default). Operating mode selected by nAutoRun pin status: ▪ Self-contained Run mode (nAutoRUN pin held at 0V) ▪ If Low (0V), runs $autorun$ if it exists ▪ Interactive/Development mode (nAutoRUN pin held at VCC) ▪ If High (VCC), runs via AT+rRUN (and file name of application)

In the development board nAutoRUN pin is connected so that the state is driven by the host's DTR output line.

Table 8: VSP mode

Signal Name	Pin #	I/O	Comments
SIO_02	37	I	Internal pull down (default). VSP mode selected by externally pulling-up SIO_02 pin: **High (VCC),** then OTA *smart*BASIC application download is possible.

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4 Power Consumption

Data at VDD_NRF (and VDD_NRF_1) of 3.3 V with internal (to chipset) LDO(REG1) ON, or with internal (to chipset) DCDC(REG1) ON (see Power Consumption Note 1) and 25°C.

4.1 Power Consumption

Table 9: Power consumption

Parameter	Min	Typ	Max	Unit
Active mode 'peak' current (Note 1)		With DCDC [with LDO]		
(Advertising or Connection)				
Tx only run peak current @ Txpwr = +8 dBm		14.2 [30.4]		mA
Tx only run peak current @ Txpwr = +4 dBm		9.6 [20.7]		mA
Tx only run peak current @ Txpwr = 0 dBm		4.9 [10.3]		mA
Tx only run peak current @ Txpwr = -4 dBm		3.8 [8.0]		mA
Tx only run peak current @ Txpwr = -8 dBm		3.4 [7.1]		mA
Tx only run peak current @ Txpwr = -12 dBm		3.1 [6.4]		mA
Tx only run peak current @ Txpwr = -16 dBm		2.9 [5.9]		mA
Tx only run peak current @ Txpwr = -20 dBm		2.7 [5.5]		mA
Tx only run peak current @ Txpwr = -40 dBm		2.3 [4.5]		mA
Active Mode				
Rx only 'peak' current, Bluetooth LE 1Mbps (Note 1)		4.6 [9.6]		mA
Rx only 'peak' current, Bluetooth LE 2Mbps (Note 2)		5.2 [10.7]		mA
Ultra-Low Power Mode 1 (Note 2)		2.6		uA
Standby Doze, 256k RAM retention				
Ultra-Low Power Mode 2 (Note 3)		0.6		uA
Deep Sleep (no RAM retention)				
Active Mode Average current (Note 4)				
Advertising Average Current draw				
Max, with advertising interval (min) 20 mS		Note 4		uA
Min, with advertising interval (max) 10240 mS		Note 4		uA
Connection Average Current draw				
Max, with connection interval (min) 7.5 mS		Note 4		uA
Min, with connection interval (max) 4000 mS		Note4		uA

Power Consumption Notes:

Note 1	This is for Peak Radio Current only, but there is additional current due to the MCU. The internal DCDC convertor (REG1) or LDO (REG1) is decided by the underlying Bluetooth LE stack.
Note 2	BL653µ modules Standby Doze is 2.6 uA typical. When using smartBASIC firmware, Standby Doze is entered automatically (when a waitevent statement is encountered within a smartBASIC application script). In Standby Doze, all peripherals that are enabled stay on and may re-awaken the chip. Depending on active peripherals, current consumption ranges from 2.6 µA to 370 uA (when UART is ON). See individual peripherals current consumption data in the Peripheral Block Current Consumption section. smartBASIC firmware has functionality to detect GPIO change with no current consumption cost, it is possible to close the UART and get to the 2.6 uA current consumption regime and still be able to detect for incoming data and be woken up so that the UART can be re-opened at expense of losing that first character. The BL653µ Standby Doze current (at 25°C) consists of the below nRF52833 blocks:

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Power Consumption Notes:

	▪ nRF52 System ON IDLE current (no RAM retention) (1.1 uA) – This is the base current of the CPU ▪ LFRC (0.7 uA) and RTC (0.1uA or near 0uA) running as well as 128k RAM retention (0.8 uA) – This adds to the total of 2.7 uA typical. The RAM retention is 20nA per 4k block, but this can vary to 30nA per 4k block which would make the total 2.55uA to 2.86uA.
Note 3	In Deep Sleep, everything is disabled and the only wake-up sources (including NFC to wakeup) are reset and changes on SIO or NFC pins on which sense is enabled. The current consumption seen is ~0.6 uA typical in BL653µ modules. ▪ Coming out from Deep Sleep to Standby Doze through the reset vector.
Note 4	Average current consumption depends on several factors (including Tx power, VCC, accuracy of 32MHz and 32.768 kHz). With these factors fixed, the largest variable is the advertising or connection interval set. Advertising Interval range: ▪ 20 milliseconds to 10240 mS (10485759.375 mS in BT5.1) in multiples of 0.625 milliseconds. For an advertising event: ▪ The minimum average current consumption is when the advertising interval is large 10240 mS (10485759.375 mS (in BT5.0) although this may cause long discover times (for the advertising event) by scanners ▪ The maximum average current consumption is when the advertising interval is small 20 mS ▪ Other factors that are also related to average current consumption include the advertising payload bytes in each advertising packet and whether it's continuously advertising or periodically advertising. Connection Interval range (for a peripheral): ▪ 7.5 milliseconds to 4000 milliseconds in multiples of 1.25 milliseconds. For a connection event (for a peripheral device): ▪ The minimum average current consumption is when the connection interval is large 4000 milliseconds ▪ The maximum average current consumption is with the shortest connection interval of 7.5 ms; no slave latency. Other factors that are also related to average current consumption include: ▪ Number packets per connection interval with each packet payload size ▪ An inaccurate 32.768 kHz master clock accuracy would increase the average current consumption. Connection Interval range (for a central device): ▪ 2.5 milliseconds to 40959375 milliseconds in multiples of 1.25 milliseconds.

4.2 Peripheral Block Current Consumption

The values below are calculated for a typical operating voltage of 3V.

Table 10: UART power consumption

Parameter	Min	Typ		Max	Unit
		WITH DCDC(REG1)	WITH LDO(REG1)		
UART Run current @ 115200 bps	-	450	721	-	uA
UART Run current @ 1200 bps	-	450	721	-	uA
Idle current for UART (no activity)	-	2.9	2.9	-	uA
UART Baud rate	1.2	-		1000	kbps

Table 11: SPI power consumption

Parameter	Min	Typ		Max	Unit
		WITH DCDC(REG1)	WITH LDO(REG1)		

SPI Master Run current @ 2 Mbps	-	536	803	-	uA
SPI Master Run current @ 8 Mbps	-	536	803	-	uA
Idle current for SPI (no activity)	-	<1	<1	-	uA
SPI bit rate	-	-		8	Mbps

Table 12: I2C power consumption

Parameter	Min	Typ		Max	Unit
		WITH DCDC(REG1)	WITH LDO(REG1)		
I2C Run current @ 100 kbps	-	734	994	-	uA
I2C Run current @ 400 kbps	-	734	994	-	uA
Idle current for I2C (no activity)	-	2.5	2.5	-	uA
I2C Bit rate	100	-		400	kbps

Table 13: ADC power consumption

Parameter	Min	Typ		Max	Unit
		WITH DCDC(REG1)	WITH LDO(REG1)		
ADC current during conversion	-	1900	1350	-	uA
Idle current	-	0	0	-	uA

The above current consumption is for the given peripheral including the internal blocks that are needed for that peripheral for both the case when DCDC(REG1) is on and LDO (REG1) is on. The peripheral Idle current is when the peripheral is enabled but not running (not sending data or being used) and must be added to the StandByDoze current (Nordic System ON Idle current). In all cases radio is not turned on.

For asynchronous interface, like the UART (asynchronous as the other end can communicate at any time), the UART on the BL653µ must be kept open (by a command in *smart*BASIC application script), resulting in the base current consumption penalty.

For a synchronous interface like the I2C or SPI (since BL653µ side is the master), the interface can be closed and opened (by a command in *smart*BASIC application script) only when needed, resulting in current saving (no base current consumption penalty). There's a similar argument for ADC (open ADC when needed).

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Functional Description

To provide the widest scope for integration, a variety of physical host interfaces/sensors are provided. The major BL653µ series module functional blocks described below.

5.1 Power Management

5 Power management features:

- System Standby Doze and Deep Sleep modes
- Open/Close peripherals (UART, SPI, I2C, SIO's, ADC, NFC). Peripherals consume current when open; each peripheral can be individually closed to save power consumption
- Use of the internal DCDC (REG1) convertor or LDO (REG1) is decided by the underlying Bluetooth LE stack
- *smart*BASIC command allows the supply voltage to be read (through the internal ADC)
- Pin wake-up system from deep sleep (including from NFC pins)

Power supply features:

- Supervisor hardware to manage power during reset, brownout, or power fail.
- 1.7V to 3.6V supply range for normal power supply (VDD_NRF) using internal DCDC convertor (REG1) or LDO(REG1) decided by the underlying Bluetooth LE stack.
- 2.5V to 5.5 supply range for High voltage power supply (VDD_HV pin) using internal LDO(REG0).
- 4.35V to 5.5V supply range for powering USB (VBUS pin) portion of BL653µ only. The remainder of the BL653µ module circuitry must still be powered through the VDD_NRF (or VDD_HV) pin.

5.2 BL653µ Power Supply Options

The BL653µ module power supply internally contains the following two main supply regulator stages (Figure 5):

- REG0 – Connected to the VDD_HV pin
- REG1 – Connected to the VDD_NRF pin (and VDD_NRF_1)

The USB power supply is separate (connected to the VBUS pin).

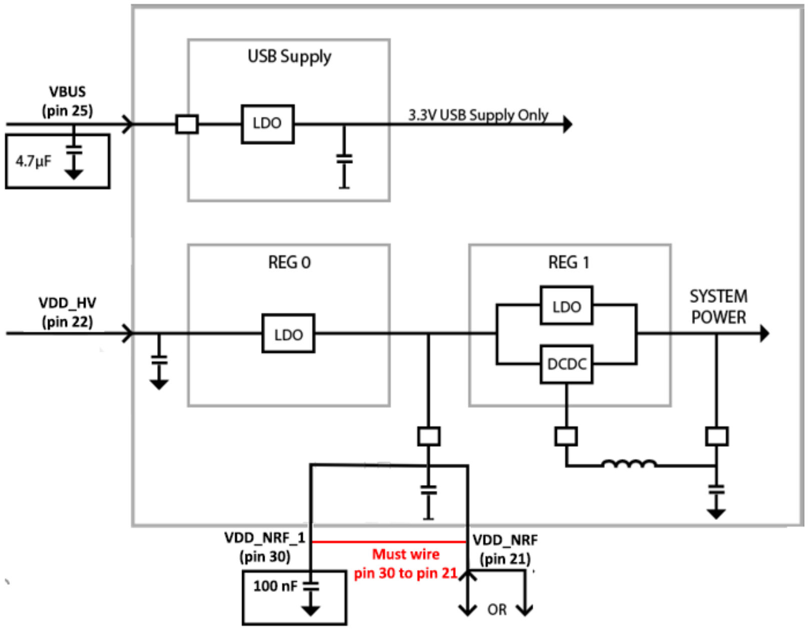

Figure 5: BL653µ power supply block diagram (adapted from the following resource: https://infocenter.nordicsemi.com/pdf/nRF52833_PS_v1.3.pdf

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The BL653µ power supply system enters one of two supply voltage modes, normal or high voltage mode, depending on how the external supply voltage is connected to these pins.

BL653µ power supply options:

- BL653µ power supply pin VDD_NRF_1 (pin 30) MUST be connected to VDD_NRF(pin 21) on customers design.
- BL653µ power supply pin VDD_NRF_1 (pin 30) MUST have decoupling capacitor 100nF minimum connected (16V rating, X7R) placed next to VDD_NRF_1 (pin 30).

The above two points apply whether option 1 or option 2 below is used.

- **Option 1** – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD_NRF(and VDD_NRF1) and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 1.7V to 3.6V range to BL653µ VDD_NRF (and VDD_NRF1) and VDD_HV pins.

  OR

- **Option 2** – High voltage mode power supply mode (using BL653µ VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD_NRF pin is not connected to any external voltage supply. Connect external supply within range 2.5V to 5.5V range to BL653µ VDD_HV pin. BL653µ VDD_NRF pin left unconnected.

  No external current draw (from VDD_NRF pin) is allowed when using High Voltage mode (VDD_HV) (limitation of nRF52833 chipset).

Note: To avoid surpassing the maximum die temperature (110 ºC), it is important to minimize current consumption when operating in the extended operating temperature conditions (+85 ºC to +105ºC). It is therefore recommended to use the module device on Normal Voltage mode with DCDC (REG1) enabled.

For either option, if you use USB interface then the BL653µ VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the BL653µ VBUS pin, you **MUST** externally fit a 4.7uF to ground.

Table 14 summarizes these power supply options.

Table 14: BL653µ powering options

Power Supply Pins and Operating Voltage Range	OPTION 1 Normal voltage mode operation connect?	OPTION 2 High voltage mode operation connect?	OPTION 1 with USB peripheral, and normal voltage mode operation connect?	OPTION 2 with USB peripheral, and high voltage operation connect?
VDD_NRF (pin21) 1.7V to 3.6V (Note 0)	Yes (Note 1)	No (Note 2)	Yes	No (Note 2)
VDD_HV (pin22) 2.5V to 5.5V	No	Yes	No	Yes (Note 5)
VBUS (pin25) 4.35V to 5.5V	No	(Note 3)	Yes (Note 4)	Yes (Note 4)

Power Supply Option Notes:

Note 0	▪ BL653µ power supply pin VDD_NRF_1 (pin 30) MUST be connected to VDD_NRF(pin 21) on customers design. ▪ BL653µ power supply pin VDD_NRF_1 (pin 30) MUST have decoupling capacitor 100nF minimum connected (16V rating, X7R) placed next to VDD_NRF_1 (pin 30). The above two points apply whether option 1 or option 2 below is used.
Note 1	**Option 1 –** External supply voltage is connected to BOTH the VDD_NRF and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within range 1.7V to 3.6V range to BOTH BL653µ VDD and VDD_HV pins.

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Power Supply Option Notes:

Note 2	**Option 2 –** External supply within range 2.5V to 5.5V range to the BL653µ VDD_HV pin ONLY. BL653µ VDD_NRF pin left unconnected. In High voltage mode, the VDD_NRF pin becomes an output voltage pin but no current can be taken from VDD pin (limitation of the nRF52833 chip). It Additionally, the VDD_NRF output voltage is configurable from 1.8V to 3.3V with possible settings of 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. The default voltage is 1.8V. The supported BL653µ VDD_NRF pin output voltage range depends on the supply voltage provided on the BL653µ VDD_HV pin. The minimum difference between voltage supplied on the VDD_HV pin and the voltage output on the VDD pin is 0.3 V. The maximum output voltage of the VDD_NRF pin is VDDH – 0.3V.
Note 3	Depends on whether USB operation is required
Note 4	When using the BL653µ **VBUS** pin, you **must** externally fit a 4.7uF capacitor to ground.
Note 5	To use the BL653µ USB peripheral: 1. Connect the BL653µ VBUS pin to the external supply within the range 4.35V to 5.5V. When using the BL653µ VBUS pin, you **MUST** externally fit a 4.7uF to ground. 2. Connect the external supply to either the VDD_NRF (Option 1) or VDD_HV (Option 2) pin to operate the rest of BL653µ module. When using the BL653µ USB peripheral, the VBUS pin can be supplied from same source as VDD_HV (within the operating voltage range of the VBUS pin and VDD_HV pin).

5.3 Clocks and Timers

5.3.1 Clocks

The integrated high accuracy 32 MHz (±10 ppm) crystal oscillator helps with radio operation and reducing power consumption in the active modes.

The integrated on-chip 32.768 kHz LFRC oscillator (±500 ppm) provides protocol timing and helps with radio power consumption in the system StandByDoze and Deep Sleep modes by reducing the time that the RX window needs to be open.

To keep the on-chip 32.768 kHz LFRC oscillator within ±500 ppm (which is needed to run the Bluetooth LE stack) accuracy, RC oscillator needs to be calibrated (which takes 33 mS) regularly. The default calibration interval is eight seconds which is enough to keep within ±500 ppm. The calibration interval ranges from 0.25 seconds to 31.75 seconds (in multiples of 0.25 seconds) and configurable via firmware

5.3.2 Timers

When using *smart*BASIC, the timer subsystem enables applications to be written which allow future events to be generated based on timeouts.

- **Regular Timer** – There are eight built-in timers (regular timers) derived from a single RTC clock which are controlled solely by smart BASIC functions. The resolution of the regular timer is 976 microseconds.
- **Tick Timer** – A 31-bit free running counter that increments every (1) millisecond. The resolution of this counter is 488 microseconds.

Refer to the *smartBASIC User Guide* available from the Laird Connectivity BL653µ product page. For timer utilization when using the Nordic SDK, refer to http://infocenter.nordicsemi.com/index.jsp.

5.4 Radio Frequency (RF)

- 2402–2480 MHz Bluetooth Low Energy radio BT5.1 – 1 Mbps, 2 Mbps, and long-range (125 kbps and 500 kbps) over-the-air data rate.
- Tx output power of +8 dBm programmable down to 7 dBm, 6 dBm, 5 dBm, 4 dBm, 2 dBm, 0 dBm and further down to -20 dBm in steps of 4 dB and final TX power level of -40 dBm.
- Receiver (with integrated channel filters) to achieve maximum sensitivity -96 dBm @1 Mbps BLE, -92 dBm @ 2 Mbps, -103 dBm@125 kbps long-range and -99 dBm@ 500 kbps long-range).

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- RF conducted interface available in the following two ways:
  - 453-00059: RF connected to on-board chip antenna
  - 453-00060: RF connected to RF pad on BL653µ
- Antenna options:
  - Integrated chip antenna on the 453-00059
  - External dipole antenna connected to IPEX MH4 RF connector on host PCB. If using the BL653µ module RF pad variant (453-00060), customer MUST copy the 50-Ohms GCPW RF track design, MUST add series 2nH RF inductor (Murata LQG15HN2N0B02# or Murata LQG15HS2N0B02) and RF connector IPEX MHF4 Receptacle (MPN: 20449-001E) Detailed in the following section: 6.4 50-Ohms RF Trace and RF Match Series 2nH RF Inductor on Host PCB for BL653µ RF Pad Variant (453-00060)
- Received Signal Strength Indicator (RSSI)
  - RSSI accuracy (valid range -90 to -20 dBm) is ±2 dB typical
  - RSSI resolution 1 dB typical

5.5 NFC

NFC support:

- Based on the NFC forum specification
  - 13.56 MHz
  - Date rate 106 kbps
  - NFC Type 2 and Type 4 tag emulation
- Modes of operation:
  - Disable
  - Sense
  - Activated

5.5.1 Use Cases

- Touch-to Pair with NFC
- Launch a smartphone app (on Android)
- NFC enabled Out-of-Band Pairing
- System Wake-On-Field function
  - Proximity Detection

Table 15: NFC interface

Signal Name	Pin No	I/O	Comments
NFC1/SIO_09/P0.09	32	I/O	The NFC pins are by default NFC pins and an alternate function on each pin is GPIO. Refer to the *smart*BASIC. User manual.
NFC2/SIO_10/P0.10	33	I/O	

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5.5.2 NFC Antenna Coil Tuning Capacitors

From Nordic's *nRF52833* Objective *Product Specification v1.0*: http://infocenter.nordicsemi.com/pdf/nRF52833_PS_v1.0.pdf

The NFC antenna coil must be the connected differential between the NFC1 and NFC2 pins of the BL653µ. Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz (Figure 6).

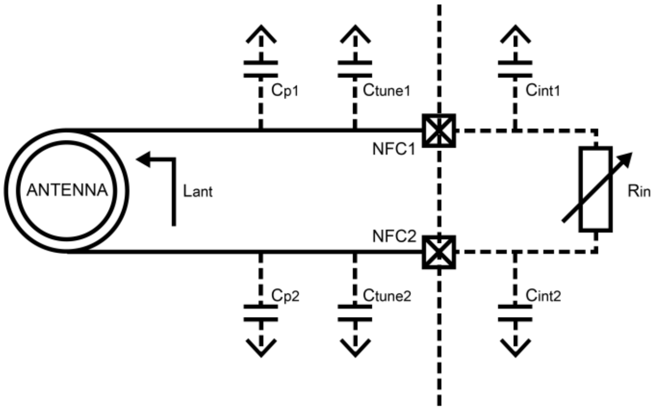

Figure 6: NFC antenna coil tuning capacitors

The required external tuning capacitor value is given by the following equations:

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} - C_p - C_{int}$$

An antenna inductance of Lant = 0.72 uH provides tuning capacitors in the range of 300 pF on each pin. The total capacitance on NFC1 and NFC2 must be matched. Cint and Cp are small usually (Cint is 4pF), so can omit from calculation.

Battery Protection Note: If the NFC coil antenna is exposed to a strong NFC field, the supply current may flow in the opposite direction due to parasitic diodes and ESD structures.

If the used battery does not tolerate a return current, a series diode must be placed between the battery and the BL653µ to protect the battery.

5.6 UART Interface

Note: The BL653µ has two UARTs.

The Universal Asynchronous Receiver/Transmitter (UART) offers fast, full-duplex, asynchronous serial communication with built-in flow control support (UART_CTS, UART_RTS) in HW up to one Mbps baud. Parity checking and generation for the ninth data bit are supported.

UART_TX, UART_RX, UART_RTS, and UART_CTS form a conventional asynchronous serial data port with handshaking. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signaling levels are nominal 0 V and 3.3 V (tracks VDD) and are inverted with respect to the signaling on an RS232 cable.

Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and UART_CTS is an input. Both are active low.

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These signals operate according to normal industry convention. UART_RX, UART_TX, UART_CTS, UART_RTS are all 3.3 V level logic (tracks VDD_NRF). For example, when RX and TX are idle they sit at 3.3 V. Conversely for handshaking pins CTS, RTS at 0 V is treated as an assertion.

The module communicates with the customer application using the following signals:

- Port/TxD of the application sends data to the module's UART_RX signal line
- Port/RxD of the application receives data from the module's UART_TX signal line

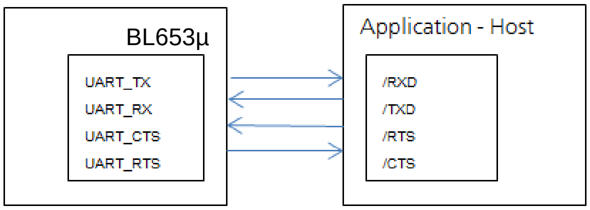

Figure 7: UART signals

Note: The BL653µ serial module output is at 3.3V CMOS logic levels (tracks VDD). Level conversion must be added to interface with an RS-232 level compliant interface.

Some serial implementations link CTS and RTS to remove the need for handshaking. We do not recommend linking CTS and RTS other than for testing and prototyping. If these pins are linked and the host sends data at the point that the BL653µ deasserts its RTS signal, there is significant risk that internal receive buffers will overflow, which could lead to an internal processor crash. This will drop the connection and may require a power cycle to reset the module. We recommend that the correct CTS/RTS handshaking protocol be adhered to for proper operation.

Table 16: UART interface

Signal Name	Pin No.	I/O	Comments
SIO_06 / UART_Tx/P0.06	42	O	SIO_06 (alternative function UART_Tx) is an output, set high (in firmware).
SIO_08 / UART_Rx/P0.08	14	I	SIO_08 (alternative function UART_Rx) is an input, set with internal pull-up (in firmware).
SIO_05 / UART_RTS/P0.05	44	O	SIO_05 (alternative function UART_RTS) is an output, set low (in firmware).
SIO_07 / UART_CTS//P0.07	15	I	SIO_07 (alternative function UART_CTS) is an input, set with internal pull-down (in firmware).

The UART interface is also used to load customer developed *smart*BASIC application script.

5.7 USB Interface

BL653µ has USB 2.0 FS (Full Speed, 12 Mbps) hardware capability. There is a CDC driver/Virtual UART as well as other USB drivers available via Nordic SDK – such as: usb_audio, usb_hid, usb_generic, usb_msc (mass storage device).

Table 17: USB interface

Signal Name	Pin No	I/O	Comments
D-	49	I/O	
D+	26	I/O	
VBUS	25		When using the BL653µ VBUS pin (which is mandatory when USB interface is used), Customer MUST connect externally a 4.7uF capacitor to ground. ***Note:*** *You MUST power the rest of BL653µ module circuitry through the VDD_NRF pin (OPTION1) or VDD_HV pin (OPTION2).*

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5.8 SPI Bus

The SPI interface is an alternate function on SIO pins.

The module is a master device that uses terminals SPI_MOSI, SPI_MISO, and SPI_CLK. SPI_CS is implemented using any spare SIO digital output pins to allow for multi-dropping.

The SPI interface enables full duplex synchronous communication between devices. It supports a three-wire (SPI_MOSI, SPI_MISO, SPI_SCK,) bidirectional bus with fast data transfers to and from multiple slaves. Individual chip select signals are necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of SIO signals. I/O data is double buffered.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

Table 18: SPI interfaces

Signal Name	Pin No	I/O	Comments
SIO_40/SPI_MOSI/P1.08	17	O	This interface is an alternate function configurable by *smart*BASIC. Default in the FW pin 56 and 53 are SIO inputs. SPIOPEN() in *smart*BASIC selects SPI function and changes pin 56 and 53 to outputs (when in SPI master mode).
SIO_04/AIN2/SPI_MISO/P0.04	43	I	
SIO_41/SPI_CLK/P1.09	47	O	
Any_SIO/SPI_CS	8	I	SPI_CS is implemented using any spare SIO digital output pins to allow for multi-dropping. On Laird Connectivity devboard SIO_44/P0.23 (pin8) used as SPI_CS.

5.9 I2C Interface

The I2C interface is an alternate function on SIO pins.

The two-wire interface can interface a bi-directional wired-OR bus with two lines (SCL, SDA) and has master /slave topology. The interface is capable of clock stretching. Data rates of 100 kbps and 400 kbps are supported.

An I2C interface allows multiple masters and slaves to communicate over a shared wired-OR type bus consisting of two lines which normally sit at VDD. The SCL is the clock line which is always sourced by the master and SDA is a bi-directional data line which can be driven by any device on the bus.

IMPORTANT: It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.

Table 19: I2C interface

Signal Name	Pin No	I/O	Comments
SIO_26/I2C_SDA/P0.26	45	I/O	This interface is an alternate function on each pin, configurable by *smart*BASIC. I2COPEN() in *smart*BASIC selects I2C function.
SIO_27/I2C_SCL/P0.27	40	I/O	

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5.10 General Purpose I/O, ADC, PWM, and FREQ

5.10.1 GPIO

The 42 SIO pins are configurable by *smart*BASIC application script or Nordic SDK. They can be accessed individually. Each has the following user configured features:

- Input/output direction
- Output drive strength (standard drive 0.5 mA or high drive 5mA)
- Internal pull-up and pull-down resistors (13 K Ohms typical) or no pull-up/down or input buffer disconnect
- Wake-up from high or low-level triggers on all pins including NFC pins

5.10.2 ADC

The ADC is an alternate function on SIO pins, configurable by *smart*BASIC or Nordic SDK.

The BL653µ provides access to 8-channel 8/10/12-bit successive approximation ADC in one-shot mode. This enables sampling up to 8 external signals through a front-end MUX. The ADC has configurable input and reference pre-scaling and sample resolution (8, 10, and 12 bit).

5.10.2.1 Analog Interface (ADC)

Table 20: Analog interface

Signal Name	Pin No	I/O	Comments
SIO_05/UART_RTS/AIN3/P0.05 – Analog Input	44	I	This interface is an alternate function on each pin, configurable by *smart*BASIC. AIN configuration selected using GpioSetFunc() function. Configurable 8, 10, 12-bit resolution. Configurable voltage scaling 4, 2, 1/1, 1/3, 1/3, 1/4, 1/5, 1/6(default). Configurable acquisition time 3uS, 5uS, 10uS(default), 15uS, 20uS, 40uS. Full scale input range (VDD_NRF)
SIO_04/AIN2/SPI_MISO/P0.04 – Analog Input	43	I	
SIO_03/AIN1/P0.03 – Analog Input	10	I	
SIO_02/AIN0/P0.02 – Analog Input	37	I	
SIO_31/AIN7/P0.31 – Analog Input	12	I	
SIO_30/AIN6/P0.30 – Analog Input	38	I	
SIO_29/AIN5/P0.29 – Analog Input	39	I	
SIO_28/AIN4/P0.28 – Analog Input	36	I	

5.10.3 PWM Signal Output on Up to 16 SIO Pins

The PWM output is an alternate function on ALL (GPIO) SIO pins, configurable by *smart*BASIC or the Nordic SDK.

The **PWM output** signal has a frequency and duty cycle property. Frequency is adjustable (up to 1 MHz) and the duty cycle can be set over a range from 0% to 100%.

PWM output signal has a frequency and duty cycle property. PWM output is generated using dedicated hardware in the chipset. There is a trade-off between PWM output frequency and resolution.

For example:

- PWM output frequency of 500 kHz (2 uS) results in resolution of 1:2
- PWM output frequency of 100 kHz (10 uS) results in resolution of 1:10
- PWM output frequency of 10 kHz (100 uS) results in resolution of 1:100
- PWM output frequency of 1 kHz (1000 uS) results in resolution of 1:1000

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5.10.4 FREQ Signal Output on Up to 16 SIO Pins

The FREQ output is an alternate function on 16 (GPIO) SIO pins, configurable by *smart*BASIC or Nordic SDK.

Note: The frequency driving each of the 16 SIO pins is the same but the duty cycle can be independently set for each pin.

FREQ output signal frequency can be set over a range of 0Hz to 4 MHz (with 50% mark-space ratio).

5.11 nRESET Pin

Table 21: nRESET pin

Signal Name	Pin No	I/O	Comments
nRESET	6	I	BL653µ HW reset (active low). Pull the nRESET pin low for minimum 100 mS for the BL653µ to reset.

5.12 Two-Wire Interface SWD (JTAG)

The BL653µ Firmware hex file consists of four elements:

- *smart*BASIC runtime engine
- Nordic Softdevice
- Master Bootloader

Laird Connectivity BL653µ *smart*BASIC firmware (FW) image part numbers are referenced as w.x.y.z (ex. V30.x.y.z). The BL653µ *smart*BASIC runtime engine and Softdevice combined image can be upgraded by the customer over the UART interface.

You also have the option to use the two-wire SWD (JTAG) interface, during production, to clone the file system of a Golden preconfigured BL653µ to others using the Flash Cloning process. This is described in the following application note *Flash Cloning for the BL653µ*. In this case the file system is also part of the .hex file.

Signal Name	Pin No	I/O	Comments
SWDIO	52	I/O	Internal pull-up resistor
SWDCLK	31	I	Internal pull-down resistor

The Laird Connectivity development board incorporates an on-board SWD (JTAG) J-link programmer for this purpose. There is also the following SWD (JTAG) connector which allows on-board SWD (JTAG) J-link programmer signals to be routed off the development board. The only requirement is that you should use the following SWD (JTAG) connector on the host PCB.

The SWD (JTAG) connector MPN is as follows:

Reference	Part	Description and MPN (Manufacturers Part Number)
JP1	FTSH-105	Header, 1.27mm, SMD, 10-way, FTSH-105-01-L-DV Samtech

Note: Reference on the BL653 development board schematic (Figure 8) shows the DVK development schematic wiring only for the SWD (JTAG) connector and the BL653µ module JTAG pins.

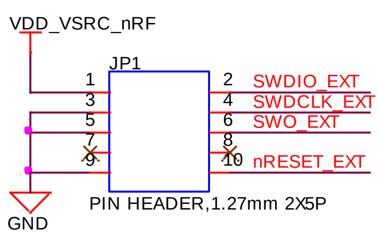

Figure 8: BL653µ development board schematic

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Note: The BL653µ is developed with the BL653 development board. The BL653 development board allows Laird Connectivity on-board SWD (JTAG) J-link programmer signals to be routed off the development board by from connector JP1

SWD (JTAG) is required because Nordic SDK applications can only be loaded using the SWED (JTAG) (*smart*BASIC firmware can be loaded using SWD (JTAG) as well as over the UART). We recommend that you use SWD (JTAG) (2-wire SWD interface) to handle future BL653µ module firmware upgrades. You **must** wire out the JTAG (2-wire SWD interface) on your host design (see Figure 8, where the following four lines should be wired out – SWDIO, SWDCLK, GND, and VCC). *smart*BASIC firmware upgrades can still be performed over the BL653µ UART interface, but this is slower than using the BL653µ JTAG (2-wire SWD interface) – (60 seconds using UART vs. 10 seconds when using JTAG).

5.13 BL653µ Wakeup

5.13.1 Waking Up BL653µ From Host

Wake the BL653µ from the host using wake-up pins (any SIO pin). You may configure the BL653µ's wakeup pins via *smart*BASIC to do any of the following:

- Wake up when signal is low
- Wake up when signal is high
- Wake up when signal changes

Refer to the *smart*BASIC user guide for details. You can access this guide from the Laird Connectivity BL653µ product page.

For BL653µ wake-up using the Nordic SDK, refer to Nordic infocenter.nordicsemi.com.

5.14 Low Power Modes

The BL653µ has three power modes: Run, Standby Doze, and Deep Sleep.

The module is placed automatically in Standby Doze if there are no pending events (when WAITEVENT statement is encountered within a customer's *smart*BASIC script). The module wakes from Standby Doze via any interrupt (such as a received character on the UART Rx line). If the module receives a UART character from either the external UART or the radio, it wakes up.

Deep sleep is the lowest power mode. Once awakened, the system goes through a system reset.

For different Nordic power modes using the Nordic SDK, refer to Nordic infocenter.nordicsemi.com.

5.15 Temperature Sensor

The on-silicon temperature sensor has a temperature range greater than or equal to the operating temperature of the device. Resolution is 0.25°C degrees. The on-silicon temperature sensor accuracy is ±5°C.

To read temperature from on-silicon temperature sensor (in tenth of centigrade, so 23.4°C is output as 234) using *smart*BASIC:

- In command mode, use **ATI2024**

  OR

- From running a *smart*BASIC application script, use **SYSINFO(2024)**

5.16 Security/Privacy

5.16.1 Random Number Generator

Exposed via an API in *smart*BASIC (see *smart*BASIC documentation available from the BL653µ product page). The **rand()** function from a running *smart*BASIC application returns a value.

For Nordic related functionality, visit Nordic infocenter.nordicsemi.com

5.16.2 AES Encryption/Decryption

Exposed via an API in *smart*BASIC (see *smart*BASIC documentation available from the BL653µ product page). Function called **aesencrypt** and **aesdecrypt**.

For Nordic related functionality, visit Nordic infocenter.nordicsemi.com

5.16.3 Readback Protection

The BL653µ supports readback protection capability that disallows the reading of the memory on the nRF52833 using a JTAG interface. Available via *smart*BASIC or the Nordic SDK.

5.16.4 Elliptic Curve Cryptography

The BL653µ offers a range of functions for generating public/private keypair, calculating a shared secret, as well as generating an authenticated hash. Available via *smart*BASIC or the Nordic SDK.

5.17 Optional External 32.768 kHz Crystal

This is not required for normal BL653µ module operation.

The BL653µ uses the on-chip 32.76 kHz RC oscillator (LFCLK) by default (which has an accuracy of ±500 ppm) which requires regulator calibration (every eight seconds) to within ±500 ppm.

You can connect an optional external high accuracy (±20 ppm) 32.768 kHz crystal (and associated load capacitors) to the BL653µSIO_01/XL2 (pin 41) and SIO_00/XL1 (pin 42) to provide improved protocol timing and to help with radio power consumption in the system standby doze/deep sleep modes by reducing the time that the RX window needs to be open. Table 22 compares the current consumption difference between RC and crystal oscillator.

Table 22: Comparing current consumption difference between BL653µ on-chip RC 32.76 kHz oscillator and optional external crystal (32.768kHz) based oscillator

	BL653µ On-chip 32.768 kHz RC Oscillator (±500 ppm) LFRC	Optional External Higher Accuracy (±20 ppm) 32.768 kHz Crystal-based Oscillator LFXO
Current Consumption of 32.768 kHz Block	0.7 uA	0.23 uA
Standby Doze Current (SYSTEM ON IDLE +full RAM retention +RTC run current (0uA) + LFRC or LFXO)	2.5 uA	2.03 uA
Calibration	Calibration required regularly (default eight seconds interval). Calibration takes 32 ms; with DCDC used, the total charge of a calibration event is 15.1 uC (or 18.8uC with DCDC disabled). The average current consumed by the calibration depends on the calibration interval and can be calculated using the following formula: **CAL_charge/CAL_interval –** The lowest calibration interval (0.25 seconds) provides an average current of (DCDC enabled): **15.1uC/0.25s = 60.4uA**	Not applicable

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	BL653µ On-chip 32.768 kHz RC Oscillator (±500 ppm) LFRC	Optional External Higher Accuracy (±20 ppm) 32.768 kHz Crystal-based Oscillator LFXO
	To get the 250-ppm accuracy, the Bluetooth LE stack specification states that a calibration interval of 8 seconds is enough. This gives an average current of: **15.1uC/8s = 1.89 uA** Added to the LFRC run current and Standby Doze (IDLE) base current shown above results in a total average current of: **LFRC + CAL = 2.5 + 1.89 = 4.39 uA**	
Total	4.39 uA	2.03 uA
Summary	▪ Low current consumption ▪ Accuracy 250 ppm	▪ Lowest current consumption ▪ Needs external crystal ▪ High accuracy (depends on the crystal, usually 20 ppm)

Table 23: Optional external 32.768 kHz crystal specification

Optional external 32.768kHz crystal	Min	Typ	Max
Crystal Frequency	-	32.768 kHz	-
Frequency tolerance requirement of Bluetooth LE stack	-	-	±500 ppm
Load Capacitance	-	-	12.5 pF
Shunt Capacitance	-	-	2 pF
Equivalent series resistance	-	-	100 kOhm
Drive level	-	-	1 uW
Input capacitance on XL1 and XL2 pads	-	4 pF	-
Run current for 32.768 kHz crystal based oscillator	-	0.23 uA	-
Start-up time for 32.768 kHz crystal based oscillator	-	0.25 seconds	-
Peak to peak amplitude for external low swing clock input signal must not be outside supply rails	200 mV	-	1000 mV

Be sure to tune the load capacitors on the board design to optimize frequency accuracy (at room temperature) so it matches that of the same crystal standalone, Drive Level (so crystal operated within safe limits) and oscillation margin (R_{neg} is at least 3 to 5 times ESR) over the operating temperature range.

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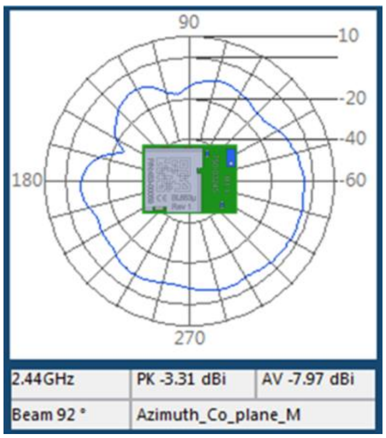
5.18 453-00059 On-board chip antenna characteristics

The 453-00059 on-board chip antenna radiated performance depends on the host PCB layout. BL653u 453-00059 on board chip antenna Yageo ANT1608LL14R2400A datasheet.

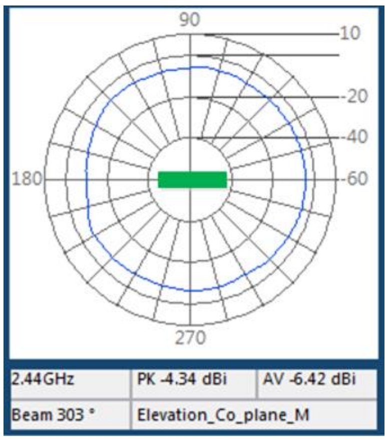
The Laird internal BL653µ development board was used for BL653µ development and the 453-00059 chip antenna performance evaluation. To obtain similar performance, follow guidelines in section *PCB Layout on Host PCB for the 453-00059* to allow the on-board PCB antenna to radiate and reduce proximity effects due to nearby host PCB GND copper or metal covers.

Antenna Efficiency	XY-plane		YZ-plane		ZX-plane	
	Peak	Avg	Peak	Avg	Peak	Avg
453-00059 chip antenna (Yageo ANT1608LL14R2400A)	-3.31 dBi	-7.97 dBi	-4.34 dBi	-6.42 dBi	-5 dBi	-10.3 dBi

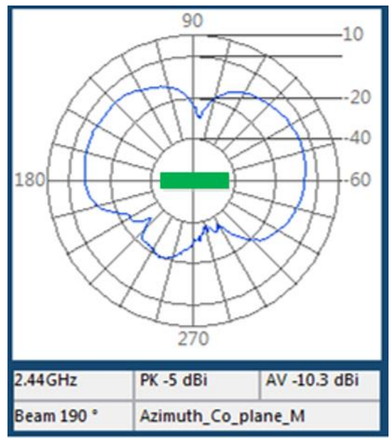
XY Plane



YZ Plaze



ZX Plane



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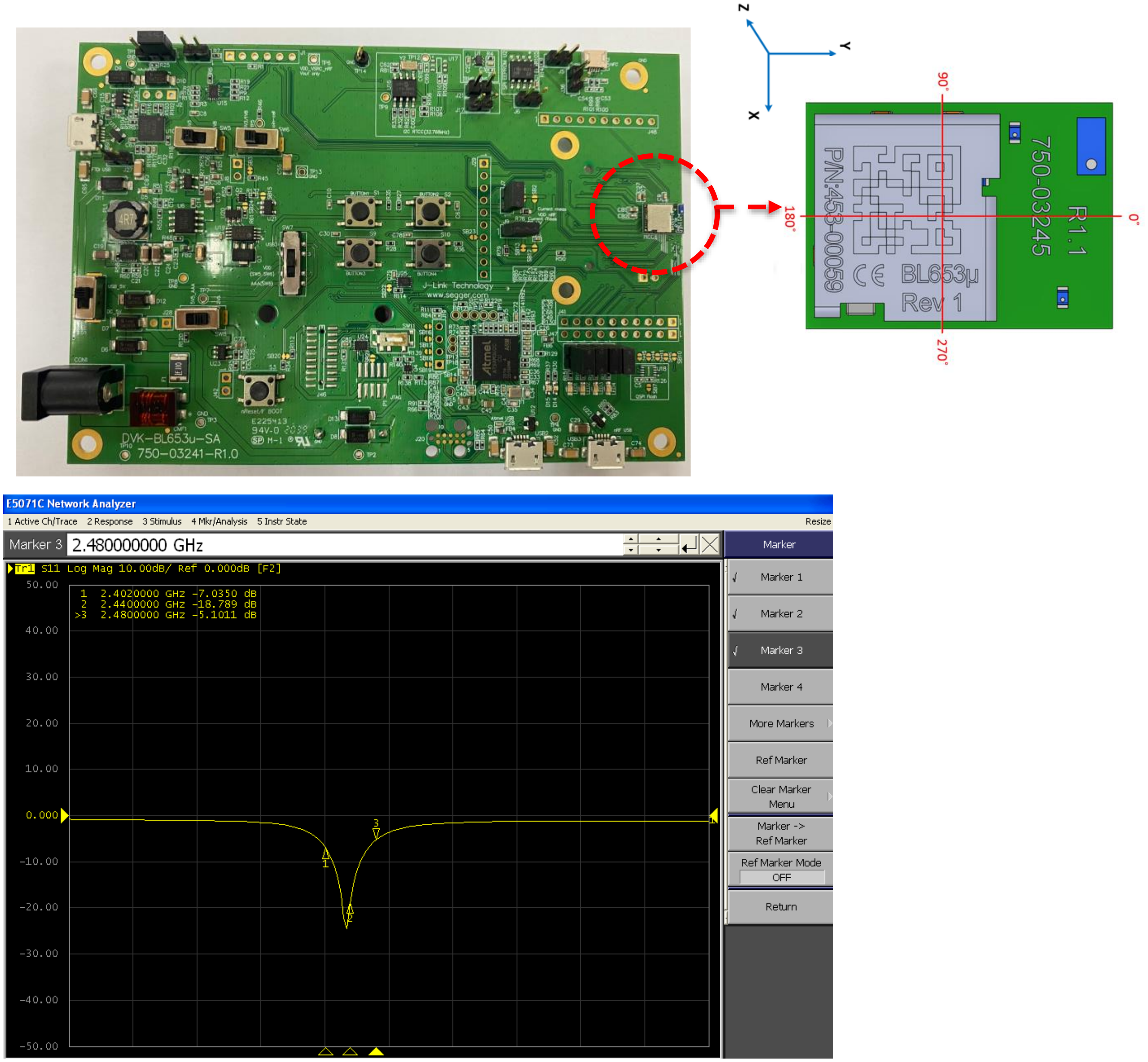

Figure 9: 453-00059 on-board chip antenna performance (Antenna Gain and S11 – whilst 453-00059 module sitting on Laird internal devboard

6 Hardware Integration Suggestions

6.1 Circuit

The BL653µ is easy to integrate, requiring no external components on your board apart from those which you require for development and in your end application.

The following are suggestions for your design for the best performance and functionality.

Checklist (for Schematic):

BL653µ power supply options:

- BL653µ power supply pin VDD_NRF_1 (pin 30) MUST be connected to VDD_NRF(pin 21) on customers design.
- BL653µ power supply pin VDD_NRF_1 (pin 30) MUST have decoupling capacitor 100nF minimum connected (16V rating, X7R) placed next to VDD_NRF_1 (pin 30).

The above two points apply whether option 1 or option 2 below is used.

Option 1 – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDDH pins (so that VDD equals VDD_HV). Connect external supply within range 1.7V to 3.6V range to BL653µ VDD and VDD_HV pins.

OR

Option 2 – High voltage mode power supply mode (using BL653µ VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD pin is not connected to any external voltage supply. Connect external supply within range 2.5V to 5.5V range to BL653µ VDD_HV pin. BL653µ VDD_NRF pin left unconnected.
In High Voltage mode (VDD_HV), No external current draw (from VDD pin) is allowed (limitation of nRF52833 chipset).

For either option, if you use USB interface then the BL653µ VBUS pin must be connected to external supply within the range 4.35V to 5.5V. When using the BL653µ VBUS pin, you MUST externally fit a 4.7uF to ground.

Note: To avoid surpassing the maximum die temperature (110 ºC), it is important to minimize current consumption when operating in the extended operating temperature conditions (+85 ºC to +105ºC). It is therefore recommended to use the module device on Normal Voltage mode with DCDC (REG1) enabled.

External power source should be within the operating range, rise time and noise/ripple specification of the BL653µ. Add decoupling capacitors for filtering the external source. Power-on reset circuitry within BL653µ series module incorporates brown-out detector, thus simplifying your power supply design. Upon application of power, the internal power-on reset ensures that the module starts correctly.

- **VDD and coin-cell** operation

  With a built-in DCDC (operating range 1.7V to 3.6V), that reduces the peak current required from a coin-cell, making it easier to use with a coin-cell.

- **AIN (ADC) and SIO pin IO voltage levels**

  BL653µ SIO voltage levels are at VDD. Ensure input voltage levels into SIO pins are at VDD also (if VDD source is a battery whose voltage will drop). Ensure ADC pin maximum input voltage for damage is not violated.

- **AIN (ADC) impedance and external voltage divider setup**

  If you need to measure with ADC a voltage higher than 3.6V, you can connect a high impedance voltage divider to lower the voltage to the ADC input pin.

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- **JTAG (SWD)**

  This is REQUIRED as Nordic SDK applications can only be loaded using the SWD (JTAG) (*smart*BASIC firmware can be loaded using the JTAG as well as the UART).

  We recommend that you use JTAG (2-wire interface) to handle future BL653µ module firmware upgrades. You MUST wire out the JTAG (2-wire interface) on your host design (see Figure 8, where four lines should be wired out, namely SWDIO, SWDCLK, GND and VCC). Firmware upgrades can still be performed over the BL653µ UART interface, but this is slower (60 seconds using UART vs. 10 seconds when using JTAG) than using the BL653µ JTAG (2-wire interface).
  JTAG may be used if you intend to use Flash Cloning during production to load *smart*BASIC scripts.

- **UART**

  Required for loading your *smart*BASIC application script during development (or for subsequent firmware upgrades (except JTAG for FW upgrades and/or Flash Cloning of the *smart*BASIC application script). Add connector to allow interfacing with UART via PC (UART–RS232 or UART-USB).

- **UART_RX and UART_CTS**

  SIO_08 (alternative function UART_RX) is an input, set with internal weak pull-up (in firmware). The pull-up prevents the module from going into deep sleep when UART_RX line is idling.
  SIO_07 (alternative function UART_CTS) is an input, set with internal weak pull-down (in firmware). This pull-down ensures the default state of the UART_CTS will be asserted which means can send data out of the UART_TX line. Laird Connectivity recommends that UART_CTS be connected.

- **nAutoRUN pin and operating mode selection**

  nAutoRUN pin needs to be externally held high or low to select between the two BL653µ operating modes at power-up:

  - Self-contained Run mode (nAutoRUN pin held at 0V).
  - Interactive / development mode (nAutoRUN pin held at VDD).
    Make provision to allow operation in the required mode. Add jumper to allow nAutoRUN pin to be held high or low (BL653µ has internal 13K pull-down by default) OR driven by host GPIO.

- **I2C**

  It is essential to remember that pull-up resistors on both I2C_SCL and I2C_SDA lines are not provided in the BL653µ module and MUST be provided external to the module as per I2C standard.

- **SPI**

  Implement SPI chip select using any unused SIO pin within your *smart*BASIC application script or Nordic application then SPI_CS is controlled from the software application allowing multi-dropping.

- **SIO pin direction**

  BL653µ modules shipped from production with *smart*BASIC FW, all SIO pins (with default function of DIO) are mostly digital inputs (see Pin Definitions Table 2). Remember to change the direction SIO pin (in your *smart*BASIC application script) if that particular pin is wired to a device that expects to be driven by the BL653µ SIO pin configured as an output. Also, these SIO pins have the internal pull-up or pull-down resistor-enabled by default in firmware (see Pin Definitions Table 2). This was done to avoid floating inputs, which can cause current consumption in low power modes (e.g. StandbyDoze) to drift with time. You can disable the PULL-UP or Pull-down through their *smart*BASIC application.

  Note: Internal pull-up, pull down takes current from VDD.

- **SIO_02 pin** and OTA *smart*BASIC application download feature
  SIO_02 is an input, set with internal pull-down (in FW). Refer to latest firmware release documentation on how SIO_02 is used for Over the Air *smart*BASIC application download feature. The SIO_02 pin must be pulled high externally to enable the feature. Decide if this feature is required in production. When SIO_02 is high, ensure nAutoRun is NOT high at same time; otherwise you cannot load the *smart*BASIC application script.

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- **NFC antenna connector**
  To make use of the Laird Connectivity flexi-PCB NFC antenna, fit connector:
  - Description – FFC/FPC Connector, Right Angle, SMD/90d, Dual Contact,1.2 mm Mated Height
  - Manufacturer – Molex
  - Manufacturers Part number – 512810594

  Add tuning capacitors of 300 pF on NFC1 pin to GND and 300 pF on NFC2 pins to GND if the PCB track length is similar as development board.
- **nRESET pin (active low)**
  Hardware reset. Wire out to push button or drive by host.
  By default module is out of reset when power applied to VCC pins.
- **Optional External 32.768kHz crystal**

  If the optional external 32.768kHz crystal is needed, then use a crystal that meets specification and add load capacitors whose values should be tuned to meet all specification for frequency and oscillation margin.
- **BL653µ module RF pad variant 453-00060**

  If using the BL653µ module RF pad variant (453-00060), MUST copy the 50-Ohms GCPW RF track design, MUST add series 2nH RF inductor (Murata LQG15HN2N0B02# or Murata LQG15HS2N0B02) and RF connector IPEX MHF4 Receptacle (MPN: 20449-001E) Detailed in the following section: 6.4 50-Ohms RF Trace and RF Match Series 2nH RF Inductor on Host PCB for BL653µ RF Pad Variant (453-00060)

6.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate BL653µ module close to the edge of PCB (mandatory for the 453-00059 for on-board chip antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect the copper flood to the inner GND plane. If GND flood copper is on the bottom of the module, then connect it with GND vias to the inner GND plane.
- Route traces to avoid noise being picked up on VDD_NRF (and VDD_NRF_1), VDDH, VBUS supply and AIN (analogue) and SIO (digital) traces.
- Ensure no exposed copper is on the underside of the module (refer to land pattern of BL653µ).
- **BL653µ G1 Ground Pin (453-00059. 453-00060)** – Must be grounded to ground plane of host PCB as shown below (shown example is for 453-00059).

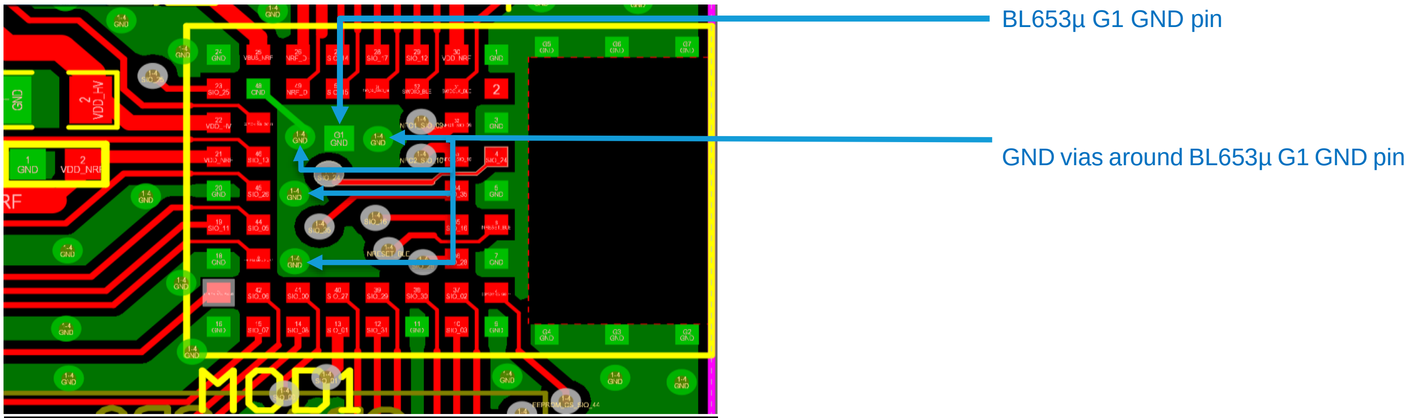

Figure 10: Layer1 (GND is shown in green colour) and shows BL653µ G1 GND pin grounding

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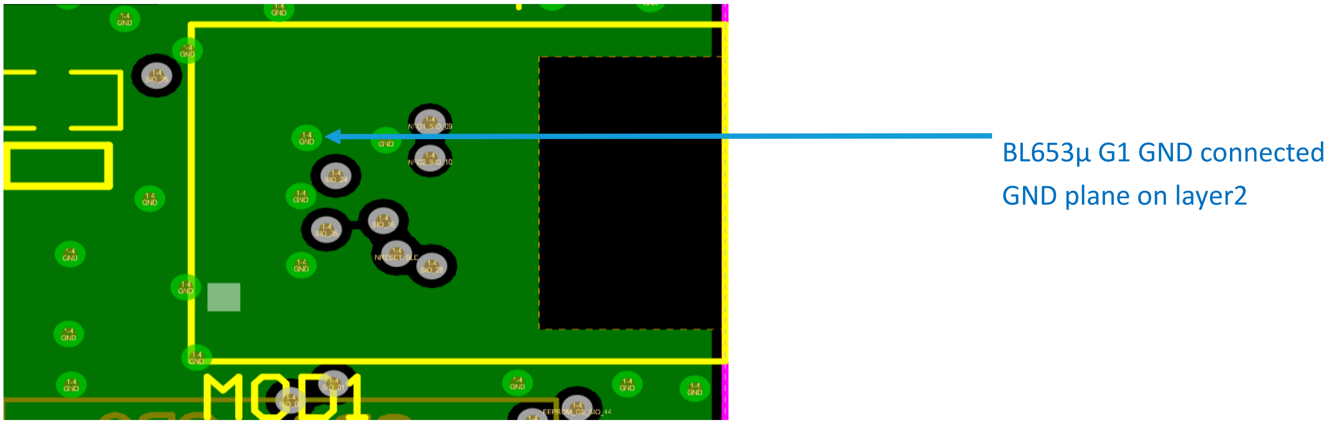


Figure 11: Layer2 (GND plane – green color) BL653µ G1 GND pin grounded to GND plane

6.3 PCB Layout on Host PCB for the 453-00059

6.3.1 Antenna Keep-Out on Host PCB

The 453-00059 has an integrated chip antenna and its performance is sensitive to host PCB. It is critical to locate the 453-00059 on the edge of the host PCB to allow the antenna to radiate properly. Refer to guidelines in section ***PCB land pattern and antenna keep-out area for the 453-00059***. Some of those guidelines repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the 453-00059 module on the edge of the host PCB, preferably in the edge center.
- The BL653µ development board has the 453-00059 module on the edge of the board (not in the corner). The antenna keep-out area is defined by the Laird Connectivity internal BL653µ development board which was used for module development and antenna performance evaluation is shown in Figure 12, where the antenna keep-out area is ~5 mm wide, 3 mm long; with PCB dielectric (no copper) height ~1 mm sitting under the 453-00059 chip antenna.
- The 453-00059 module on-board chip antenna is tuned when the 453-00059 is sitting on Laird Connectivity internal development board (host PCB) with size of 125 mm x 85 mm x 1mm.
- A different host PCB thickness dielectric will have small effect on antenna.
- The antenna-keep-out defined in the Host PCB Land Pattern and Antenna Keep-out for the 453-00059 section.
- Host PCB land pattern and antenna keep-out for the BL653µ applies when the 453-00059 is placed in the edge of the host PCB preferably in the edge center. Figure 12 shows an example.

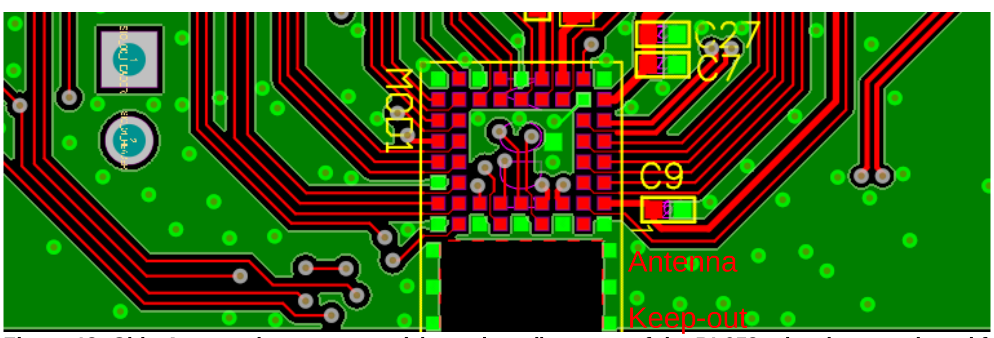


Figure 12: Chip Antenna keep-out area (shown in red), corner of the BL653µ development board for the 453-00059 module.

Antenna Keep-out Notes:

Note 1	The BL653µ module is placed on the edge, preferably edge centre of the host PCB.
Note 2	Copper cut-away on all layers in the *Antenna Keep-out* area under the 453-00059 on host PCB.

6.3.2 Antenna Keep-Out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the 453-00059 chip antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of that degradation is entirely system dependent, meaning you will need to perform some testing with your host application.
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic) and host PCB board size (GND plane size).

6.4 50-Ohms RF Trace and RF Match Series 2nH RF Inductor on Host PCB for BL653µ RF Pad Variant (453-00060)

To use an external antenna requires BL653µ module variant with RF pad (453-00060) and 50-Ohm RF trace (GCPW, that is Grounded Coplanar Waveguide) from RF_pad (pin2) of the module (BL653µ 453-00060) to RF antenna connector (IPEX MHF4) on host PCB. On this RF path, MUST use 2nH series RF inductor. BL653µ module GND pin1 and GND pin3 used to support GCPW 50-Ohm RF trace.

Checklist for SCH

- MUST fit 2 nH RF inductor (R144) in series. RF inductor part number is Murata LQG15HN2N0B02# or Murata LQG15HS2N0B02# with 0402 body size.
  https://www.murata.com/en-eu/products/productdetail.aspx?partno=LQG15HN2N0B02%23
  https://www.murata.com/en-eu/products/productdetail.aspx?partno=LQG15HS2N0B02%23
- MUST fit RF connector IPEX MHF4 Receptacle (MPN: 20449-001E), https://www.i-pex.com/product/mhf-4-smt#!

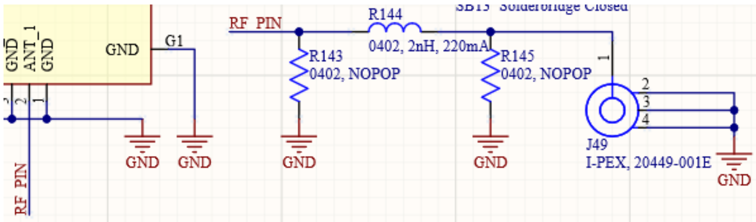
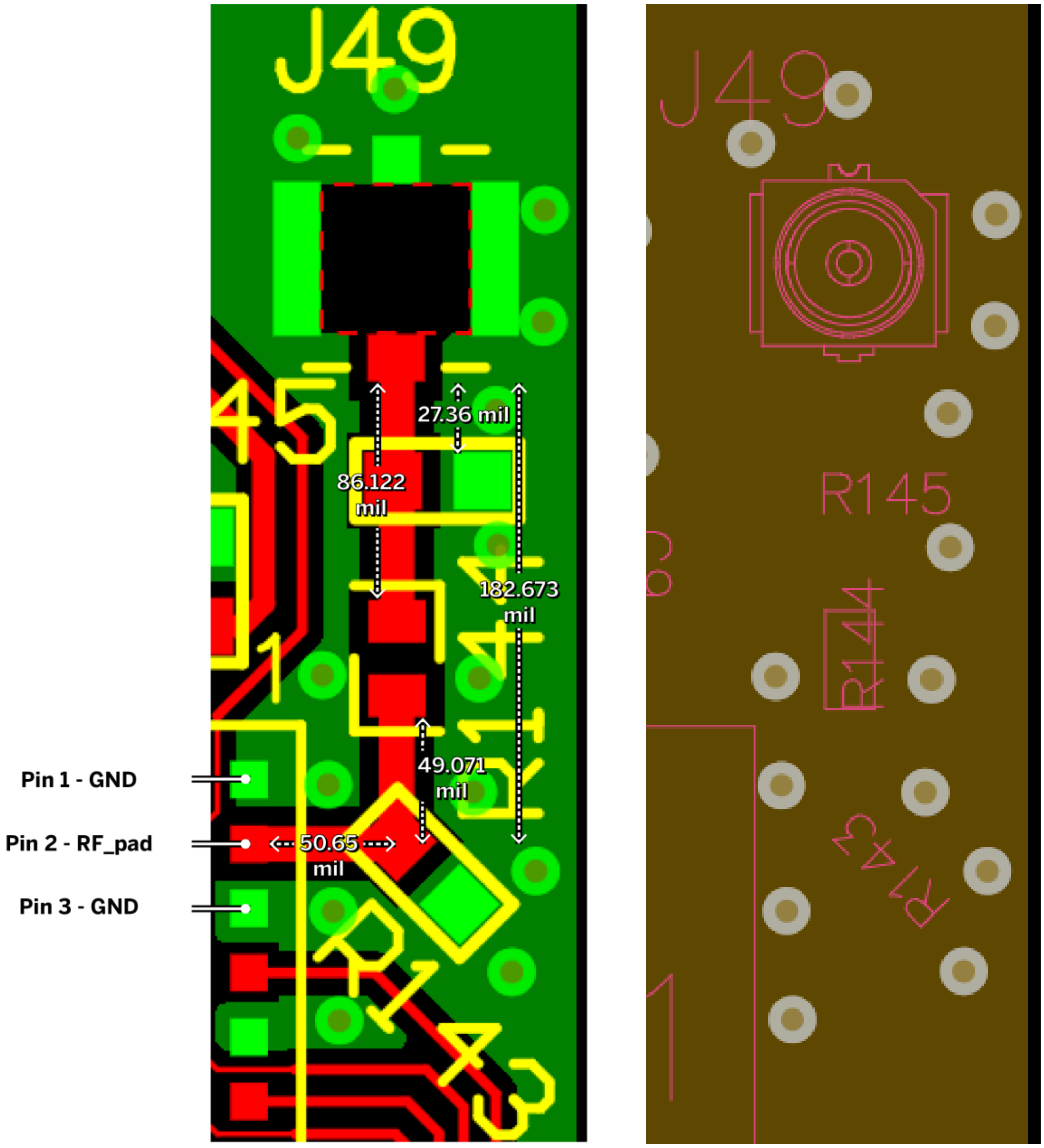


Figure 13: BL653u RF pad variant (453-00060) Host PCB 50-Ohm RF trace schematic with series 2nH inductor, RF connector



Layer1 (RF Track and RF GND)

Layer2 (RF GND) and Layer2 copper cut-out under RF connector

Figure 14: 50-Ohm RF trace design (Layer1 and Layer2) on BL653µ development board (or host PCB) for use with BL653µ (453-00060) module

Checklist for PCB:

- MUST use a 50-Ohm RF trace (GCPW, that is Grounded Coplanar Waveguide) from RF_pad (pin2) of the module (BL653µ 453-00060) to RF antenna connector (IPEX MHF4) on host PCB.

  To ensure regulatory compliance, MUST follow exactly the following considerations for 50-Ohms RF trace design and test verification:

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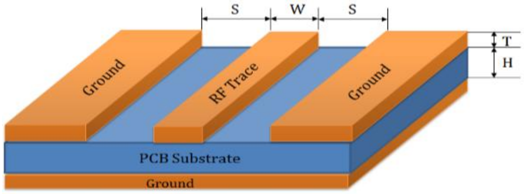

	Thickness mil	Dielectric Constant Er
Solder Mask	0.4	3.5
Layer1 Copper 0.5oz+plating (Note1)	1.3	
Prepreg ()	10.1	4.3
Layer2 Copper 1oz	1.3	
Core 0.3mm	12	4.1
Layer3 Copper 1oz	1.3	
Prepreg ()	10.1	4.3
Layer1 Copper 0.5oz+plating	1.3	
Solder Mask	0.4	3.5

Stack up for 50Ohms GCPW RF track.

Note 1: The plating (ENIG) above base 0.5z copper is not listed, but plating expected to be ENIG.

Figure 15: BL653µ development board PCB stack-up and L1 to L2 50-Ohms Grounded CPW RF trace design

- The 50-Ohms RF trace design MUST be Grounded Coplanar Waveguide (GCPW) with
  - Layer1 RF track width (W) of 14.0mil and
  - Layer1 gap (G) to GND of 7.3mil and where the
  - Layer1 to Layer 2 dielectric thickness (H) MUST be 10.1mil (dielectric constant Er 4.3).
  - Further the Layer1 base copper must be 0.5-ounce base copper (that is 0.7mil) plus the plating and
  - Layer1 MUST be covered by solder mask of 0.4mil thickness (dielectric constant Er 3.5).
- The 50-Ohms RF trace design MUST follow the PCB stack-up shown in Figure 15. (Layer1 to Layer2 thickness MUST be identical to that in Figure 15 board).
- The 50-Ohms RF track should be a controlled-impedance trace e.g. ±10%.
- The 50-Ohms RF trace length MUST be identical (as seen in Figure 15) (233.323mil) from BL653µ module RF pad (pin2) to the RF connector IPEX MHF4 Receptable (MPN: 20449-001E).
- Place GND vias regularly spaced either side of 50-Ohms RF trace to form GCPW (Grounded coplanar waveguide) transmission line as shown in Figure 14 and use BL653µ module GND pin1 and GND pin3.
- Use spectrum analyzer to confirm the radiated (and conducted) signal is within the certification limit.

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6.5 External Antenna Integration with 453-00060

Please refer to the regulatory sections for FCC, IC, CE, RCM, KC, and Japan for details of use of BL653µ-with external antennas in each regulatory region.

The BL653µ RF Trace pin module variant has been designed to operate with the below external antennas (with a maximum gain of 2.0 dBi). The required antenna impedance is 50 ohms. See Table 24. External antennas improve radiation efficiency.

Table 24: External antennas for the BL653µ

Manufacturer	Model	Laird Connectivity Part Number	Type	Connector	Peak Gain	
					2400-2500 MHz	2400-2480 MHz
Laird Connectivity	NanoBlue	EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2 dBi	-
Laird Connectivity	FlexPIFA	001-0022	PIFA	IPEX MHF4	-	2 dBi
Mag.Layers	EDA-8709-2G4C1-B27-CY	0600-00057	Dipole	IPEX MHF4	2 dBi	-
Laird Connectivity	mFlexPIFA	EFA2400A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Laird Connectivity	Laird Connectivity NFC	0600-00061	NFC	N/A	-	-

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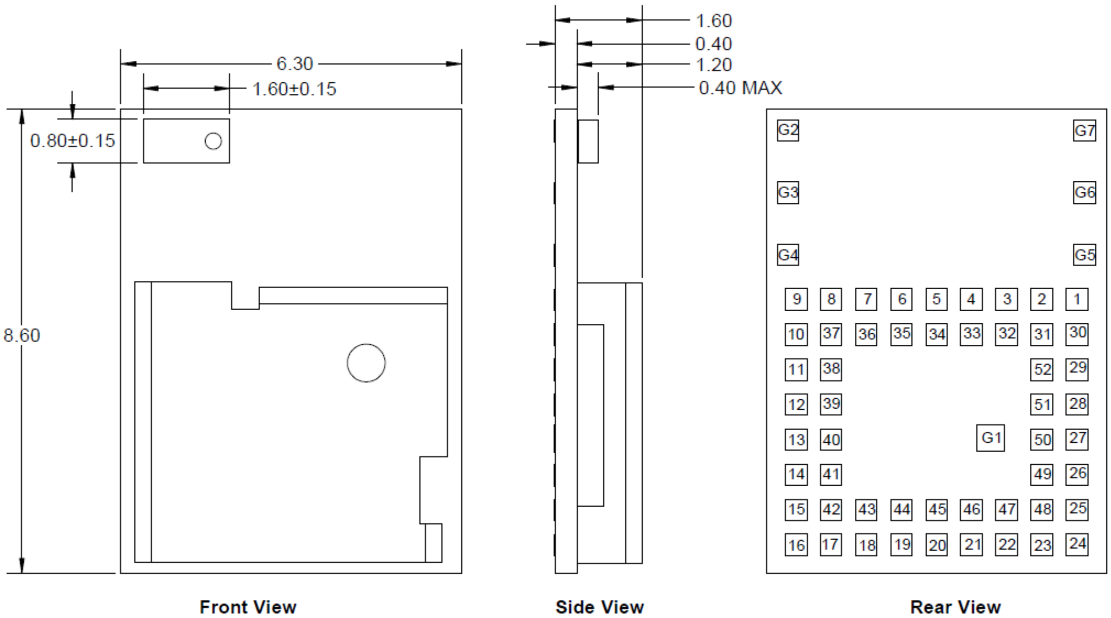
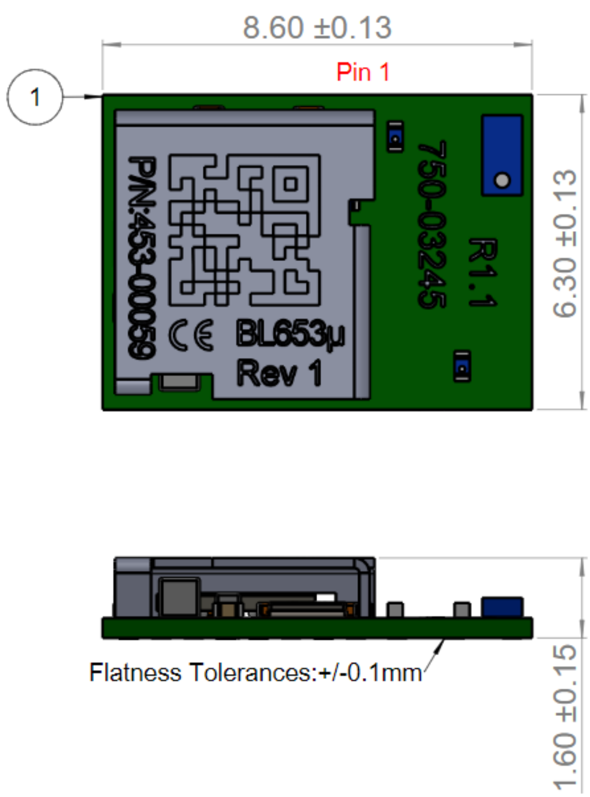
Mechanical Details

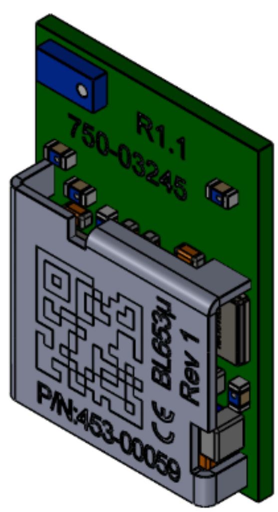
7.1 BL653µ Mechanical Details

3D Models can be found on the BL653µ product page.

7 **453-00059 BL653µ Micro Bluetooth LE module (Nordic nRF52833) – Integrated antenna**







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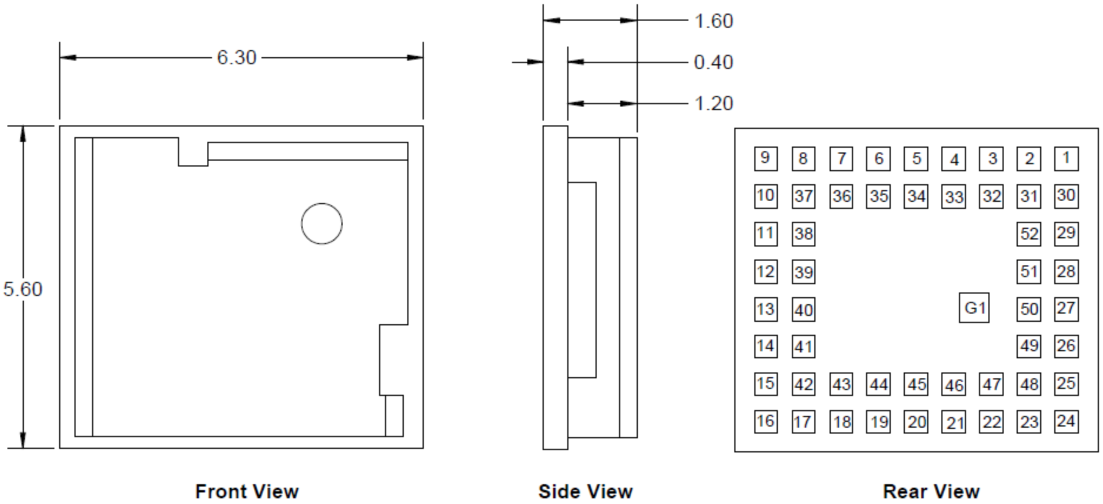
453-00060 BL653µ Micro Bluetooth LE module (Nordic nRF52833) – Trace pin



Tolerances

Board Outline:+/-0.13mm
Board Height:+/-0.15mm

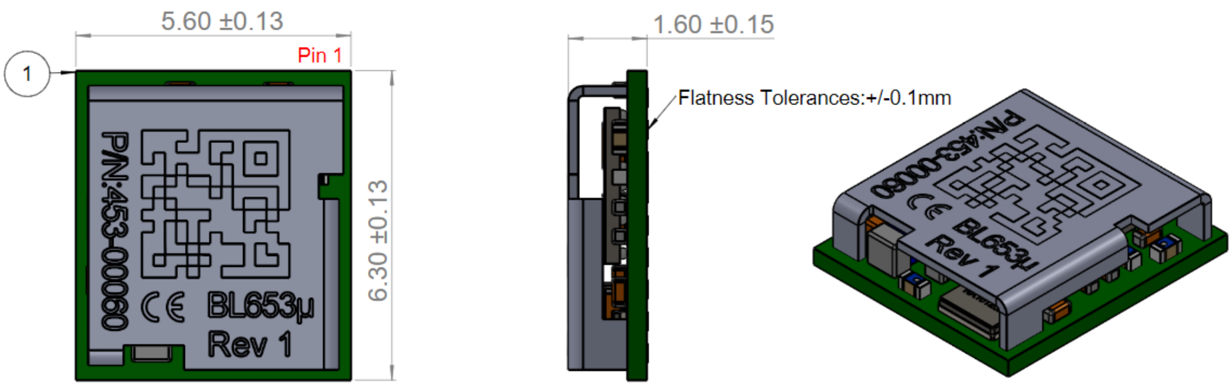


Figure 16: BL653µ mechanical drawings

7.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00059

PCB Footprints (DXF and Altium format) can be found on the BL653µ product page.

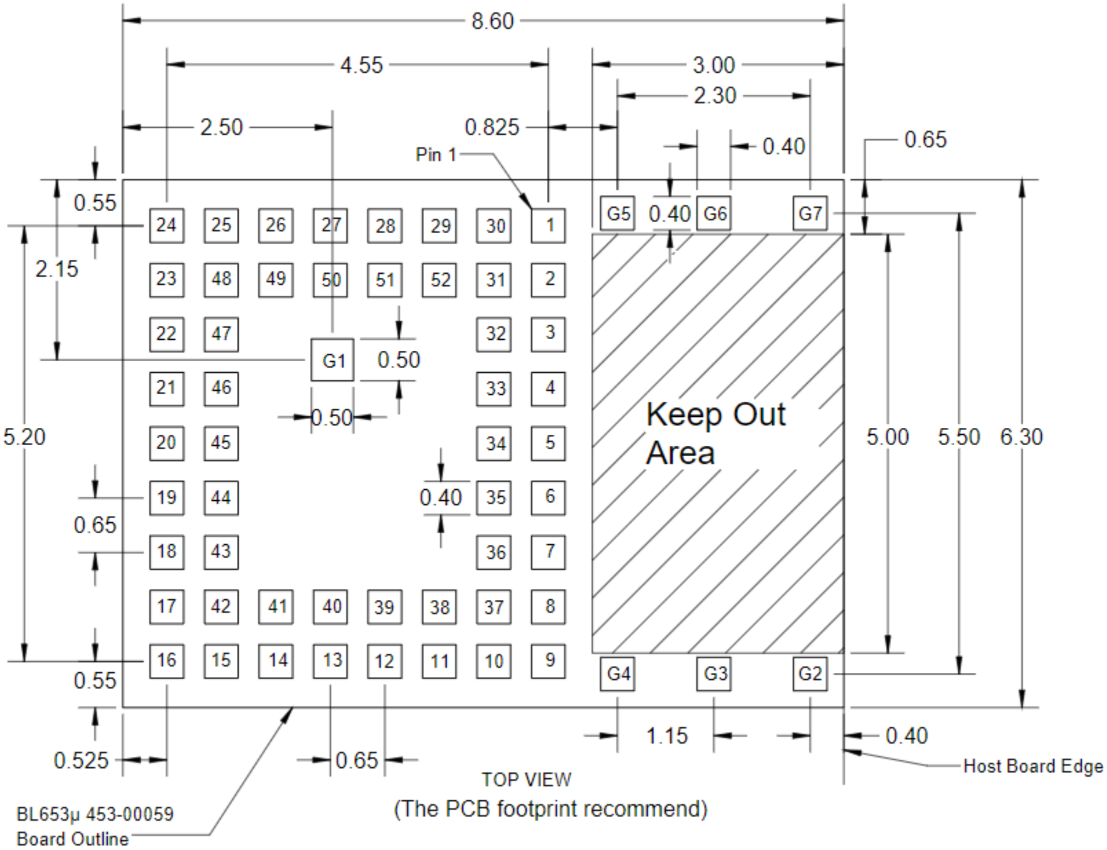


Figure 17: Land pattern and Keep-out for the 453-00059

All dimensions are in millimeters.

Host PCB Land Pattern and Antenna Keep-out for the 453-00059 Notes:

Note 1	Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear of the area (Refer to 6.3.2) to reduce effects of proximity detuning the antenna and to help antenna radiate properly.
Note 2	For the best on-board antenna performance, the module 453-00059 MUST be placed on the edge of the host PCB and preferably in the edge centre and host PCB, the antenna "Keep Out Area" is extended (see Note 4).
Note 3	Laird internal BL653µ development board has the 453-00059 placed on the edge of the PCB board (and not in corner) see section *PCB Layout on Host PCB for the 453-00059*, Figure 17. This was used for module development and antenna performance evaluation.
Note 4	Ensure that there is no exposed copper under the module on the host PCB.
Note 5	You may modify the PCB land pattern dimensions based on their experience and/or process capability.
Note 6	BL653µ G1 Ground Pin (453-00059. 453-00060) – Must be grounded to ground plane of host PCB as shown in section 6.2. PCB Layout on Host PCB - General

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Application Note for Surface Mount Modules

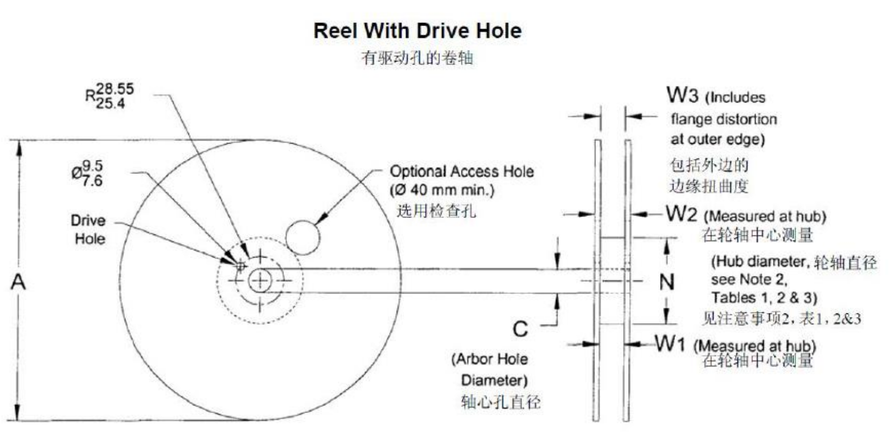
8.1 Introduction

Laird Connectivity's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is
8 considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

8.2 Shipping

8.2.1 Tape and Reel Package Information

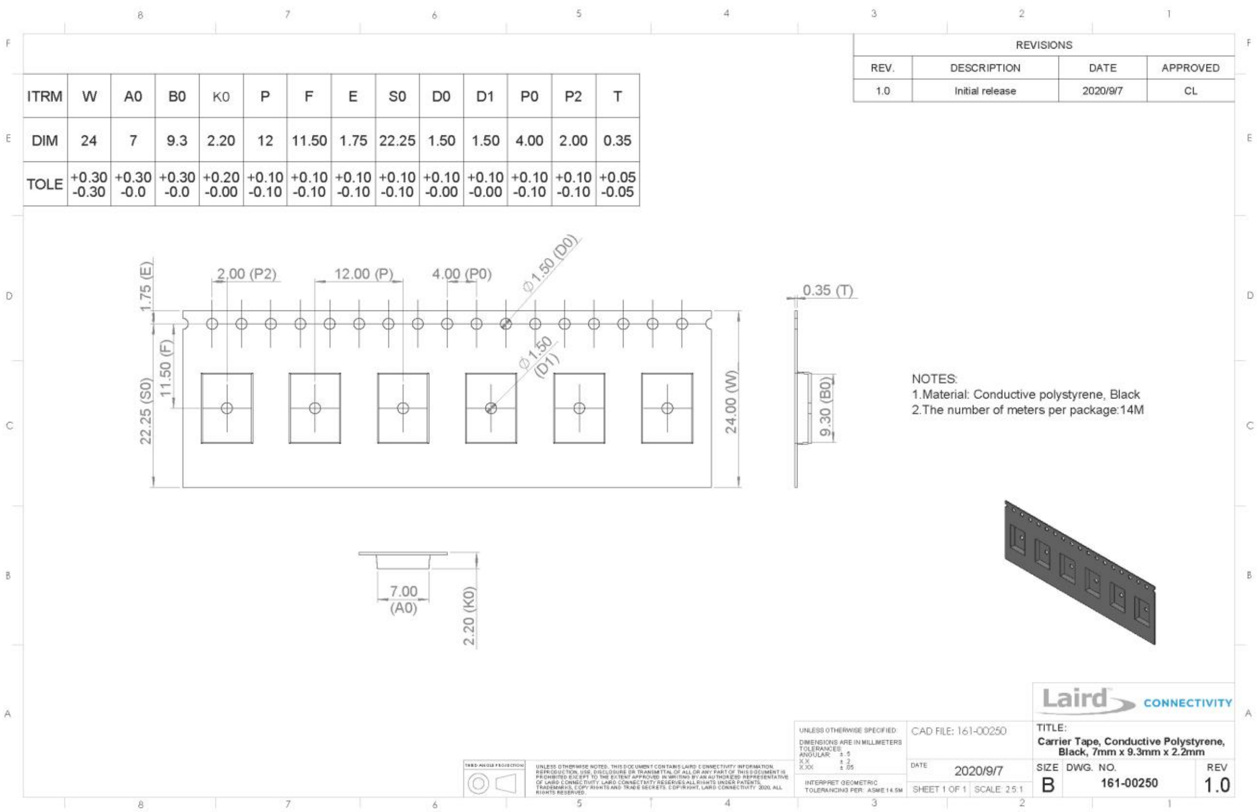


Variable Dimensions 变动尺寸部分

Tape Size (mm) 带宽 (毫米)	N Min. See Note 2, Tables 1-3 见注意事项 2,表 1-3	W_1	W_2 Max for A<360 mm See Note 1 A<360 毫米时的 W_2 最大值见注意事项 1	W_2 Max for A ≥360 and ≤ 609 mm See Note 2 360≤A≤690 毫米时的 W_2 最大值见注意事项 2	W_3
24	60	24.4+2.0/-0.0	30.4	37.0	

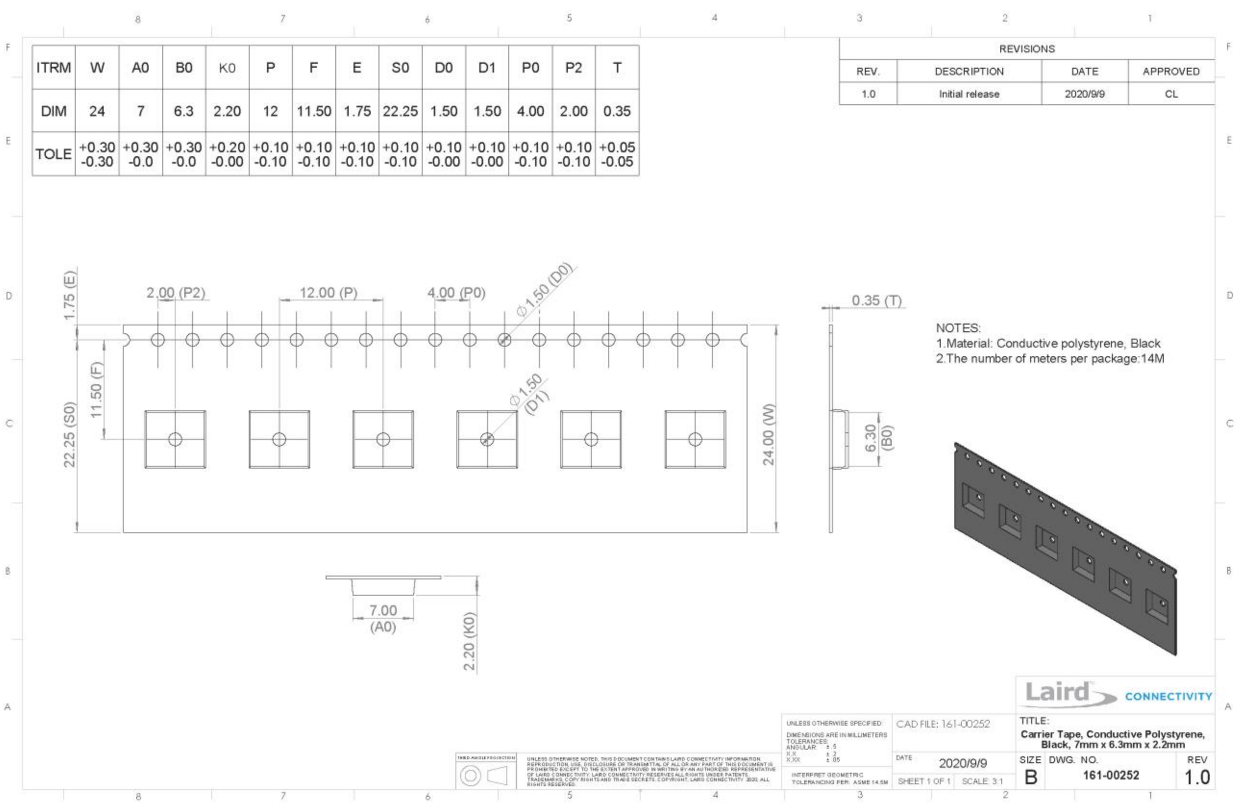
A值为13“（约330MM）

Figure 18: Reel specifications



ITRM	W	A0	B0	K0	P	F	E	S0	D0	D1	P0	P2	T
DIM	24	7	9.3	2.20	12	11.50	1.75	22.25	1.50	1.50	4.00	2.00	0.35
TOLE	+0.30 -0.30	+0.30 -0.0	+0.30 -0.0	+0.20 -0.00	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.00	+0.10 -0.00	+0.10 -0.10	+0.10 -0.10	+0.05 -0.05

Figure 19: Tape specifications, 161-00250



ITRM	W	A0	B0	K0	P	F	E	S0	D0	D1	P0	P2	T
DIM	24	7	6.3	2.20	12	11.50	1.75	22.25	1.50	1.50	4.00	2.00	0.35
TOLE	+0.30 -0.30	+0.30 -0.0	+0.30 -0.0	+0.20 -0.00	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.00	+0.10 -0.00	+0.10 -0.10	+0.10 -0.10	+0.05 -0.05

Figure 20: Tape specifications, 161-00252

There are 1,000 BL653µ modules taped in a reel (and packaged in a pizza box) and five boxes per carton (5000 modules per carton). Reel, boxes, and carton are labeled with the appropriate labels. See Carton Contents for more information.

8.2.2 Carton Contents

The following are the contents of the carton shipped for the BL653µ modules.

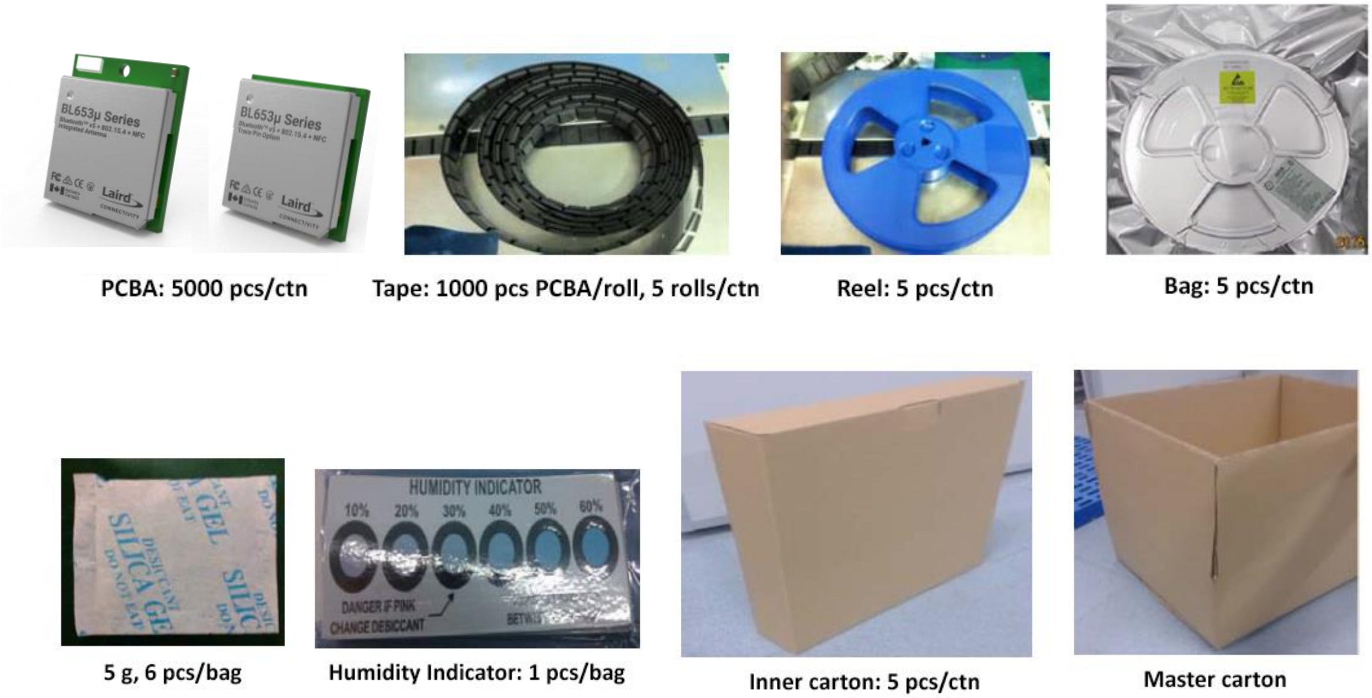


Figure 21: Carton contents for the BL653µ

8.2.3 Packaging Process

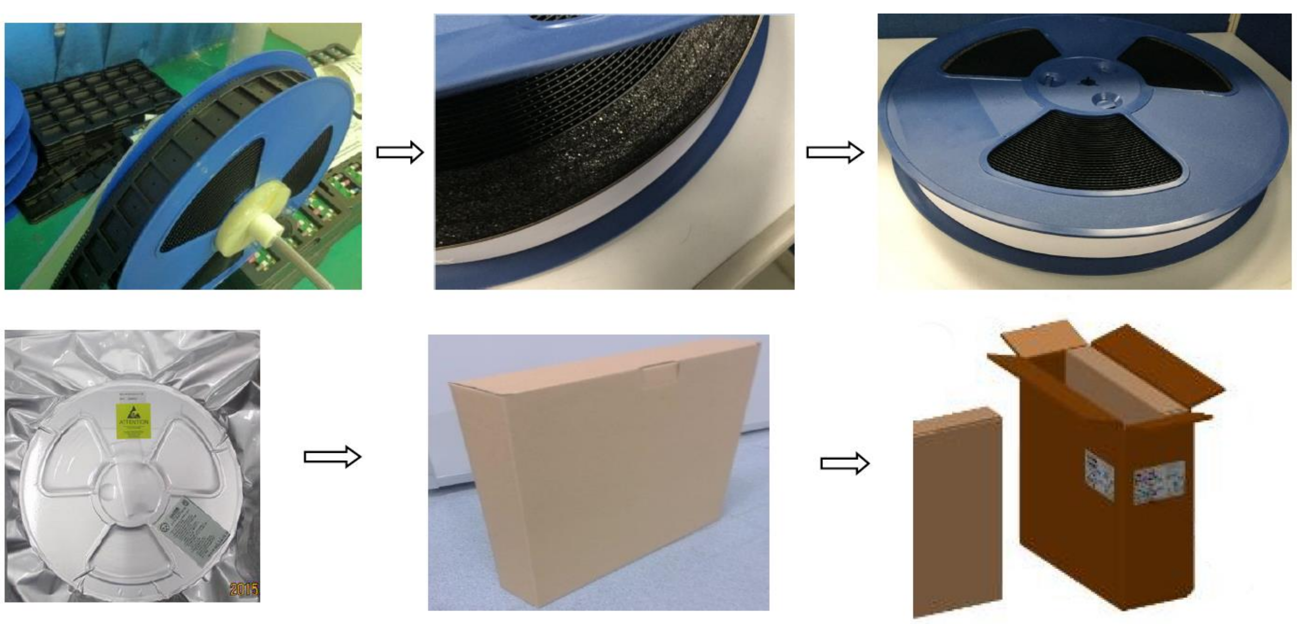


Figure 22: BL653µ packaging process

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8.2.4 Labeling

The following labels are located on the antistatic bag:

Figure 23: Antistatic bag labels

The following package label is located on both sides of the master carton:

Figure 24: Master carton package label

The following is the packing slip label:

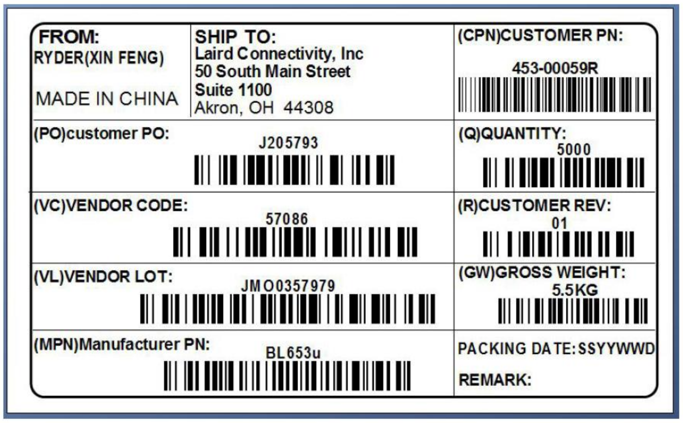

Figure 25: Packing slip label

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8.3 Reflow Parameters

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to *bake units* on the card, see Table 25 and follow instructions specified by IPC/JEDEC J-STD-033. A copy of this standard is available from the JEDEC website: http://www.jedec.org/sites/default/files/docs/jstd033b01.pdf

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 4 devices is 72 hours in ambient environment ≤30°C/60%RH.

Table 25: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	**Floor Life Limit + 72 hours @ 30°C/60%**	**Saturated @ 30°C/85%**	**Floor Life Limit + 72 hours @ 30°C/60%**	**Saturated @ 30°C/85%**	**Floor Life Limit + 72 hours @ 30°C/60%**
4	11 hours	7 hours	37 hours	23 hours	15 days	9 days

Laird Connectivity surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Laird Connectivity surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

Important: During reflow, modules should not be above 260° and not for more than 30 seconds. In addition, we recommend that the BL653µ module **does not** go through the reflow process more than one time; otherwise the BL653µ internal component soldering may be impacted.

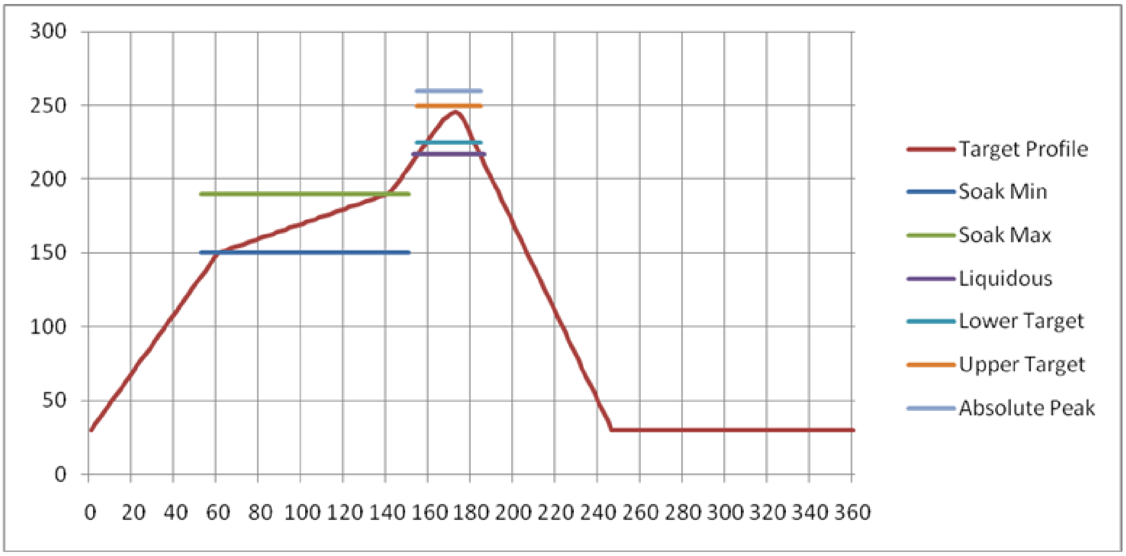

Figure 26: Recommended reflow temperature

Temperatures should not exceed the minimums or maximums presented in Table 26.

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Table 26: Recommended maximum and minimum temperatures

Specification	Value	Unit
Temperature Inc./Dec. Rate (max)	1~3	°C / Sec
Temperature Decrease rate (goal)	2-4	°C / Sec
Soak Temp Increase rate (goal)	.5 - 1	°C / Sec
Flux Soak Period (Min)	70	Sec
Flux Soak Period (Max)	120	Sec
Flux Soak Temp (Min)	150	°C
Flux Soak Temp (max)	190	°C
Time Above Liquidous (max)	70	Sec
Time Above Liquidous (min)	50	Sec
Time In Target Reflow Range (goal)	30	Sec
Time At Absolute Peak (max)	5	Sec
Liquidous Temperature (SAC305)	218	°C
Lower Target Reflow Temperature	240	°C
Upper Target Reflow Temperature	250	°C
Absolute Peak Temperature	260	°C

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9 Regulatory

Note: For complete regulatory information, refer to the BL653µ Regulatory Information document which is also available from the BL653µ product page.

The 453-00059/453-00060 (BL653µ) holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQGBL653U
EU	N/A
Canada (ISED)	3147A-BL653U
Japan (MIC)	201-200419

10 Ordering Information

Part Number	Product Description
453-00059R	BL653µ Micro Bluetooth LE module (Nordic nRF52833) – Integrated antenna (Tape/Reel)
453-00060R	BL653µ Micro Bluetooth LE module (Nordic nRF52833) – Trace pin (Tape/Reel)
453-00059C	BL653µ Micro Bluetooth LE module (Nordic nRF52833) – Integrated antenna (Cut Tape)
453-00060C	BL653µ Micro Bluetooth LE module (Nordic nRF52833) – Trace pin (Cut Tape)

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11 Bluetooth SIG Qualification

11.1 Overview

The BL653µ module is listed on the Bluetooth SIG website as a qualified End Product.

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
BL653µ	Laird Connectivity	D049591	147394	https://launchstudio.bluetooth.com/ListingDetails/104900

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to registered as a member of the Bluetooth SIG – www.bluetooth.org

The following link provides a link to the Bluetooth Registration page: https://www.bluetooth.org/login/register/

For each Bluetooth Design, it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document:

https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

11.2 Qualification Steps When Referencing a Laird Connectivity End Product Design

To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

In step 1, select the option, **Reference a Qualified Design** and enter D049591 in the End Product table entry. You can then select your pre-paid Declaration ID from the drop-down menu or go to the Purchase Declaration ID page, (please note that unless the Declaration ID is pre-paid or purchased with a credit card, it will not be possible to proceed until the SIG invoice is paid.

Once all the relevant sections of step 1 are finished, complete steps 2, 3, and 4 as described in the help document. Your new Design will be listed on the SIG website and you can print your Certificate and Declaration of Conformity.

For further information, please refer to the following training material:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

Note: If using the BL653µ with Laird Connectivity Firmware and *smart*BASIC script, you can skip "Controller Subsystem", "Host Subsystem", and "Profile Subsystem".

11.3 Qualification Steps When Deviating from a Laird Connectivity End Product Design

If you wish to deviate from the standard End Product design listed under D0xxxxx, the qualification process follows the Traditional Project route, creating a new design. When creating a new design, it is necessary to complete the full qualification listing process and also maintain a compliance folder for the new design.

The BL653µ design under D049591 incorporates the following components:

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Listing reference	Design Name	Core Spec Version
D043345	S140 Link Layer v7.0.1	5.1
D043346	S140 Host Layer v7.0.1	5.1

In the future, Nordic may list updated versions of these components and it is possible to use them in your new design. Please check with Nordic to make sure these software components are compatible with the nRF52833 hardware.

If your design is based on un-modified BL653µ hardware it is possible use the following process;

1. Reference the existing RF-PHY test report from the BL653µ listing.
2. Combine the relevant Nordic Link Layer (LL) – check QDID with Nordic.
3. Combine in a Host Component (covering L2CAP, GAP, ATT, GATT, SM) - check QDID with Nordic.
4. Test any standard SIG profiles that are supported in the design (customs profiles are exempt).

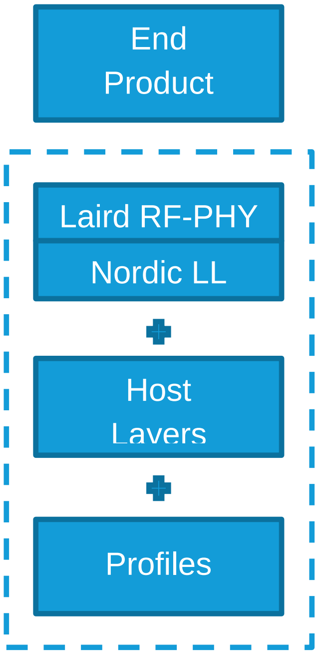

Figure 27: Scope of the qualification for an End Product Design

The first step is to generate a project on the TPG (Test Plan Generator) system. This determines which test cases apply to demonstrate compliance with the Bluetooth Test Specifications. If you are combining pre-tested and qualified components in your design and they are within their three-year listing period, you are not required to re-test those layers covered by these components.

If the design incorporates any standard SIG LE profiles (such as Heart Rate Profile), it is necessary to test these profiles using PTS or other tools where permitted; the results are added to the compliance folder.

You are required to upload your test declaration and test reports (where applicable) and then complete the final listing steps on the SIG website. Remember to purchase your Declaration ID before you start the qualification process, as it's impossible to complete the listing without it.

12 Reliability Tests

The BL653µ module went through the below reliability tests and passed.

Test Sequence	Test Item	Test Limits and Pass	Test Conditions
1	Vibration Test	JESD22-B103B Vibration, Variable frequency	Sample: Unpowered Sample number: 3 Vibration waveform: Sine waveform Vibration frequency /Displacement: 20 to 80 Hz /1.52 mm Vibration frequency /Acceleration: 80 to 2000 Hz /20 g Cycle time: 4 minutes Number of cycles: 4 cycles for each axis Vibration axis: X, Y, and Z (Rotating each axis on vertical vibration table)
2	Mechanical Shock	JESD22-B104C	Sample: Unpowered Sample number: 3 Pulse shape: Half-sine waveform Impact acceleration: 1500 g Pulse duration: 0.5 ms Number of shocks: 30 shocks (5 shocks for each face) Orientation: Bottom, top, left, right, front and rear faces
3	Thermal Shock	JESD22-A104E Temperature cycling	Sample: Unpowered Sample number: 3 Temperature transition time: Less than 30 seconds Temperature cycle: -40℃ (10 minutes), +105 ℃ (10 minutes) Number of cycles: 350

Before and after the testing, visual inspection showed no physical defect on samples.

After Vibration test and Mechanical Shock testing, the samples were functionally tested, and all samples functioned as normal. Then after Thermal shock test, the samples were functionally tested, and all samples functioned as normal.

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Additional Assistance

Please contact your local sales representative or our support team for further assistance:

Laird Connectivity
Support Centre: https://www.lairdconnect.com/resources/support
Email: support@lairdconnect.com
13 Phone: Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610
Web: https://www.lairdconnect.com/products

Note: Information contained in this document is subject to change.