Integration Guide

Sona™ IF573 Modules

Application Note *v1.2*

1 Introduction

This document describes key hardware aspects of Laird Connectivity's Sona™IF573 M.2 modules, which are based on Infineon's AIROC™ CYW55573 chipset. It serves as a preliminary to the full module datasheet, and is provided to assist in initial hardware integration.

The following are covered in this integration guide:

- SONA™ IF573 SMT Module
  - SONA™ IF573 SMT Module PCB Footprint
  - SONA™ IF573 SMT Module Mechanical Drawing
  - SONA™ IF573 SMT Module Pinout
- SONA™ IF573 M.2 2230 Module
  - SONA™ IF573 M.2 2230 Module Mechanical Drawing
  - SONA™ IF573 M.2 2230 Module Pinout
  - SONA™ IF573 M.2 2230 Mounting Guidelines
- RF Layout Design Guidelines

Note: Data in this document is drawn from several sources and is subject to change.

Figure 1: Sona IF573 SMT Module

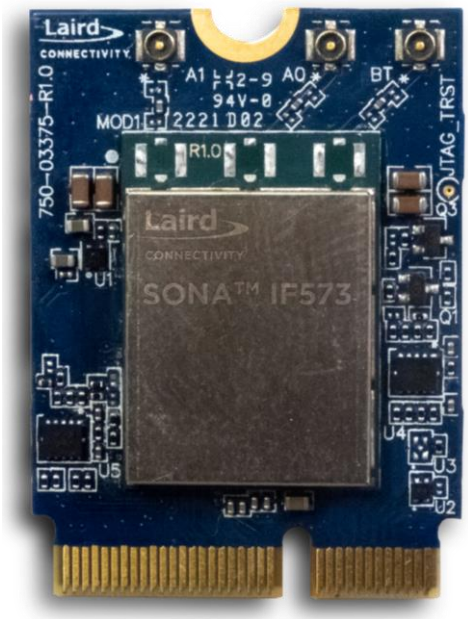

Figure 2: Sona IF573 M.2 Module

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2 SONA™ IF573 SMT MODULE

This section describes the hardware footprint, mechanical drawing and hardware pinout of the Sona IF573 M.2 1318 module. It provides details and pin assignments critical to hardware integration of the module.

Detail drawings are shown in Figure 3, Figure 4, and Figure 5.

2.1 SONA™ IF573 SMT Module PCB Footprint

Module dimensions of the Sona IF573 SMT wireless module are 18 x 13 x 1.9 mm.

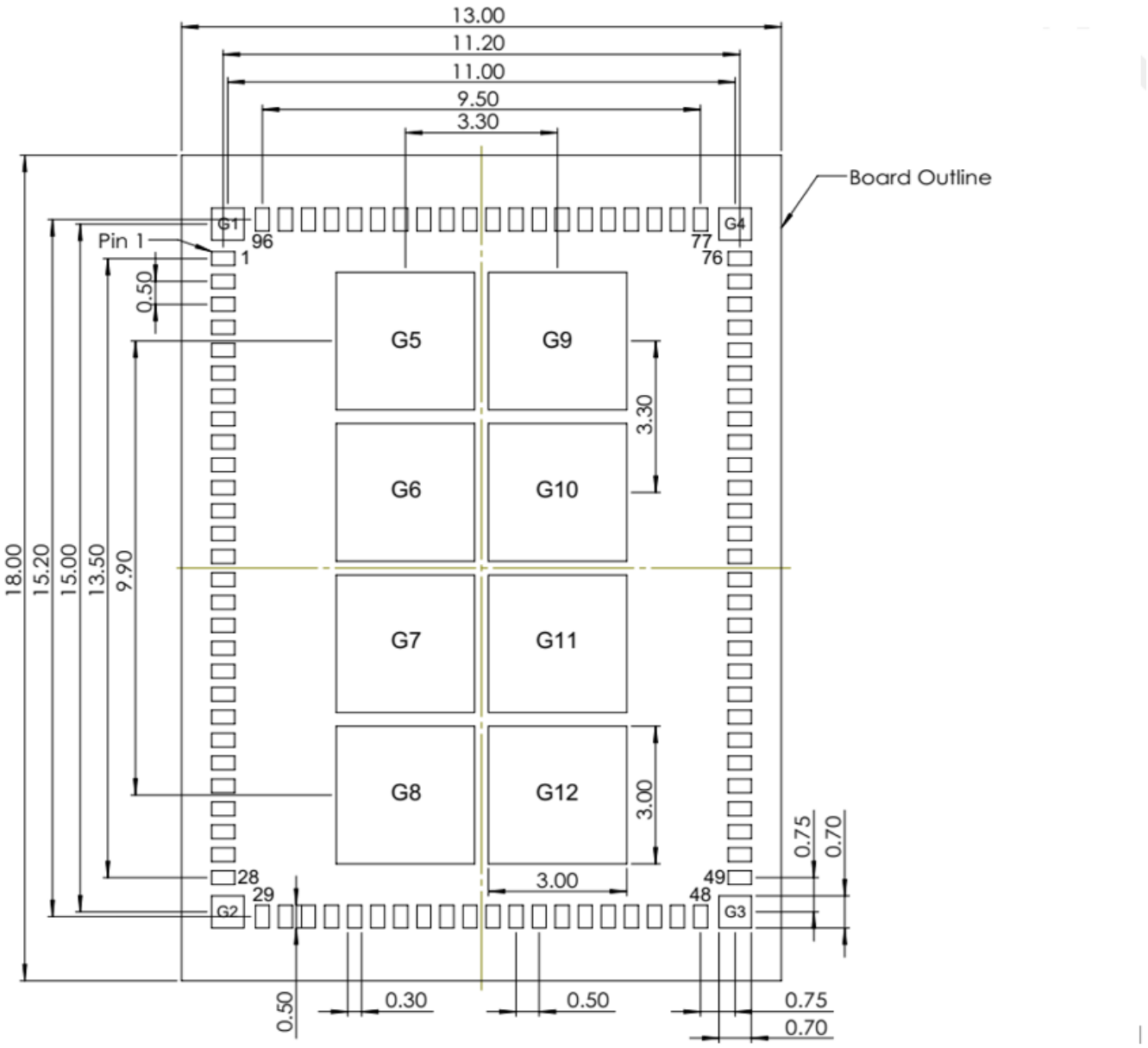

Figure 3: PCB Footprint (Bottom View) - IF573 SMT Module

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2.2 SONA™ IF573 SMT Module Mechanical Drawing

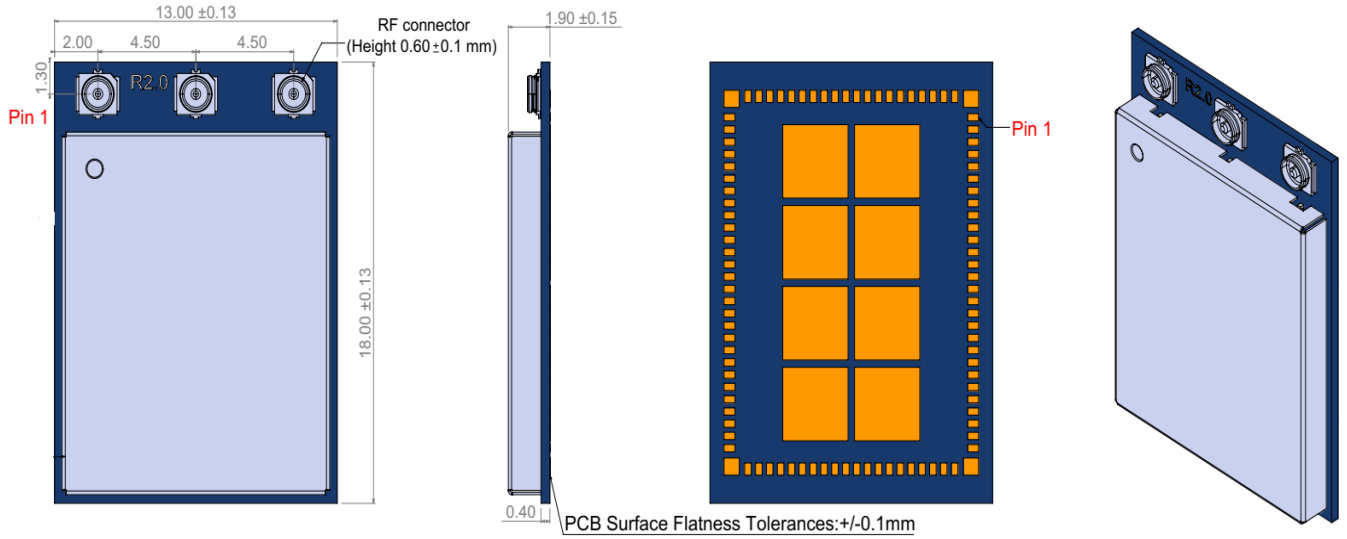

Figure 4: Mechanical Drawing - SMT module with External Antenna Connector (-SC)

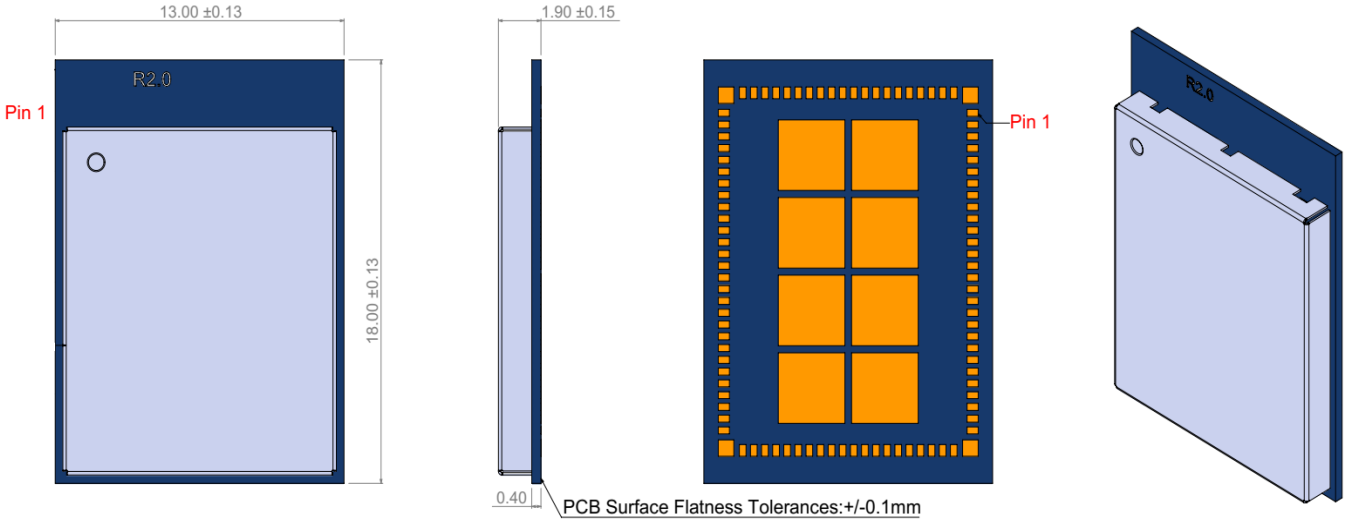

Figure 5: Mechanical Drawing - SMT module with External Antenna Connector (-ST)

Note: The Wi-Fi MAC address is located on the product label.

The last digit of Wi-Fi MAC address is assigned to either *0, 2, 4, 6, 8, A, C, E.*

The Bluetooth MAC address is the Wi-Fi MAC address plus 1.

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2.3 SONA™ IF573 SMT Module Pinout

Pin #	Name	Type	Voltage Ref.	Function	If Not Used
1	-	-	-	-	Unused
2	-	-	-	-	Unused
3	-	-	-	-	Unused
4	VBAT	PWR	3.3V	DC supply voltage for module. Operational: VBAT is 3.0V to 4.8V ** VBAT at 3.13V to 3.5V has the same TX power but a better EVM/harmonic emissions margin	-
5	VBAT	PWR	3.3V	DC supply voltage for module. Operational: VBAT is 3.0V to 4.8V ** VBAT at 3.13V to 3.5V has the same TX power but a better EVM/harmonic emissions margin	-
6	GND	-	-	Ground	GND
7	-	-	-	-	Unused
8	-	-	-	-	Unused
9	-	-	-	-	Unused
10	-	-	-	-	Unused
11	GPIO_3_WL_JTAG_TMS	O	VDDIO	JTAG test mode select	NC
12	GPIO_2_WL_JTAG_TCK	O	VDDIO	JTAG test clock	NC
13	GPIO_4_WL_JTAG_TDI	I	VDDIO	JTAG test data in	NC
14	-	-	-	-	Unused
15	-	-	-	-	Unused
16	-	-	-	-	Unused
17	GND	-	-	Ground	GND
18	LHL_GPIO1_WL_DEV_WAKE	I	VDDIO	WLAN Device Wake-up: Signal from host to the IF573 module. ** It forms the option of the “WLAN_DEV_WAKE” with the Pin22.	NC
19	GPIO_5_WL_JTAG_TDO	O	VDDIO	JTAG test data out	NC
20	GND	-	-	Ground	GND
21	LHL_GPIO0_BT_DEV_WAKE	I	VDDIO	Bluetooth Device Wake-up: Signal from host to the IF573 module. ** It forms the option of the “BT_DEV_WAKE” with the Pin66.	NC
22	GPIO_8_WL_UART_CTS	I	VDDIO	WLAN Device Wake-up: Signal from host to IF573 module. ** It forms the option of the “WLAN_DEV_WAKE” with the Pin18. Please reference the boot strapping table: **Interface** / **Pin18** / **Pin22** PCIe / X / Used SDIO / Used / X	NC
23	GND	-	-	Ground	GND
24	GPIO_1	I/O	VDDIO	WLAN interface - PCIE or SDIO option **Interface** / **Pin1** PCIe / High SDIO / Low	NC

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Pin #	Name	Type	Voltage Ref.	Function	If Not Used
25	JTAG_SEL	I	VDDIO	JTAG select input. ▪ Pull-High to select the JTAG interface ▪ Connected to ground if not used this pin	NC
26	GND	-	-	Ground	GND
27	LPO_IN	I	VDDIO	External sleep clock input (32.768 KHz)	NC
28	WL_REG_ON	I	VDDIO	Enables WLAN regulators. Internal 200K pull-down resistor that is enabled by default. Ground to disable WLAN.	-
29	PCIE_PME_L	O	VDDIO	PCI power management event out	NC
30	PCIE_CLKREQ_L	O	VDDIO	PCIe clock request signal which indicated when the “REFCLK” to the PCIe interface can be gated. ▪ 1 = the clock can be gated ▪ 0 = the clock is required	NC
31	PCIE_PERST_L	I	VDDIO	PCIe system reset.	NC
32	GND	-	-	Ground	GND
33	PCIE_REFCLKN	I	-	PCIE Differential Pair Clock Source (100 MHz) Negative Input	NC
34	PCIE_REFCLKP	I	-	PCIE Differential Pair Clock Source (100 MHz) Positive Input	NC
35	GND	-	-	Ground	GND
36	PCIE_TDN	O	-	PCIE Transmitter Differential Pair Negative Output	NC
37	PCIE_TDP	O	-	PCIE Transmitter Differential Pair Positive Output	NC
38	GND	-	-	Ground	GND
39	PCIE_RDN	I	-	PCIE Receiver Differential Pair Negative Input	NC
40	PCIE_RDP	I	-	PCIE Receiver Differential Pair Positive Input	NC
41	GND	-	-	Ground	GND
42	VDDIO	PWR	1.8V	1.8V IO Supply for WLAN GPIOs	-
43	-	-	-	-	Unused
44	-	-	-	-	Unused
45	-	-	-	-	Unused
46	GPIO_0_WL_HOST_WAKE	O	VDDIO	Host wake up. Signal from the Sona IF573.	NC
47	SDIO_DATA_3	I/O	VDDIO	SDIO Data line 3	NC
48	SDIO_DATA_2	I/O	VDDIO	SDIO Data line 2	NC
49	SDIO_DATA_1	I/O	VDDIO	SDIO Data line 1	NC
50	SDIO_DATA_0	I/O	VDDIO	SDIO Data line 0	NC
51	SDIO_CMD	I/O	VDDIO	SDIO Command Line	NC
52	SDIO_CLK	I	VDDIO	SDIO Clock Input	NC
53	BT_HOST_WAKE	O	VDDIO	Host wake up. Signal from the Sona IF573.	NC

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Pin #	Name	Type	Voltage Ref.	Function	If Not Used
54	BT_UART_CTS_N	I	VDDIO	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	NC
55	BT_UART_TXD	O	VDDIO	UART Serial Output. Serial data output for the HCI UART interface.	NC
56	BT_UART_RXD	I	VDDIO	UART Serial Input. Serial data input for the HCI UART interface.	NC
57	BT_UART_RTS_N	O	VDDIO	UART request-to-send. Active-low request-to-send signal for the HCI UART interface.	NC
58	BT_PCM_SYNC	I/O	VDDIO	PCM Sync. Supported - Master (Output) or Slave (Input).	NC
59	BT_PCM_IN	I	VDDIO	PCM data input.	NC
60	BT_PCM_OUT	O	VDDIO	PCM data output	NC
61	BT_PCN_CLK	I/O	VDDIO	PCM clock. Supported – Master (Output) or Slave (Input).	NC
62	GND	-	-	Ground	GND
63	BT_REG_ON	I	VDDIO	Enables Bluetooth regulators. Internal 200K pull-down resistor that is enabled by default. Ground to disable Bluetooth.	-
64	CPIO_13	I/O	VDDIO	Reserved for feature support	NC
65	GPIO_12	I/O	VDDIO	Bluetooth interface – UART (Pull up this pin via a 10K resistor)	NC
66	BT_DEV_WAKE	I	VDDIO	Bluetooth Device Wake-up: Signal from host to Sona IF573. ** It forms the option of the “BT_DEV_WAKE” with the Pin21.	NC
67	GPIO_6_WL_JTAG_TRST	I	VDDIO	JTAG reset input	NC
68	GND	-	-	Ground	GND
69	-	-	-	-	Unused
70	-	-	-	-	Unused
71	GND	-	-	Ground	GND
72	VBAT	PWR	3.3V	DC supply voltage for module. Operational: VBAT is 3.0V to 4.8V ** VBAT at 3.13V to 3.5V has the same TX power but a better EVM/harmonic emissions margin	-
73	VBAT	PWR	3.3V	DC supply voltage for module. Operational: VBAT is 3.0V to 4.8V ** VBAT at 3.13V to 3.5V has the same TX power but a better EVM/harmonic emissions margin	-
74~78	GND	-	-	Ground	GND
79	BT_S	I/O	-	For the Sona IF573 Trace type module – Bluetooth port	-

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Pin #	Name	Type	Voltage Ref.	Function	If Not Used
80~85	GND	-	-	Ground	GND
86	WL_C0	I/O	-	For the Sona IF573 Trace type module – WLAN port0	-
87~93	GND	-	-	Ground	GND
94	WL_C1	I/O	-	For the Sona IF573 Trace type module – WLAN port1	-
95~96	GND	-	-	Ground	GND
G1~12	GND	-	-	Ground	GND

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3 SONA™ IF573 M.2 2230 MODULE

This section describes the mechanical drawing and hardware pinout of the Sona IF573 M.2 2230 module. It provides details and pin assignments critical to hardware integration of the module.

Detail drawings are shown in Figure 6.

3.1 SONA™ IF573 M.2 2230 Module Mechanical Drawing

Module dimensions of the Sona IF573 M.2 2230 module are 22 x 30 x 2.7 mm.

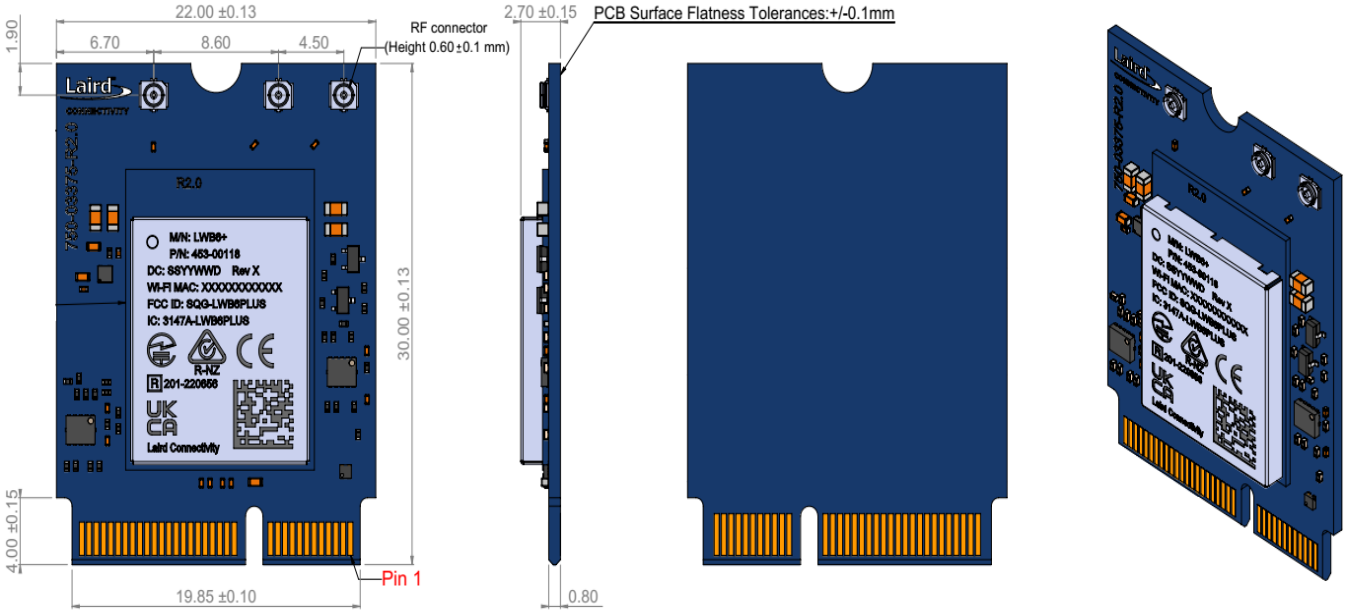

Figure 6: Mechanical Drawing – M.2 2230 module with External Antenna Connector (-SC)

Note: The Wi-Fi MAC address is located on the product label.

The last digit of Wi-Fi MAC address is assigned to either *0, 2, 4, 6, 8, A, C, E.*

The Bluetooth MAC address is the Wi-Fi MAC address plus 1.

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3.2 SONA™ IF573 M.2 2230 Module Pinout

Pin #	Name	Type	Voltage Ref.	Function	If Not Used
1	GND	-	-	Ground	GND
2	3.3V	PWR I/P	3.3V	DC supply voltage for module. ** VBAT at 3.13V to 3.5V has the same TX power but a better EVM/harmonic emissions margin	-
3	USB_D+	-	-	NC	Unused
4	3.3 V	PWR I/P	3.3 V	DC supply voltage for module. ** VBAT at 3.13V to 3.5V has the same TX power but a better EVM/harmonic emissions margin	-
5	USB_D-	-	-	NC	Unused
6	LED1#	O	3.3V	Reserved for the GPIO12	NC
7	GND	-	-	Ground	GND
8	PCM_CLK	I/O	1.8V	PCM clock. Can be master (Output) or slave (Input)	NC
9	SDIO CLK	I	1.8V	SDIO clock input	NC
10	PCM_SYNC	I/O	1.8V	PCM Sync. Can be master (Output) or slave (Input)	NC
11	SDIO CMD	I/O	1.8V	SDIO command line	NC
12	PCM_OUT	O	1.8V	PCM data output.	NC
13	SDIO DATA0	I/O	1.8V	SDIO data lin0	NC
14	PCM_IN	I	1.8V	PCM data input.	NC
15	SDIO DATA1	I/O	1.8V	SDIO data lin1	NC
16	LED2#	O	3.3V	Reserved for the GPIO13	NC
17	SDIO DATA2	I/O	1.8V	SDIO data lin2	NC
18	GND	-	-	Ground	GND
19	SDIO DATA3	I/O	1.8V	SDIO data lin3	NC
20	UART WAKE#	O	3.3 V	Reserved for feature support BT_HOST_WAKE. Output signal to wake up Host.	NC
21	SDIO WAKE#	I	1.8V	Reserved for feature support Reserved for WL_HOST_WAKE. Output signal to wake up host.	NC
22	UART_TXD	O	1.8V	Serial data output for the HCI UART interface.	NC
23	SDIO RESET#	-	-	NC	Unused
32	UART_RXD	I	1.8V	Serial data input for the HCI UART interface.	NC
33	GND	-	-	Ground	GND
34	UART_RTS	O	1.8V	Active-Low request-to-send signal for the HCI UART interface.	NC
35	PERp0	I	-	PCIE Receiver Differential Pair Positive Input	NC
36	UART_CTS	I	1.8V	Active-Low clear-to-send signal for the HCI UART interface.	NC

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Pin #	Name	Type	Voltage Ref.	Function	If Not Used
37	PERn0	I	-	PCIE Receiver Differential Pair Negative Input	NC
38	VENDOR DEFINED38	O	1.8V	Reserved for feature support JTAG_TDO. JTAG test data output	NC
39	GND	-	-	Ground	GND
40	VENDOR DEFINED40	I	1.8V	Reserved for feature support WL_DEVICE_WAKE. Input signal from host to wake up WLAN module.	NC
41	PETp0	O	-	PCIE Transmitter Differential Pair Positive Output	NC
42	VENDOR DEFINED42	I/O	1.8V	Reserved for feature support Reserved for BT_DEVICE_WAKE. Input signal from host.	NC
43	PETn0	O	-	PCIE Transmitter Differential Pair Negative Output	NC
44	COEX3	I	1.8 V	Reserved for feature support. JTAG_TDI. JTAG test data input.	NC
45	GND	-	-	Ground	GND
46	COEX2	O	1.8 V	Reserved for feature support JTAG_TCK. JTAG test clock	NC
47	REFCLKp0	I	-	PCIE Differential Pair Clock Source (100 MHz) Positive Input	NC
48	COEX1	I/O	1.8 V	Reserved for feature support. JTAG_TMS. JTAG test mode selection.	NC
49	REFCLKn0	I	-	PCIE Differential Pair Clock Source (100 MHz) Negative Input	NC
50	SUSCLK	I	3.3 V	External Sleep Clock input (32.768KHz) The sleep clock is always needed for using this module	-
51	GND	-	-	Ground	GND
52	PERST0#	I	3.3 V	PCIE system reset	NC
53	CLKREQ0#	O	3.3 V	PCIe clock request signal which indicated when the “REFCLK” to the PCIe interface can be gated. 1 = the clock can be gated 0 = the clock is required	NC
54	W_DISABLE2#	I	3.3 V	Enables Bluetooth regulators. Internal 200K pull-down resistor that is enabled by default. Ground to disable Bluetooth.	NC
55	PEWAKE0#	0	3.3 V	PCI power management event out	NC
56	W_DISABLE1#	I	3.3 V	Enables WLAN regulators. Internal 200K pull-down resistor that is enabled by default. Ground to disable WLAN.	NC
57	GND	-	-	Ground	GND

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Pin #	Name	Type	Voltage Ref.	Function	If Not Used
58	I2C DATA	-	-	NC	NC
59	RESERVED	-	-	NC	NC
60	I2C CLK	-	-	NC	NC
61	RESERVED	-	-	NC	NC
62	ALERT#	-	-	NC	NC
63	GND	-	-	Ground	GND
64	RESERVED	-	-	NC	NC
65	RESERVED	-	-	NC	NC
66	UIM_SWP	-	-	NC	NC
67	RESERVED	-	-	NC	NC
68	UIM_POWER_SNK	-	-	NC	NC
69	GND	-	-	Ground	GND
70	UIM_POWER_SRC	-	-	NC	NC
71	RESERVED	-	-	NC	NC
72	3.3V	PWR I/P	3.3V	DC supply voltage for module. ** VBAT at 3.13V to 3.5V has the same TX power but a better EVM/harmonic emissions margin	--
73	RESERVED	-	-	NC	NC
74	3.3V	PWR I/P	3.3V	DC supply voltage for module. ** VBAT at 3.13V to 3.5V has the same TX power but a better EVM/harmonic emissions margin	--
75	GND	-	-	Ground	GND

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3.3 SONA™ IF573 M.2 2230 Mounting Guidelines

The Sona IF573 M.2 module connects to the host via a standard PCI EXPRESS M2 connector. The Kyocera's (www.Kyocera-connector.com) 6411 series provide 1.8 mm, 2.3 mm and 3.2 mm connector heights and JAE's (https://www.jae.com/en/) SM3 series provide 1.2 mm, 2.15 mm, 3.1 mm and 4.1 mm connector heights.

Because the Sona IF573 M.2 module is a single-side component module, we recommend the following part numbers which have 2.3 mm and 3.1 mm connector height):

M.2 Key-E Connector	Connector Height
KYOCERA 24-6411-067-101-894E	2.3 mm
JAE SM3ZS067U310AERxxxx	3.1 mm

The stand-off mating to the recommend 2.3 mm connector from EMI STOP (www.EMISTOP.com) is part number **F50M16-041525P1D4M** and 3.1mm from JAE (https://www.jae.com/en/) is part number **SM3ZS067U310-NUT1-Rxxxx**.

M.2 Key-E Connector	Stand-off
KYOCERA 24-6411-067-101-894E	EMI STOP F50M16-041525P1D4M
JAE SM3ZS067U310AERxxxx	JAE SM3ZS067U310-NUT1-Rxxxx

Detailed layout and stencil opening are shown as follows in Figure 7.

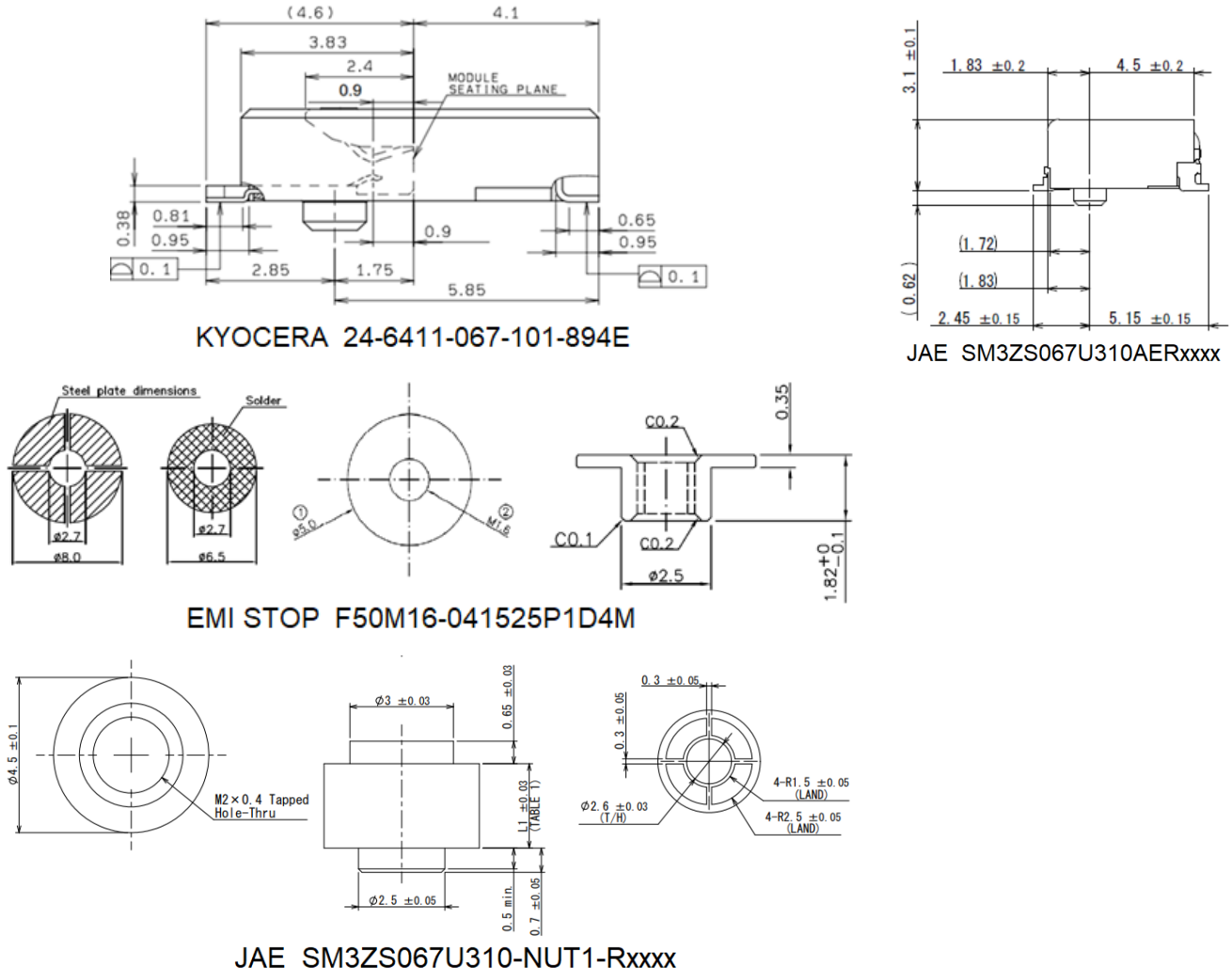

Figure 7: Mounting information of the Sona IF573 M.2 module and recommended layout pattern for the stand-off

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4 RF Layout Design Guidelines

The following is a list of RF layout design guidelines and recommendation when installing a Laird Connectivity radio into your device.

- Do not run antenna cables directly above or directly below the radio.
- Do not place any parts or run any high-speed digital lines below the radio.
- Ensure that there is the maximum allowable spacing separating the antenna connectors on the Laird Connectivity radio from the antenna. In addition, do not place antennas directly above or directly below the radio.
- Laird Connectivity recommends the use of a double-shielded cable for the connection between the radio and the antenna elements.
- Be sure to put a 10uF/16V/0603 capacitor on EACH 3.3V power pin. Also, place that capacitor to the pin as close as possible to make sure the internal PMU working correctly.
- Use proper electro-static-discharge (ESD) procedures when installing the Laird Connectivity radio module. To avoid negatively impacting Tx power and receiver sensitivity, do not cover the antennas with metallic objects or components.
- Laird Connectivity's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.
- The modules are designed to meet the needs of commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

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5 Revision History

Version	Date	Notes	Contributor(s)	Approver
1.0	23 Oct 2023	Initial Release	Andrew Chen Jacky Kuo	Andy Ross
1.1	26 Jan 2024	Updated description of pins 28 and 63 in SONA™ IF573 SMT Module Pinout	Jacky Kuo	Andy Ross
1.2	23 Feb 2024	Updated SONA™ IF573 SMT Module Pinout with detail on pins G1-G12	Jacky Kuo	Andrew Chen

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