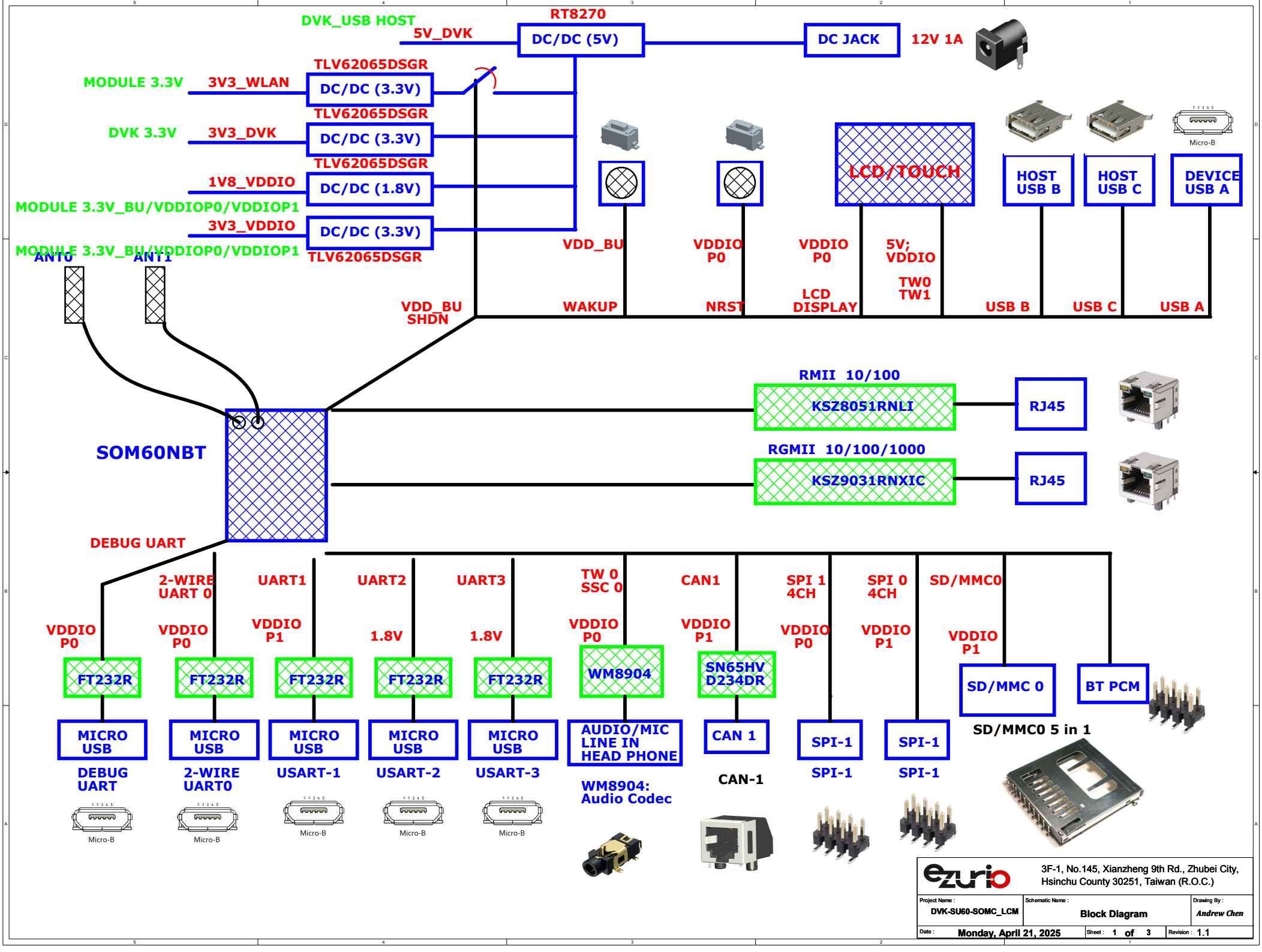


ezurio

3F-1, No.145, Xianzheng 9th Rd., Zhubei City, Hsinchu County 30251, Taiwan (R.O.C.)

Project Name :	Schematic Name :	Drawing By :
DVK-SU60-SOMC_LCM	Block Diagram	*Andrew Chen*

Date :	Sheet :	Revision :
Monday, April 21, 2025	1 of 3	1.1

DATE	REVISION NUMBER	INITIALS	Initial Release
2017/07/07	A0	ANDREW CHEN	Initial for EVT design review
2017/07/17	A0	ANDREW CHEN	update after design review (1) Correct MOS FET (2) Correct 2-wire UART loop back mode (3) Correct SDIO connector. (4) Add JTAG connector (5) Add Antenna Holder
2017/07/27	A0	ANDREW CHEN	Change (1) remove SDIO_Data 4-8 (2) Change 1V8_SDIO to 1v8_UART2_3. (3) cahnge CAN 5V to 5V_DVK2
2017/08/03	A0	ANDREW CHEN	(1) enable FDTI chip can set in RESET mode (2) Add pin-header for SDIO power (3) Add pin-header for 5V USB Host. (4) Correct MIC design (5) Add BIG hole (6) Add pin-header on 5V (7) detail 12V input.
2018/03/20	B0	ANDREW CHEN	(1) Change U12 to MX25R4035FM1IL0 for SPI0 (2) Change R222,R279 to 30.1K ohm 1% to get correct 5V (3) Change C192 to 1uF (0402) to delay the NRST reset. (4) Remove U18 and uisng Q13 to solve the VBUS_SENS (5) Correct the USB port assignment. USB A for device (6) Change FB2 to 0ohm (0603) to reduce the ripple when running i-perf (7) Y1,Y2 change to E2SB25E00000LE; C26=15pF,C27=12pF; C45=C46=10pF for better accuracy. (8) Change SW1, SW2 to TS-03M-ASM-T-T/R (SMT type) (9) Adding Q8 and change Q3 to PCH to solve the USB VBUS_EN issue (10) adding Q9 and change Q5 to PCH to solve the SDIO power control issue (11) Remove U13 and adding Q10 for SDIO card detedt function. Also change eMMC_CD to "H" acive. (12) add Q11/Q12 and change Q6/Q7 to PCH in orderto fix the LED EVL circuit when VDDIO=1.8V (13) Change R209/R210 to 59Kohm. Fix the level shifter voltage. (14) Debug UART powered by the 5V from DVK to solve the first power on issue without plug debug port to USB. (15) Add FB93 to enhance the ESD for Audio
2018/04/09	B0	ANDREW CHEN	Seperate the DVK-60-SOMC-LCM design from DVK-60-SOMC
2018/08/16	1.0	ANDREW CHEN	Issue for MP
2025/4/21	1.1	AL	Replace brand to Ezurio

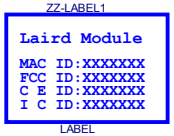
PCB design specification

1. Substrate: FR4 ROHS compliant, High TG 190 degree.
2. Solder mask, color=GREEN, Silkscreen color=WHITE
3. Surface finish to be Immersion Nickel/Gold (ENIG) with 1-2 u"
4. Start with 1 oz. copper on all layers.

ZZ-PCB1

PCB

ZZ-LABEL1



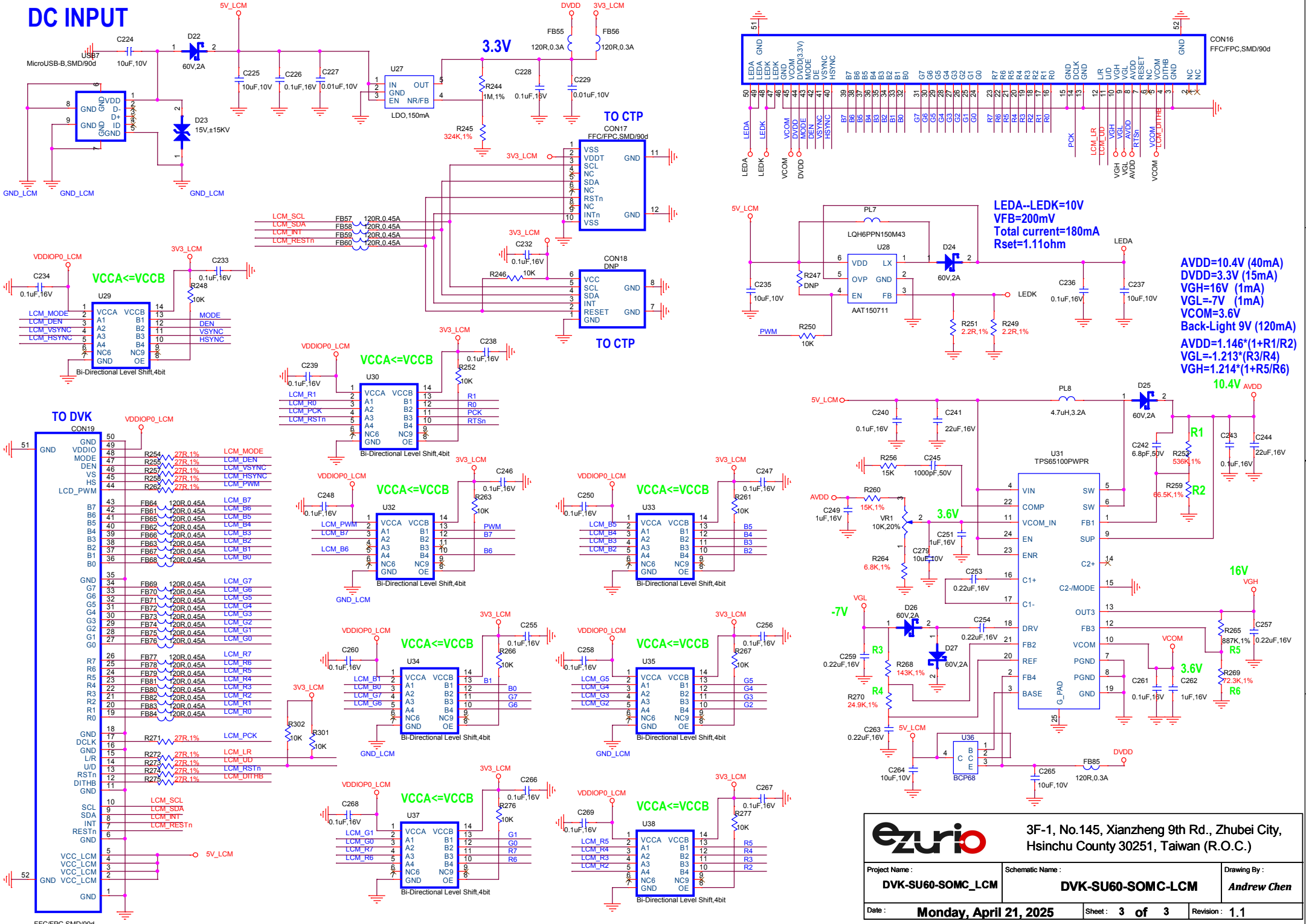
LABEL

ezurio
3F-1, No.145, Xianzheng 9th Rd., Zhubei City,
Hsinchu County 30251, Taiwan (R.O.C.)

Project Name :	Schematic Name :	Drawing By :
DVK-SU60-SOMC_LCM	History	Andrew Chen

Date :	Sheet :	Revision :
Monday, April 21, 2025	2 of 3	1.1

DC INPUT


USB7
MicroUSB-B,SMD/90d
C224
10uF,10V
D22
60V,2A
D23
15V,±15KV
5V_LCM
C225
10uF,10V
C226
0.1uF,16V
C227
0.01uF,10V
U27
LDO,150mA
3.3V
R244
1M,1%
R245
324K,1%
DVDD
3V3_LCM
FB55
120R,0.3A
FB56
120R,0.3A
C228
0.1uF,16V
C229
0.01uF,10V
GND_LCM
TO CTP
CON17
FFC/FPC,SMD/90d
CON18
DNP
LCM_SCL
LCM_SDA
LCM_INT
LCM_RESTn
FB57
FB58
FB59
FB60
120R,0.45A
C232
0.1uF,16V
R246
10K
VDDIOP0_LCM
C234
0.1uF,16V
VCCA<=VCCB
U29
C233
0.1uF,16V
R248
10K
LCM_MODE
LCM_DEN
LCM_VSYNC
LCM_HSYNC
MODE
DEN
VSYNC
HSYNC
Bi-Directional Level Shift,4bit
TO DVK
CON19
FFC/FPC,SMD/90d
R254
R255
R256
R258
R262
27R,1%
LCM_MODE
LCM_DEN
LCM_VSYNC
LCM_HSYNC
LCM_PWM
LCD_PWM
FB64
FB61
FB65
FB62
FB66
FB63
FB67
FB68
LCM_B7
LCM_B6
LCM_B5
LCM_B4
LCM_B3
LCM_B2
LCM_B1
LCM_B0
FB69
FB70
FB71
FB72
FB73
FB74
FB75
FB76
LCM_G7
LCM_G6
LCM_G5
LCM_G4
LCM_G3
LCM_G2
LCM_G1
LCM_G0
FB77
FB78
FB79
FB81
FB80
FB82
FB83
FB84
LCM_R7
LCM_R6
LCM_R5
LCM_R4
LCM_R3
LCM_R2
LCM_R1
LCM_R0
R271
R272
R273
R274
R275
LCM_PCK
LCM_LR
LCM_UD
LCM_RSTn
LCM_DITHB
R302
R301
10K
SCL
SDA
INT
RESTn
VCC_LCM
U30
U32
U33
U34
U35
U36
U37
U38
R252
R263
R261
R266
R267
R276
R277
R1
R0
PCK
RTSn
B5
B4
B3
B2
B1
B0
G5
G4
G3
G2
G1
G0
R5
R4
R3
R2
BCP68
CON16
FFC/FPC,SMD/90d
LEDA--LEDK=10V
VFB=200mV
Total current=180mA
Rset=1.11ohm
PL7
LQH6PPN150M43
U28
AAT150711
D24
60V,2A
R247
DNP
R250
10K
R251
2.2R,1%
R249
2.2R,1%
C235
10uF,10V
C236
0.1uF,16V
C237
10uF,10V
LEDK
PWM
AVDD=10.4V (40mA)
DVDD=3.3V (15mA)
VGH=16V (1mA)
VGL=-7V (1mA)
VCOM=3.6V
Back-Light 9V (120mA)
AVDD=1.146*(1+R1/R2)
VGL=-1.213*(R3/R4)
VGH=1.214*(1+R5/R6)
PL8
4.7uH,3.2A
D25
60V,2A
10.4V
AVDD
C240
0.1uF,16V
C241
22uF,16V
C242
6.8pF,50V
R253
536K,1%
R1
C243
0.1uF,16V
C244
22uF,16V
R256
15K
C245
1000pF,50V
U31
TPS65100PWPR
R260
15K,1%
VR1
10K,20%
3.6V
R259
66.5K,1%
R2
C249
1uF,16V
C251
1uF,16V
C279
10uF,10V
R264
6.8K,1%
C253
0.22uF,16V
16V
VGH
-7V
VGL
D26
60V,2A
D27
60V,2A
C254
0.22uF,16V
R3
R4
R268
143K,1%
R270
24.9K,1%
C259
0.22uF,16V
C263
0.22uF,16V
R265
887K,1%
R5
R269
72.3K,1%
R6
C257
0.22uF,16V
C261
0.1uF,16V
C262
1uF,16V
C264
10uF,10V
C265
10uF,10V
FB85
120R,0.3A
DVDD
G_PAD
3F-1, No.145, Xianzheng 9th Rd., Zhubei City,
Hsinchu County 30251, Taiwan (R.O.C.)
Project Name :
DVK-SU60-SOMC_LCM
Schematic Name :
DVK-SU60-SOMC-LCM
Drawing By :
Andrew Chen
Date :
Monday, April 21, 2025
Sheet : 3 of 3
Revision : 1.1