Datasheet

SSD50NBT

Version 3.0

Revision History

Version	Date	Notes	Contributor	Approver
1.0	27 Mar 2016	Initial Version	Andrew Chen	Andrew Chen
1.1	09 May 2016	Fixed module size error; updated OS support	Jay White	Jay White
1.2	30 June 2016	Changed document name from HIG to Datasheet Updated current consumption numbers for MIMO; removed Single Stream(SISO) references	Andrew Chen	Andrew Chen
1.3	07 Sept 2016	Updated EU Declaration of Conformity	Sue White	Sue White
1.4	03 Nov 2016	Updated Tx power numbers to the following: 6 Mbps 18 dBm (63 mW) 54 Mbps 15 dBm (32 mW) 6 Mbps 16 dBm (40 mW) 54 Mbps 15 dBm (32 mW) 6.5 Mbps (MCS0;HT20) 18 dBm (63 mW) 65 Mbps (MCS7;HT20) 14 dBm (25 mW) (MCS0;HT40) 15 dBm (32 mW) (MCS7; HT40) 12 dBm (16 mW) 6.5 Mbps (MCS0;HT20) 16 dBm (40 mW) 65 Mbps (MCS7;HT20) 13 dBm (20 mW) (MCS0;HT40) 15 dBm (32 mW) (MCS7; HT40) 12 dBm (16 mW)	Andrew Chen	Andrew Chen
1.5	08 Nov 2016	Updated to add section numbers.	Sue White	Sue White
1.6	09 Dec 2014	Removed *Preliminary* references	Jay White	Jay White
1.7	06 Feb 2017	Added Packaging section	Andrew Chen	Andrew Chen
1.8	07 Feb 2017	Removed duplicate section re: Reflow	Andrew Chen	Andrew Chen
1.9	10 Mar 2017	Updated 5 GHz frequency bands and operating channels info.	Kris Sidle	Kris Sidle
1.10	03 Apr 2017	Removed M2US50NBT references	Andrew Chen	Andrew Chen
1.11	1 May 2017	OS Support	Jay White	Jay White
1.12	15 June 2017	Updated EU DoC with new RED standards	Tom Smith	Tom Smith
1.13	18 Aug 2017	Removed 802.11r references	Jay White	Jay White
1.14	01 May 2018	Updated product photo Updated Industry Canada statement Updated to new Laird template	Maggie Teng	Maggie Teng
1.15	06 Mar 2019	Updated logos and URLs	Sue White	Sue White
1.16	10 Jan 2020	Added Channel 144 to the FCC channels	Maggie Teng	Maggie Teng
1.17	04 Sept 2020	Updated EU regulatory section with new standards	Ryan Urness	Ryan Urness
1.18	21 Oct 2020	Updated regulatory information	Ryan Urness	Ryan Urness
2.0	21 Feb 2021	Move all detailed regulatory information to separate document	Jonathan Kaye	Jonathan Kaye
3.0	2 May 2025	Ezurio Rebranding and update MSL from 3 to 4	Dave Drogowski	Jonathan Kaye

Contents

1 Scope

This document describes key hardware aspects of the Ezurio SSD50NBT system in package (SIP) modules providing SDIO interface for WLAN connection and UART/PCM for Bluetooth® connection. This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from a number of sources and includes information found in the Qualcomm Atheros (QCA) QCA6004 and Cambridge Silicon Radio Ltd. (CSR) CSR8811 A08 data sheets issued in July 2011, along with other documents provided from QCA and CSR.

Note that the information in this document is subject to change. Please refer to the SSD50NBT product page for the most recent documentation.

2 Introduction

2.1 General Description

The SSD50NBT SIP module is an integrated, small form factor 2x2 MIMO 802.11 a/b/g/n WLAN plus *Bluetooth* 4.0 dual mode device that is optimized for low-power mobile devices. The integration of all WLAN and *Bluetooth* functionality in a single package supports low cost and simple implementation along with flexibility for platform-specific customization.

This device is pre-calibrated and integrates the complete transmit/receive RF paths including baluns, mobile phone coexistence band pass filter, diplexer, switches, power amplifier, low noise amplifier, and reference crystal oscillator.

The SSD50NBT device supports Bluetooth 2.1 + EDR and Bluetooth 4.0 (Bluetooth Low Energy or BLE). The device's low power consumption radio architecture and proprietary power save technologies allow for extended battery life.

In addition, its dual 802.11 and Bluetooth radio includes full digital MAC and baseband engines that handle all 802.11 CCK/OFDM® 2.4/5GHz, and Bluetooth basic rate and EDR baseband and protocol processing.

Dual embedded low-power CPU cores minimize host loading and maximize flexibility to support customer specific use cases.

3 SSD50NBT Features Summary

The Ezurio SSD50NBT device features are described in Table 1.

Table 1: SSD50NBT features

Feature	Description
Radio Front End	Integrates the complete transmit/receive RF paths including baluns, coexistence band pass filter, diplexer, switches, power amplifier, low noise amplifier, and reference crystal oscillator.
Enhanced WLAN/BT Coexistence Algorithms	Enhanced important use cases including: • PCM/I2S digital audio interface • BT stereo audio (A2DP) • BT data transfer profiles (such as OPP and FTP) • BT2.1+EDR • BT-LE Flexible radio architecture ensures simple customization for future use cases.
Power Management	Uses power-saving techniques including: • Gating clocks to idle or inactive blocks • Fast start and settling circuits to reduce Tx power • Active duty cycles • CPU frequency scaling
Pre-Calibration	RF system tested and calibrated in production.
Internal Sleep Clock	Integrated on-chip low power sleep clock to regulate internal timing.
Multiple Interface Support	• SDIO 2.0 (50 MHz, 4-bit and 1-bit) WLAN • HS-UART for Bluetooth HCI (compatible with any upper layer Bluetooth stack)
Advanced 802.11n	• Half Guard Interval and Frame Aggregation for high throughput • Space Time Block Coding (STBC) Rx for improved downlink robustness over range • Low Density Parity Check (LDPC) for improved uplink and downlink robustness over range
Reference Frequency	• Incorporates a 26 MHz reference frequency source in package • Sleep regulated and gated to enable the internal crystal to be powered down when the device is in sleep mode • BT shares the clock from the Wi-Fi chip • Wi-Fi cannot be turned off or in reset when running BT
Advanced WLAN	Includes the following advanced WLAN features: • IEEE 802.11e QoS, Wi-Fi Alliance WMM Power Save, and 802.11n power saving compliance • AES, AES-CCMP, TKIP engines for faster data encryption • Cisco CCXv4 ASD, WPS support • Standard WEP/WPA/WPA2 for personal and enterprise environments support • WWR, 802.11d, 802.11h support • Wi-Fi Direct (Peer-to-Peer) • RTT for indoor positioning • Statistics and events for monitoring • Self-managed power state handling • Self-contained beacon processing • Shared authentication • Ad-hoc power save • Multiple PMK ID support • Simulated UAPSD • T-Spec support • Production flow diagnostics • 3-wire scheme for Wi-Fi and BT coexistence.
Host Offloading (WLAN)	Integrates extensive hardware signal processing and an embedded on-chip CPU to offload complete 11n MAC/BB/PHY processing to minimize host processor loading and support application specific customization.

- High-speed UART port (up to 4 Mbps)
- HFP v1.6 wide-band speech supported on-chip
- On-chip encoding of SBC and aptX® codecs for A2DP music streaming
- PCM/I2S digital audio interface
- Support for IEEE 802.11 coexistence
- The flexible RAM/ROM based architecture enables custom or future profiles to be easily added.

4 Specifications

Table 2: Specifications

Feature	Description
Physical Interface	64-pin LGA package
Wi-Fi Interface	1-bit or 4-bit Secure Digital I/O
Bluetooth Interface	Host Controller Interface (HCI) using High Speed UART
Main Chip	Wi-Fi: Qualcomm Atheros QCA6004 BT: Cambridge Silicon Radio Ltd. (CSR) CSR8811 A08
Input Voltage Requirements	3.3 VDC (3.20V min to 3.46V max)
I/O Signaling Voltage	3.3 VDC ± 5% or 1.8 VDC ± 5%
Average Current Consumption, VDDIO = 3.3 volts (At maximum transmit power setting) ***Note:*** *Reset refers to the radio are in reset, both Wifi and BT reset are asserted.*	MIMO 802.11a (with BT in standby) @ 18 dBm 6 Mbps Transmit: 900 mA Receive: 260 mA Reset: 0.13 mA 802.11b (with BT in standby) @ 18 dBm 1 Mbps Transmit: 680 mA Receive: 250 mA Reset: 0.13 mA 802.11g (with BT in standby) @ 18 dBm 6 Mbps Transmit: 710 mA Receive: 250 mA Reset: 0.13 mA 802.11n (2.4 GHz) (with BT in standby) @ 14 dBm MCS7 Transmit: 460 mA Receive: 250mA Reset: 0.13 mA 802.11n (5 GHz) (with BT in standby) @ 14 dBm MCS7 Transmit: 720 mA Receive: 260 mA Reset: 0.13 mA Bluetooth (with Wi-Fi in standby) Transmit: 85 mA Receive: 70 mA Reset: 0.13 mA

Feature	Description
Operating Temperature	-30° to 85°C (-22° to 185°F)
Operating Humidity	10 to 90% (non-condensing)
Storage Temperature	-40° to 85°C (-40° to 185°F)
Storage Humidity	10 to 90% (non-condensing)
Maximum Electrostatic Discharge	Conductive 4KV; Air coupled 8KV
Size	15 mm (length) x 15 mm (width) x 2.5 mm (thickness)
Weight	1.20 g
Mounting	Please see the mounting and handling guide.
Wi-Fi Media	Direct Sequence-Spread Spectrum (DSSS) Complementary Code Keying (CCK) Orthogonal Frequency Divisional Multiplexing (OFDM)
Bluetooth Media	Frequency Hopping Spread Spectrum (FHSS)
Wi-Fi Media Access Protocol	Carrier sense multiple access with collision avoidance (CSMA/CA)
Network Architecture Types	Infrastructure and ad-hoc
Wi-Fi Standards	IEEE 802.11a, 802.11b, 802.11d, 802.11e, 802.11g, 802.11h, 802.11i, 802.11n
Bluetooth Standards	*Bluetooth* version 2.1 with Enhanced Data Rate *Bluetooth* 4.0 (Bluetooth Low Energy or BLE)
Wi-Fi Data Rates Supported	11a (OFDM) 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11b (DSSS, CCK) 1, 2, 5.5, 11 Mbps 802.11g (OFDM) 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n (OFDM, MCS 0-15) Full Guard Interval: 6.5,13.0, 19.5, 26.0,39.0,52.0,58.5,65.0, 13.0,26.0,39.0, 52.0, 78.0,104.0,117.0 Mbps Short Guard Interval: 1.2,14.4,21.7,29.9,43.3,57.8,65.0,72.2, 14.4,28.9,43.3,57.8, 86.7,115.6,130.0,144.4 Mbps
Modulation	BPSK @ 1, 6,9, 6.5, 7.2,13 and 14.4 Mbps QPSK @ 2, 12, 18, 13, 14.4,19.5, 21.7, 26, 28.9, 39,43.3 Mbps CCK @ 5.5 and 11 Mbps 16-QAM @ 24, 36,26, 29.9,39,43.3,52,57.8,78,86.7 Mbps 64-QAM @ 48,54,52, 57.8, 58.5, 65,72.2,104.0,115.6,117.0,130.0,144.4 Mbps
802.11n Spatial Streams	2 (2x2 MIMO)
Bluetooth Data Rates Supported	1, 2, 3 Mbps
Bluetooth Modulation	GFSK@ 1 Mbps Pi/4-DQPSK@ 2 Mbps 8-DPSK@ 3 Mbps
Regulatory Domain Support	FCC EU ISED Canada MIC (Japan) KC (Korea)

Feature	Description
2.4 GHz Frequency Bands	**EU:** 2.4 GHz to 2.483 GHz **FCC:** 2.4 GHz to 2.473 GHz **MIC:** 2.4 GHz to 2.495 GHz **KC:** 2.4 GHz to 2.483 GHz
2.4 GHz Operating Channels (Wi-Fi)	**EU:** 13 (3 non-overlapping) **FCC:** 11 (3 non-overlapping) **MIC:** 14 (4 non-overlapping) **KC:** 13 (3 non-overlapping)
5 GHz Frequency Bands	**EU** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/132/136/140) **FCC** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/ 132/136/140/144) 5.725 GHz to 5.825 GHz (Ch 149/153/157/161/165) **MIC (Japan)** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124/128/ 132/136/140) **KC** 5.15 GHz to 5.35 GHz (Ch 36/40/44/48/52/56/60/64) 5.47 GHz to 5.725 GHz (Ch 100/104/108/112/116/120/124) 5.725 GHz to 5.825 GHz (Ch 149/153/157/161)
5 GHz Operating Channels (Wi-Fi)	EU:19 non-overlapping) MIC: 19 non-overlapping FCC: 24 non-overlapping KC: 19 non-overlapping
Transmit Power ***Note:*** *Transmit power on each channel varies according to individual country regulations. All values for lowest data rate is nominal, +/-2 dBm. Others are +/-2.5 dBm.* ***Note:*** *HT40 – 40 Mhz-wide channels* *HT20 – 20 MHz-wide channels*	802.11a (UNII-1, UNII-2A, UNII-2C) or CH 36 – CH 140 6 Mbps 18 dBm (63 mW) 54 Mbps 15 dBm (32 mW) 802.11a (UNII-3) or CH 148 – CH 165 6 Mbps 16 dBm (40 mW) 54 Mbps 15 dBm (32 mW) 802.11b 1 Mbps 18 dBm (63 mW) 11 Mbps 18 dBm (63 mW) 802.11g 6 Mbps 18 dBm (63 mW) 54 Mbps 15 dBm (32 mW) 802.11n (2.4 GHz) 6.5 Mbps (MCS0) 18 dBm (63 mW) 65 Mbps (MCS7) 14 dBm (25 mW) 802.11n (5 GHz) (UNII-1, UNII-2A, UNII-2C) or CH 36 – CH 140 6.5 Mbps (MCS0;HT20) 18 dBm (63 mW) 65 Mbps (MCS7;HT20) 14 dBm (25 mW) (MCS0;HT40) 15 dBm (32 mW) (MCS7; HT40) 12 dBm (16 mW)

Feature	Description		
	802.11n (5 GHz) (UNII-3) or CH 148 – CH 165		
	6.5 Mbps (MCS0;HT20)		16 dBm (40 mW)
	65 Mbps (MCS7;HT20)		13 dBm (20 mW)
	(MCS0;HT40)		15 dBm (32 mW)
	(MCS7; HT40)		12 dBm (16 mW)
	Bluetooth		
	1 Mbps		6 dBm (4 mW)
	2 Mbps		6 dBm (4 mW)
	3 Mbps		3 dBm (2 mW)
Typical Receiver Sensitivity ***Note:*** *All values nominal, +/-3 dBm.*	802.11a:		
	6 Mbps	-93 dBm	
	54 Mbps	-75 dBm (PER < = 10%)	
	802.11b:		
	1 Mbps	-95 dBm	
	11 Mbps	-88 dBm (PER < = 10%)	
	802.11g:		
	6 Mbps	-92 dBm	
	54 Mbps	-75 dBm (PER < = 10%)	
	802.11n (2.4 GHz)		
	MCS0 Mbps	-92 dBm	
	MCS7 Mbps	-72 dBm	
	802.11n (5 GHz)		
	MCS0 Mbps	-93 dBm	
	MCS7 Mbps	-72 dBm	
	Bluetooth:		
	1 Mbps	-84 dBm	(1DH1)
	3 Mbps	-76 dBm	(3DH5)
	BLE	-87 dBm	
Operating Systems Supported	Linux 2.6.x, 3.x.x, 4.0.x kernel Android 4.1.2 (Jellybean) and forward		

Feature	Description	
Security	Standards	
	Wireless Equivalent Privacy (WEP)	
	Wi-Fi Protected Access (WPA)	
	IEEE 802.11i (WPA2)	
	Encryption	
	Wireless Equivalent Privacy (WEP, RC4 Algorithm)	
	Temporal Key Integrity Protocol (TKIP, RC4 Algorithm)	
	Advanced Encryption Standard (AES, Rijndael Algorithm)	
	Encryption Key Provisioning	
	Static (40-bit and 128-bit lengths)	
	Pre-Shared (PSK)	
	Dynamic	
	802.1X Extensible Authentication Protocol Types	
	EAP-FAST	PEAP-MSCHAPv2
	EAP-TLS	PEAP-TLS
	EAP-TTLS	LEAP
	PEAP-GTC	
Compliance	**EU Regulatory**	
	EN 300 328	62311:2008
	EN 301 489-1	EN 50665:2017
	EN 301 489-17	EN 50385:2017
	EN 301 893	EU 2015/863 (RoHS 3)
	FCC Regulatory	**ISED Canada**
	47 CFR FCC Part 15.247	ICES-003
	47 CFR FCC Part 15.407	ANSI C63.4:2014
	47 CFR FCC Part 2.1091	RSS-102
	FCC Part 15 Subpart B Class B	RSS-247
Certifications	**Wi-Fi Alliance** 802.11a, 802.11b, 802.11g , 802.11n WPA Enterprise WPA2 Enterprise	
Warranty	**Three Year Warranty**	

All specifications are subject to change without notice

5 WLAN Functional Description

5.1 Overview

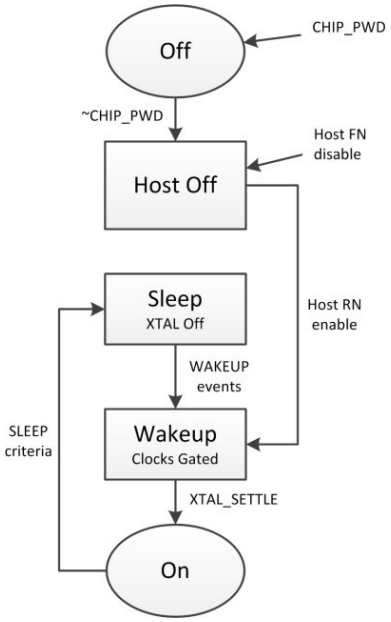
The SSD50NBT WLAN block is based on the Qualcomm-Atheros AR6004 802.11a/b/g/n chipset. It is optimized for low power embedded applications and is configured to operate in dual-band, two-stream (2x2 MIMO) mode. Its functionality includes:

- Improved throughput on the link due to frame aggregation, RIFS (reduced inter-frame spacing), and half guard intervals.
- Support for STBC (Space Time Block Codes) and LDPC (Low Density Parity Check) codes.
- Improved 11n performance due to features such as 11n frame aggregation (A-MPDU and A-MSDU) and low-overhead host-assisted buffering (RX A-MSDU and RX A-MPDU). These techniques can improve performance and efficiency of applications involving large bulk data transfers such as file transfers or high-resolution video streaming.

Other functionality are listed in the following table (Table 3).

Table 3: WLAN functions

Feature	Description
Reset Control	WLAN_PWD_L and BT_PWD_L pins must be asserted low to reset Wi-Fi and *Bluetooth*. After these signals are de-asserted, the radio waits for host communication. Until then, all modules except the host interface are held in reset. Once the host has initiated communication, the radio turns on its crystal and then the PLL. After all clocks are stable and running, the block resets are automatically de-asserted. **Note**: Because it derives its clock from WLAN, the *Bluetooth* function should be powered down/reset whenever WLAN is reset.
Reset Sequence	After a COLD_RESET event, the SSD50NBT enters the HOST_OFF state and awaits communication from the host. From that point, the typical COLD_RESET sequence is shown below: When the host is ready to use the radio, it initiates communication via the SDIO. The radio enters the WAKEUP state and then the ON state. Embedded software configures the radio functions and interfaces. When the radio is ready to receive commands from the host, it sets an internal function ready bit. The host reads the ready bit and sends function commands to the radio. The embedded CPU may continue to be held in reset under some circumstances until its reset is cleared by an external pin or when the host clears a register.

Feature	Description
Power Transition	Integrated power management and control functions and low power operation for maximum battery life across all operational states by: Gating clocks for logic when not needed Shutting down unneeded high speed clock sources Reducing voltage levels to specific blocks in some states See Figure 1.  ***Figure 1: Power state transition***
Hardware Power States	The SSD50NBT hardware has five top-level hardware power states managed by the RTC block.

State	Description
OFF	• CHIP_PWD_L pin assertion immediately brings the chip to the OFF state. • Sleep clock is disabled. • No state is preserved.
HOST_OFF	• WLAN is turned off. The *Bluetooth* clock is off but should also be powered down through BT_PWD_L. • Only the host interface is powered on. The rest of the chip is power gated (off). • The host instructs the SSD50NBT to transition to WAKEUP by writing a register in the host interface domain. • The embedded CPU and WLAN do not retain state (separate entry).
SLEEP	• Only the sleep clock is operating. • The crystal or oscillator is disabled. • Any wakeup events force a transition from this state to the WAKEUP state. • All internal states are maintained.
WAKEUP	• The system transitions from sleep states to ON. • The high frequency clock is gated off as the crystal or oscillator is brought up and the PLL is enabled. • WAKEUP duration is programmable.
ON	• The high speed clock is operational and sent to each block enabled by the clock control register.

Feature	Description
	• Lower level clock gating is implemented at the block level, including the CPU, which can be gated off using the WAITI instruction while the System is on. • No CPU, host, and WLAN activities transition to sleep states. WLAN must be initialized prior to *Bluetooth* initialization and use.
Sleep State Management	Sleep state minimizes power consumption while saving system states. In sleep state, all high speed clocks are gated off and the external reference clock source is powered off. The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, waits for the reference clock source to stabilize, and then un-gates all enabled clock trees. The embedded CPU wakes up only when an interrupt arrives, which may have also generated the system WAKEUP event.
System Clocking (RTC Block)	The SSD50NBT has an RTC block which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable and power signals which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The SSD50NBT's clocking is grouped into two types: high-speed and low-speed. **High Speed Clocking** The reference 26 MHz clock source inside the SSD50NBT drives the PLL and RF synthesizer of Wi-Fi and *Bluetooth*. To minimize power consumption, the reference clock source is powered off in SLEEP, HOST_OFF, and OFF states. **Low Speed Clocking** On Wi-Fi operation, the SSD50NBT does not need an external sleep clock source. Instead, an internal ring oscillator is used to generate a low frequency sleep clock. It is also used to run the state machines and counters related to low power states. The SSD50NBT has an internal calibration module which produces a 32.768 KHz output with minimal variation. For this, it uses the reference clock source as the golden clock. As a result, the calibration module adjusts for process and temperature variations in the ring oscillator when the system is in ON state. The *Bluetooth* section shares the clock from the Wi-Fi chip. It is not able to get into deep sleep mode without 32KHz present at pin-24. Without get into deep sleep mode, it consumes 3.3 mA at VDD_BT supply. In order to have the *Bluetooth* device get into deep sleep mode, a 32.768 KHz slow clock is a must on pin-24. When 32.768 KHz is present on pin-24, the *Bluetooth* chip can go into deep sleep mode with 0.08 mA current consume on VDD_BT supply. **Interface Clock** The host interface clock represents another clock domain for the SSD50NBT. This clock comes from the SDIO and is independent from the other internal clocks. It drives the host interface logic as well as certain registers which can be accessed by the host in HOST_OFF and SLEEP states.
MAC/BB/RF Block	The SSD50NBT Wireless MAC consists of five major blocks: • Host interface unit (HIU) for bridging to the AHB for bulk data accesses and APB for register accesses • Ten queue control units (QCU) for transferring Tx data • Ten DCF control units (DCU) for managing channel access • Protocol control unit (PCU) for interfacing to baseband • DMA receive unit (DRU) for transferring RxX data
Baseband Block	The SSD50NBT baseband module (BB) is the physical layer controller for the 802.11b/g/n air interface. It is responsible for modulating data packets in the transmit direction and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to dynamically adjust analog gains and modes.
Clock Sharing	Clock sharing is implemented on the SSD50NBT. The *Bluetooth* chip (CSR8811) receives a reference clock from the Wi-Fi chip (QCA6004). When Wi-Fi is in power off/reset state, *Bluetooth* is also off. 32.768KHz slow clock is needed for BT to get into deep sleep mode.

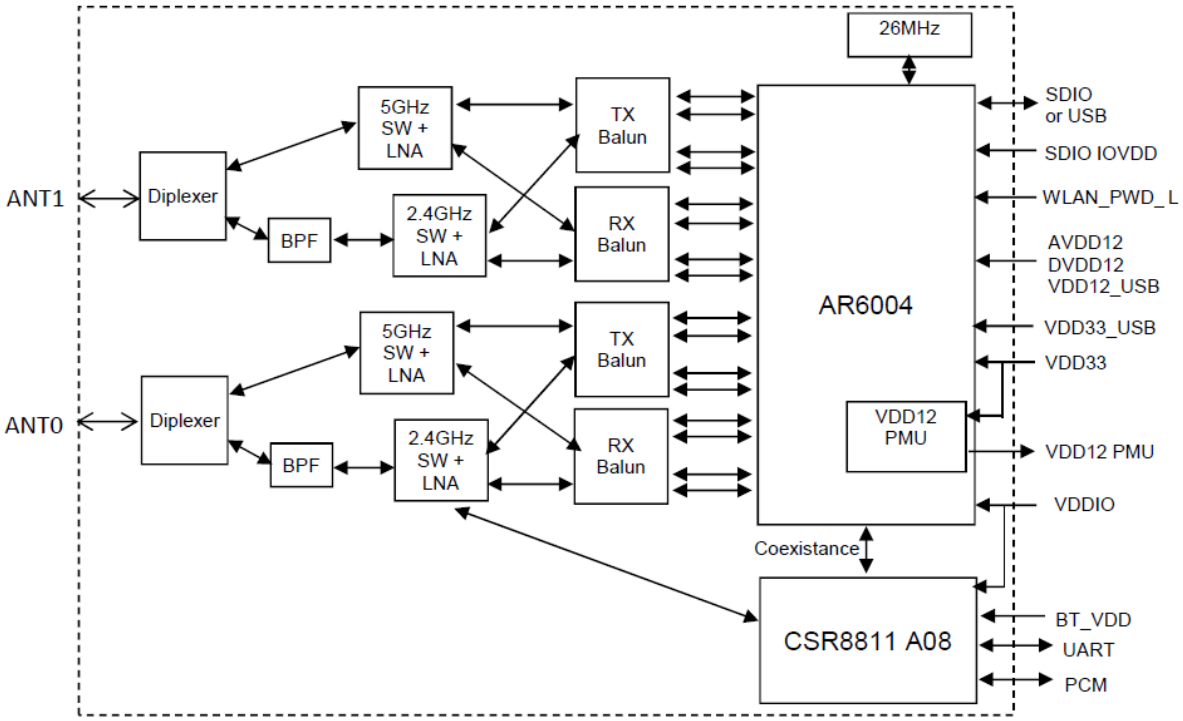
6 Bluetooth Functional Description

The SSD50NBT Bluetooth (BT) block is based on CSR8811A08 and described in the following table (Table 4).

Table 4: Bluetooth functions

Feature	Description
HCI-UART Interface	The UART Interface is a standard high-speed UART interface. It operates up to 4 Mbps, supporting *Bluetooth* HCI UART interface.
PCM or I2S Interface	• Continuous PCM encoded audio data transmission and reception over Bluetooth. • Processor overhead reduction through hardware support for continual transmission and reception of PCM data. • A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer. • Hardware on CSR8811 for sending data to and from a SCO connection. • Up to three SCO connections on the PCM interface at any one time. • PCM interface master, generating PCM_SYNC and PCM_CLK. • PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK. • Various clock formats including: – *Long Frame Sync – *Short Frame Sync • GCI timing environments • 13-bit or 16-bit linear, 8-bit µ-law or A-law companded sample formats. • Receives and transmits on any selection of three of the first four slots following PCM_SYNC. • The PCM configuration options are enabled by setting SKEY_PCM_CONFIG32.
CPU and Memory	The CSR8811 uses a 16-bit RISC MCU for low power consumption and efficient use of memory. The MCU, interrupt controller, and event timer run the *Bluetooth* software stack and control the *Bluetooth* radio and host interfaces. 56 KB of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the *Bluetooth* stack. 5 Mb of Internal ROM memory is available on the CSR8811. This memory is provided for system firmware, storing CSR8811 settings and program code.
Build-in Standard WLAN Coexistence	The SSD50NBT supports internally the standard WLAN coexistence interface through the WLAN_ACTIVE, BT_PRIORITY, and BT_ACTIVE pins.
Reference Clock	The BT block is configured for 26 MHz reference clock frequency. The clock source is provided to BT internally from the WLAN block on demand from BT_CLK_REQ. **Note:** The WLAN block must be initialized prior before BT clock sharing is enabled.
BT Low Energy	The SSD50NBT supports Low Energy specification which allows for connection to devices with single mode LE function (such as a watch, sensor, and HID). The implementation is optimized for coexistence with WLAN.
Reset	The pin BT_PWD_L resets and powers down the BT block. Holding the BT_PWD_L pin at GND turns off the entire BT block; all state information is lost. To ensure a full reset, the reset signal should be asserted for a period greater than 5 milliseconds.
Radio	The *Bluetooth* radio shares the single antenna port with the WLAN through an internal 3-way RF switch. The SSD50NBT implements WLAN/BT coexistence internally. VDDIO is to set the I/O voltage internally with either 1.8 V or 3.3 V to ensure same voltage level for the internal Wi-Fi and BT coexistence signal. Refer to the reference design specifications for details.
BT wake up Host	PIO-3 is reserved for BT to wake host from deep sleep mode.
SDIO_IOVDD	WLAN host IO (SDIO) power supply input 1.8V or 3.3V.

7 Block Diagram



Note: Refer to the Specifications table for the Wi-Fi transmitter frequencies.

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 5 summarizes the absolute maximum ratings and Table 6 lists the recommended operating conditions for the SSD50NBT. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 5: Absolute maximum ratings

Symbol (Domain)	Parameter	Max Rating	Unit
SDIO_IOVDD	WLAN host SDIO interface I/O supply	-0.3 to 4.0	V
VDDIO (Wi-Fi and BT)	WLAN and BT I/O configuration power supply	-0.3 to 4.0	V
VDD33; VDD33_FEM	External 3.3V power supply	-0.3 to 4.0	V
BT_VDD	BT Power core supply	3.6	V
VDD12_USB, DVDD12, AVDD12	WLAN 1.2V power supply	-0.3 to 1.32	V
Storage	Storage Temperature	-40 to +85	°C
ANT1; ANT2	Maximum RF input (reference to 50-Ω input)	+10	dBm
ESD	Electrostatic discharge tolerance	2000	V

8.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
SDIO_IOVDD	WLAN host interface I/O supply	1.71/3.2	1.8/3.3	1.89/3.46	V
VDDIO (Wi-Fi and BT)	WLAN and BT GPIO I/O power supply	1.71/3.2	1.8/3.3	1.89/3.46	V
VDD33	External 3.3V power supply	3.2	3.30	3.46	V
BT_VDD	BT core supply	3.2	3.30	3.46	V
VDD12_USB, DVDD12, AVDD12	WLAN 1.2V power supply	1.20	1.26	1.32	V
T-ambient	Ambient temperature	-30	25	85	°C

8.3 DC Electrical Characteristics

Table 7 and Table 8 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 7: General DC electrical characteristics (For 3.3V I/O operation)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
VIH	High Level Input Voltage			0.7 x VDD			V
VIL	Low Level Input Voltage					0.3 x VDD	V
IIL	Input Leakage Current	Without Pull-up or Pull-down	0V < VIN < VDD 0V < VOUT< VDD	0		-3	nA
		With Pull-up	0 V < VIN < VDD 0V < VOUT < VDD	16		48	µA
		With Pull-down	0V < VIN < VDD 0V < VOUT < VDD	-14		-47	µA
VOH	High Level Output Voltage		IOH = -4mA	0.9 x VDD			V
			IOH = -12mA	0.9 x VDD			V
VOL	Low Level Output Voltage		IOH = 4mA			0.1 x VDD	V
			IOH = 12mA			0.1 x VDD	V

Table 8: General DC electrical characteristics (For 1.8V I/O operation)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
VIH	High Level Input Voltage			0.7 x VDD			V
VIL	Low Level Input Voltage					0.3 x VDD	V
IIL	Input Leakage Current	Without Pull-up or Pull-down	0V < VIN < VDD 0V < VOUT < VDD	0		-3	nA
		With Pull-up	0V < VIN < VDD 0V < VOUT < VDD	3.5		13	µA
		With Pull-down	0V < VIN < VDD 0V < VOUT < VDD	-6.2		-23	µA
VOH	High Level Output Voltage		IOH = -4mA	0.9 x VDD			V
			IOH = -12mA	0.9 x VDD			V
VOL	Low Level Output Voltage		IOH = 4mA			0.1 x VDD	V
			IOH = 12mA			0.1 x VDD	V

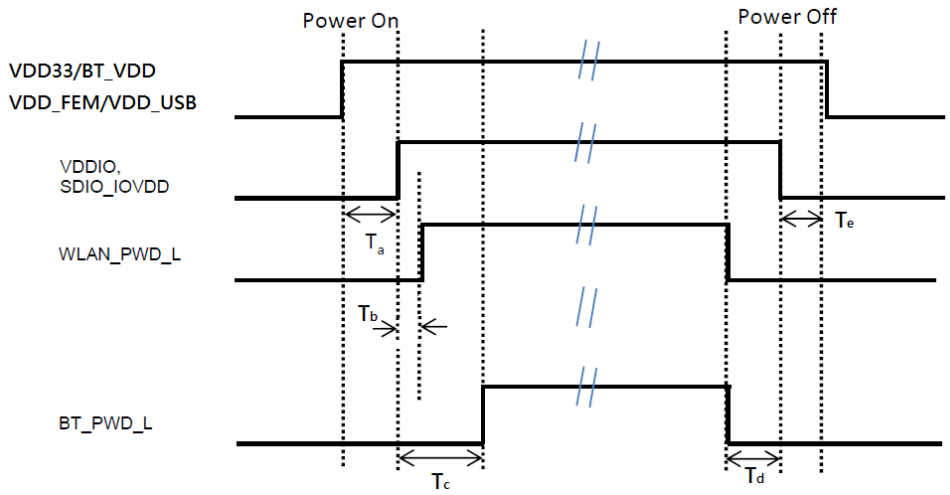


Figure 2: Power On/Off timing

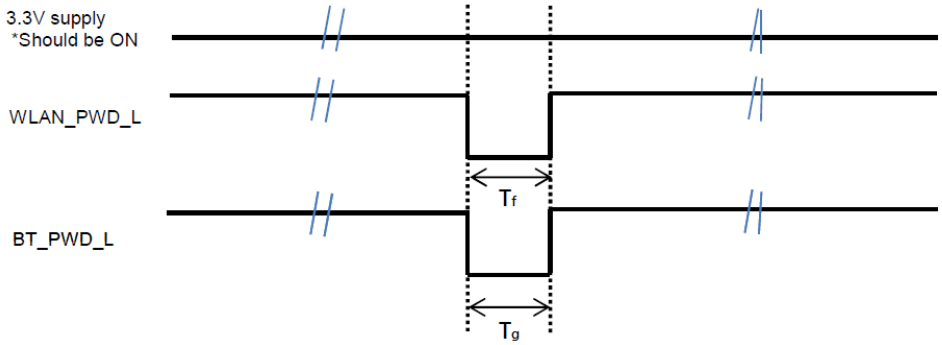


Figure 3: Wi-Fi and BT reset timing

Table 9: Timing Diagram Definitions

Timing	Description	Min	Unit
Ta	Time between 3.3V (VDD33/BT_VDD/VDD_FEM/VDD_USB) and VDDIO/SDIO_IOVDD supplies	0	µsec
Tb	Time between VDDIO/SDIO_IOVDD supplies valid and WLAN_PWD_L negation. **Note:** There are 10K ohm internal Pull-up on SD_D0, SD_D1 and SD_D3.	5	µsec
Tc	Time between VDDIO/SDIO_IOVDD supplies valid and BT_PWD_L negation	5	msec
Td	Time between WLAN_PWD_L assertion and VDDIO/SDIO_IOVDD invalid or time between BT_PWD_L negation and VDDIO/SDIO_IOVDD invalid.	0	µsec
Te	Time between VDDIO/SDIO_IOVDD invalid and 3.3V (VDD33/BT_VDD/VDD_FEM/VDD_USB) invalid.	No requirement	
Tf	Time of WLAN_PWD_L assertion during reset or power down period. Both 3.3V (VDD33/BT_VDD/VDD_FEM/VDD_USB) and VDDIO/SDIO_IOVDD should keep ON.	5	µsec
Tg	Time of BT_PWD_L assertion during reset or power down period. Both 3.3V (VDD33/BT_VDD/VDD_FEM/VDD_USB) and VDDIO/SDIO_IOVDD should keep ON.	5	msec

Important: **The SSD50NBT requires SDIO interface lines SD_CMD, SD_D1, and SD_D2 to be high prior to negation of WLAN_PWD_L. Designs should drive these lines high or, if necessary, add external pull-ups to insure proper SDIO configuration on WLAN boot-up. Failure to pull these lines high results in non-functional SDIO interface. These are boot-mode strapping options interpreted by the WLAN CPU on power-on. There is 10K ohm pull high resistor already implemented on SD_D0, SD_D1, and SD_D3. No external pull-up is required for those three lines.**

We suggest that Tb and Tf timing is greater than 5µsec but no longer than 100 msec.

8.4 WLAN Radio Receiver Characteristics

Table 10 and Table 11 summarize the WLAN SSD50NBT receiver characteristics.

Table 10: WLAN receiver characteristics for 2.4 GHz signal chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Frx	Receive input frequency range		2.412		2.484	GHz
Srf	Sensitivity					
	CCK, 1 Mbps	See Note[3]		-95		dBm
	CCK, 11 Mbps			-88		
	OFDM, 6 Mbps			-92		
	OFDM, 54 Mbps			-75		
	HT20, MCS0			-92		
	HT20, MCS7			-72		
Radj	Adjacent channel rejection					
	OFDM, 6 Mbps	See Note[4]		32		dB
	OFDM, 54 Mbps			16		
	HT20, MCS0			31		
	HT20, MCS7			14		

[3]Performance data are measured under signal chain operation.

[4]Performance data are measured under signal chain operation.

Table 11: WLAN Receiver Characteristics for 5 GHz Dual Chain Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Frx	Receive input frequency range		5.15		5.825	GHz
Srf	Sensitivity					
	OFDM, 6 Mbps	See Note[5]		-93		dBm
	OFDM, 54 Mbps			-75		
	HT20, MCS0			-93		
	HT20, MCS7			-72		
	HT40, MCS0			-87		
	HT40, MCS7			-67		
Radj	Adjacent channel rejection					
	OFDM, 6 Mbps	See Note[6]		22		dB
	OFDM, 54 Mbps			9		
	HT20, MCS0			20		
	HT20, MCS7			19		

[5]Performance data are measured under dual chain operation.

[6]Performance data are measured under dual chain operation.

8.5 WLAN Transmitter Characteristics

Table 12: WLAN transmitter characteristics for 2.4 GHz per chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ftx	Transmit output frequency range		2.412		2.484	GHz
Pout	Output power	See Note[7]				
	11b mask compliant	1Mbps		18		dBm
	11g mask compliant	6Mbps		18		
	11g EVM compliant	54Mbps		15		
	11n HT20 mask compliant	MCS0		18		
	11n HT20 EVM compliant	MCS7		14		
	11n HT20 EVM compliant	MCS15		14		
ATx	Transmit power accuracy at 18 dBm	-	-	+ 2.0		dB

Freq.	Mode/Rate (Mbps)	Output Power Per Chain (dBm)	Typical Current Consumption Single Chain (mA)[8]	Max. Current Consumption Single Chain (mA)[8]
2412MHz	1 Mbps	18dBm	420	560
	54 Mbps	15dBm	350	450
	HT20 MCS7	14dBm	340	420
2442MHz	1 Mbps	18dBm	420	560
	54 Mbps	15dBm	350	450
	HT20 MCS7	14dBm	340	420
2472MHz	1 Mbps	18dBm	420	560
	54 Mbps	15dBm	350	450
	HT20 MCS7	14dBm	340	420

Table 13: WLAN transmitter characteristics for 5 GHz per chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ftx	Transmit output frequency range		5.15		5.925	GHz
Pout	Output power	See Note[3]				
	11a mask compliant	6Mbps		18		dBm
	11a EVM compliant	54Mbps		15		
	11n HT20 mask compliant	MCS0		18		
	11n HT20 EVM compliant	MCS7		14		
	11n HT20 EVM compliant	MCS15		14		
	11n HT40 mask compliant	MCS0		15		
	11n HT40 EVM compliant	MCS7		12		
	11n HT40 EVM compliant	MCS15		12		
ATx	Transmit power accuracy at 18 dBm	-	-	+ 2.0		dB

Freq.	Mode/Rate [Mbps]	Output Power Per Chain [dBm]	Typical Current Consumption Single Chain (mA)[8]	Max. Current Consumption Single Chain (mA)[8]
5180MHz	54 Mbps	15 dBm	490	590
	HT20 MCS7	14 dBm	450	560
	HT40 MCS7	12 dBm	470	540
5500MHz	54 Mbps	15 dBm	490	590
	HT20 MCS7	14 dBm	450	560
	HT40 MCS7	12 dBm	470	540
5825MHz	54 Mbps	15 dBm	490	590
	HT20 MCS7	14 dBm	450	560
	HT40 MCS7	12 dBm	470	540

[7]Performance data are measured under single chain operation.

Note: Final TX power values on each channels are limited by the regulatory certification test limit.

Note: 2.4 GHz does not support HT40 operation, only 5 GHz support HT40 operation.

9 Bluetooth Radio Characteristics

Table 14 through Table 15 describe the basic rate transmitter performance, enhanced data transmitter performance, basic rate receiver performance, enhanced rate receiver performance, and current consumption conditions at 25°C.

Table 14: Basic rate transmitter performance temperature at 25°C (3.3V)

Test Parameter	Min	Typ	Max	BT Spec.	Unit
Maximum RF Output Power	2	6	—	−6 to +10	dBm
Frequency Range	2.4	—	2.4835	2.4 ≤ f ≤ 2.4835	GHz
20 dB Bandwidth	—	925	—	≤ 1000	KHz
Adjacent Channel TX Power F = F0 + 2 MHz	—	−36	—	≤ −20	dBm
Adjacent Channel TX Power F = F0 +3 MHz	—	−42	—	≤ −40	dBm
Δf1avg Maximum Modulation	140	165	175	140 < Δf1avg < 175	KHz
Δf2max Minimum Modulation	—	135	—	≥ 115	KHz
Δf2avg/Δf1avg	—	0.9	—	≥ 0.80	—

Test Parameter	Min	Typ	Max	BT Spec.	Unit
Initial Carrier Frequency	—	5	—	≤±75	KHz
Drift Rate	—	5	—	≤ 20	KHz/50 µs
Drift (DH1 packet)	—	6	—	≤25	KHz
Drift (DH5 packet)	—	7	—	≤ 40	KHz

Table 15: Enhanced data rate transmitter performance 25°C (3.3V)

Test Parameter		Min	Typ	Max	BT Spec.	Unit
Relative Transmit Power		-1	3	6	-4 to +1	dBm
Max Carrier Frequency Stability Iwol	π/4 DQPSK	—	1	—	≤ ±10	KHz
	8 DPSK	—	1	—		
Max Carrier Frequency Stability Iwil	π/4 DQPSK	—	1	—	≤ ±75	KHz
	8 DPSK	—	1	—		
Max Carrier Frequency Stability Iw0+wil	π/4 DQPSK	—	2	—	≤ ±75	KHz
	8 DPSK	—	1.5	—		
RMS DEVM	π/4 DQPSK	—	6	—	≤ 20	%
	8 DPSK	—	6	—	≤13	%
Peak DEVM	π/4 DQPSK	—	16	—	≤ 35	%
	8 DPSK	—	15	—	≤ 25	%
99% DEVM	π/4 DQPSK	—	12	—	≤ 30	%
	8 DPSK	—	12	—	≤ 20	%
EDR Differential Phase Encoding		—	99	—	≥ 99	%
Adjacent Channel Power	F≥ ± 3MHz	—	-60	—	‹ -40	dBm
	F = ± 2MHz	—	-28	—	≤ -20	dBm
	F = ±1MHz	—	-32	—	≤ -26	dB

Table 16: Basic rate receiver performance at 3.3V

Test Parameter		Min	Typ	Max	BT Spec.	Unit
Sensitivity	BER ≤ 0.1%	—	-84	-78	≤ -70	dBm
Maximum Input	BER ≤ 0.1%	-20	-10	—	≥ -20	dBm
Carrier-to-Interferer Ratio (C/I)	Co-Channel	—	—	11	11	
	Adjacent Channel (± 1 MHz)	—	-4/-2	0	0	dB
	Second Adjacent Channel (± 2 MHz)	—	-35/-28	-30	-30	dB
	Third Adjacent Channel (± 3 MHz)	—	-42	-40	-40	dB
Maximum Level of Intermodulation Interferers		-39	-30	-	≥ -39	dBm

Table 17: Enhanced data rate receiver performance 3.3V

Test Parameter		Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity (BER ≤0.01%)	8 DPSK	—	-76	-71	≤ -70	dBm
Maximum Input (BER ≤0.1%)	π/4 DQPSK	-20	—	—	≥ -20	dBm
	8 DPSK	-20	—	—	≥ -20	dBm
Co-Channel C/I (BER ≤0.1%)	π/4 DQPSK	—	10	13	≤ ±13	dB
	8 DPSK	—	18	20	≤ ±20	dB
Adjacent Channel C/I (BER≤ 0.1%)	π/4 DQPSK	—	-9/-6	0	≤ 0	dB
	8 DPSK	—	-3/0	5	≤5	dB
Second Adjacent Channel C/I (BER ≤ 0.1%)	π/4 DQPSK	—	-42/-28	-30	≤ -30	dB
	8 DPSK	—	-28/-22	-25	≤ -25	dB
Third Adjacent Channel C/I (BER ≤ 0.1%)	π/4 DQPSK	—	-45	-40	≤ -40	dB
	8 DPSK	—	-39	-33	≤ -33	dB

10 SDIO Timing Requirements

The following figure (Figure 4) and table (Table 18) display SDIO default mode timing.

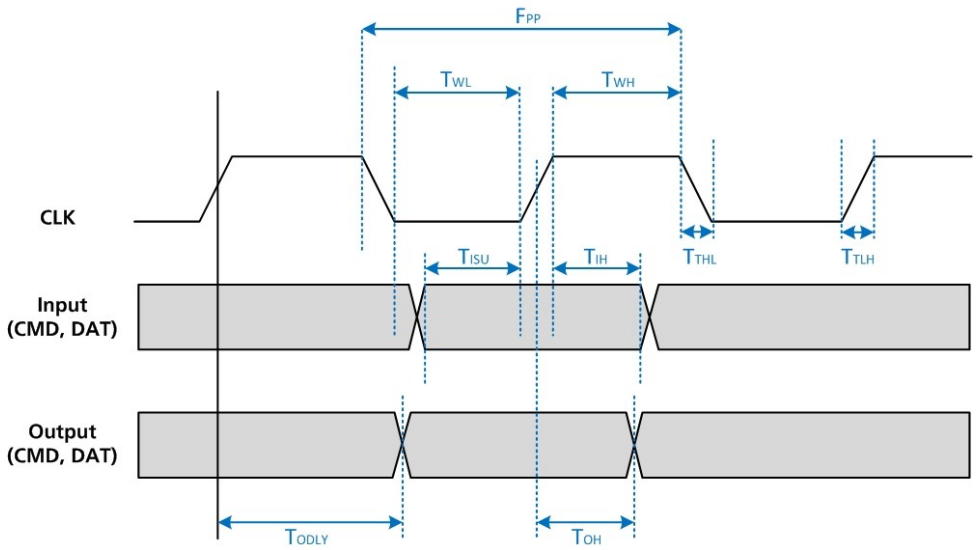


Figure 4: SDIO default mode timing

Note: Timing is based on CL ≤ 40 pF load on CMD and Data.

Table 18: SDIO timing requirements

Symbol	Parameter	Min.	Typ.	Max.	Unit
fPP	Frequency – Data Transfer mode	0	-	50	MHz
tWL	Clock low time	7	-	-	ns
tWH	Clock high time	7	-	-	ns
tTLH	Clock rise time	-	-	10	ns
tTHL	Clock low time	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					

Symbol	Parameter	Min.	Typ.	Max.	Unit
tISU	Input setup time	6	-	-	ns
tIH	Input hold time	2	-	-	ns
	Outputs: CMD, DAT (referenced to CLK)				
tODLY	Output delay time – Data Transfer mode	0	-	14	ns

11 Pin Definitions

Pin #	Name	Type	Voltage Reference	Description	If Not Used
1	GND	-	-	Ground	GND
2	GND	-	-	Ground	GND
3	WIFI_RFKILL (GPIO-10)	I, PU	SDIO_IOVDD	Reserved for RF disable (RF Kill) feature. Active Low. **Note:** The current does not support it. # See Boot strap configuration.	N/C
4	XPABIAS51	O	VDDIO	Control signal for external 5GHz power amplifier Chain 1.	N/C
5	GND	-	-	Ground	GND
6	VDD33_FEM	Power	-	3.3V Power for FEM	3.3V
7	VDD33_FEM	Power	-	3.3V Power for FEM	3.3V
8	GND	-	-	Ground	GND
9	GND	-	-	Ground	GND
10	GND	-	-	Ground	GND
11	ANT_1 (Wi-Fi)	A_IO	-	WLAN antenna port (Chain 1)	50 Ωload
12	GND	-	-	Ground	GND
13	XPABIAS20	O	VDDIO	Control signal for external 2GHz power amplifier Chain 0.	N/C
14	BT_PCM_SYNC	I/O, PD	VDDIO	PCM interface synchronization control, input for slave, output for master, weak internal pull-down. High on reset, low after reset.	N/C
15	BT_PCM_BCLK	I/O, PD	VDDIO	PCM interface bit clock, input for slave, output for master, weak internal pull-down. High on reset, low after reset.	N/C
16	BT_PCM_IN	I, PD	VDDIO	PCM synchronous input, weak internal pull-down.	N/C
17	BT_PCM_OUT	O, PD	VDDIO	PCM synchronous output, weak internal pull-down.	N/C
18	XPABIAS50	O	VDDIO	Control signal for external 5GHz power amplifier Chain 1.	N/C
19	GND	-	-	Ground	GND
20	ANT_0 (Wi-Fi and BT)	A_IO	-	WLAN/BT antenna port (Chain 0)	50 Ωload
21	GND	-	-	Ground	GND
22	BT_PWD_L	I, PD	VDDIO	BT chip power-down control. Driving this pin active low to power down or to reset the BT chip. Has internal strong pull-down. **Note:** Should be low for at least 5 ms for chip reset.	10K PU

Pin #	Name	Type	Voltage Reference	Description	If Not Used
23	NC	-	-		N/C
24	CLK_32K	I	VDDIO	External 32.768KHz input for BT chip. It is must for BT chip to get deep sleep mode.	Must be used
25	BT_VDD	Power	-	BT core power supply input 3.3V	3.3V
26	GND	-	-	Ground	GND
27	BT_UART_RXD	I, PU	VDDIO	Bluetooth UART Serial Input	N/C
28	BT_UART_TXD	O, PU	VDDIO	Bluetooth UART Serial Output	N/C
29	BT_UART_CTS	I, PU	VDDIO	Clear-to-send signal for the Bluetooth UART interface, active low.	N/C
30	BT_UART_RTS	O, PU	VDDIO	Request-to-send signal for the Bluetooth UART interface, active low.	N/C
31	BT_WAKEUP_HOST	O	VDDIO	When BT wakes up from its deep sleep state, it sends an H pulse signal out to Host. Normally, it is Low state. **Note:** The current software does not support it.	N/C
32	GND	-	-	Ground	GND
33	VDDIO	Power	-	1.8 or 3.3V I/O power configuration. This is the reference voltage for all I/O signalling pins; it accepts 1.8V or 3.3V from the host.	1.8V or 3.3V
34	GND	-	-	Ground	GND
35	SDIO_CLK	I	VDDIO	SDIO Clock	N/C
36	GND	-	-	Ground	GND
37	SDIO_DATA_0	I/O	SDIO_IOVDD	SDIO Data 0, internal 10K pulled-up.	N/C
38	SDIO_DATA_1	I/O	SDIO_IOVDD	SDIO Data 1, internal 10K pulled-up.	N/C
39	SDIO_DATA_2	I/O	SDIO_IOVDD	SDIO Data 2. **# See Boot strap configuration.**	
40	SDIO_DATA_3	I/O	SDIO_IOVDD	SDIO Data 3, internal 10K pulled-up.	N/C
41	SD_CMD	I/O	SDIO_IOVDD	SDIO Command signal, **# See Boot strap configuration.**	
42	SDIO_IOVDD	Power	-	WLAN Host bust SDIO I/O power configuration either 1.8V or 3.3V	1.8V or 3.3V
43	AVDD_12	Power	-	WLAN internal analogy 1.2V input fed from switching regulator or external 1.2V DC supply	1.2V
44	DVDD_12	Power	-	WLAN internal analogy 1.2V input fed from switching regulator or external 1.2V DC supply	1.2V
45	VDD12_USB	Power	-	USB interface 1.2V input fed from switching regulator or external 1.2V DC supply. **Note:** When Wi-Fi run at USB interface, external 1.2V (400mA max) is required.	1.2V
46	VDD33_USB	Power	-	USB interface 3.3V input. Connect to 3.3V	3.3V
47	VDD12_PMU	Power output	-	On-Chip 1.2V switching regulator output.	10uF

Pin #	Name	Type	Voltage Reference	Description	If Not Used
				A 10uF 6.3V LOW ESR cap is must to connect to this pin as close as possible.	
48	Reserved	I/O	-	Reserved pin. Please leave open.	N/C
49	Reserved	I/O	-	Reserved pin. Please leave open.	N/C
50	GND	-	-	Ground	GND
51	WLAN_PWD_L	I, PD	SDIO_IOVDD	WLAN Power down, active low, external 10K pull up is required. (0= power down, 1=WLAN awake) Negation samples boot strap pin for SDIO interface mode	10K, PU
52	WLAN_TDO	-	SDIO_IOVDD	Pull High for SDIO **# See Boot strap configuration.**	
53	AR6004_GPIO38	I/O	VDDIO	Reserved for LTE coexistence; Reserved for WiFi LED indicator, Active High. (Not support Now)	N/C
54	LTE_COEX3	-	VDDIO	Reserved for LTE coexistence	N/C
55	LTE_ACTIVE	-	VDDIO -	Reserved for LTE coexistence	N/C
56	LTE_FRAME_SYNC	-	VDDIO -	Reserved for LTE coexistence	N/C
57	VDD33	Power	-	3.3V Power	3.3V
58	VDD33	Power	-	3.3V Power	3.3V
59	GND	-	-	Ground	GND
60	WAKE_ON_WLAN	O, PD	SDIO_IOVDD	Reserved for Wake-ON-Wireless (WOW) LAN, WLAN output signal to wake up host, active Low and need external 10K pull up. **Note:** The current software does not support it.	10K,PU
61	DEBUG_UART_TXD	O	SDIO_IOVDD	WLAN debugging UART TXD (GPIO_11) **# See Boot strap configuration.**	N/C
62	WCN_PRIORITY	-	-	Reserved for LTE coexistence	N/C
63	GND	-	-	Ground	GND
64	XPABIAS21	O	VDDIO	Control signal for external 2GHz power amplifier Chain 1.	N/C
65-80	GND	-	-	Thermal Ground Pad **(Important for RF performance and thermal dissipation; please flow the reference design)**	GND

11.1 Integration Considerations

The following Wi-Fi information should be taken into consideration when integrating the SSD50NBT:

- When WLAN is communicating via the **SDIO** bus, the internal switch regulator (1.2V out) can be used to power the SSD50NBT itself. **Pin-47** (VDD12_PMU) of the SSD50NBT is the internal PMU output pin that generates 1.2V to provide to AVDD12 (**pin-43**), DVDD12 (**pin-44**), and AVDD12_USB (**pin-45**).
- When WLAN is communicating via the **USB** bus, an external 1.2 V (maximum rating 400 mA) is needed for to AVDD12 (**pin-43**), DVDD12 (**pin-44**), and AVDD12_USB (**pin-45**). This is due to insufficient power from internal PMU.
- No matter if WLAN is running at SDIO or USB bus, a 10uF, 6.3V low ESR capacitor is always needed directly on **pin-47** (VDD12_PMU) as close as possible to the pin.

12 Boot Strap Options for Wi-Fi Interface

SSD50NBT provides SDIO interface for WLAN connection. It is configured per the following table (Table 19).

Table 19: Wi-Fi interface configuration table

Pin No.	Pin Name	SDIO 2.0	Note
41	SD_CMD	H	-
39	SDIO_DATA_2	H	-
38	SDIO_DATA_1	H	10KΩ Pull High to Avoid Booting into test mode. **Note:** It is implemented inside the SSD50NBT. No external pull "H" is needed.
3	GPIO_10	L	10K Ω Pull "L" to Avoid leakage.
61	DEBUG_UART_TXD	N/C	No connection at SDIO bus.
52	WLAN_TDO	H	10K Ω Pull "H" to Avoid leakage. Only SDIO

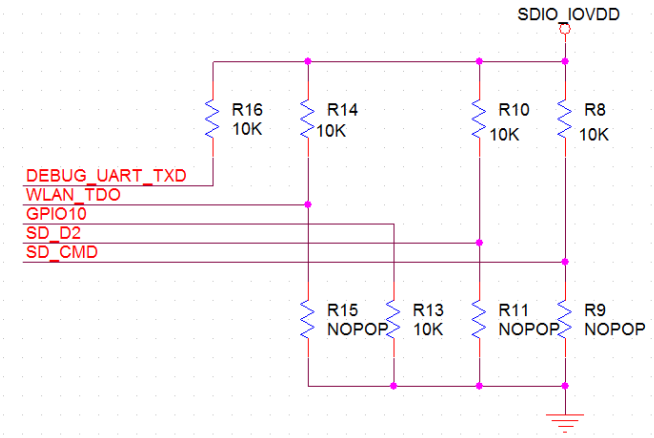


Figure 5: Setting when using SDIO interface

13 Mechanical Specifications

Module dimensions of SSD50NBT are 15 x 15 x 2.5 mm. Detail drawings are shown in Figure 6.

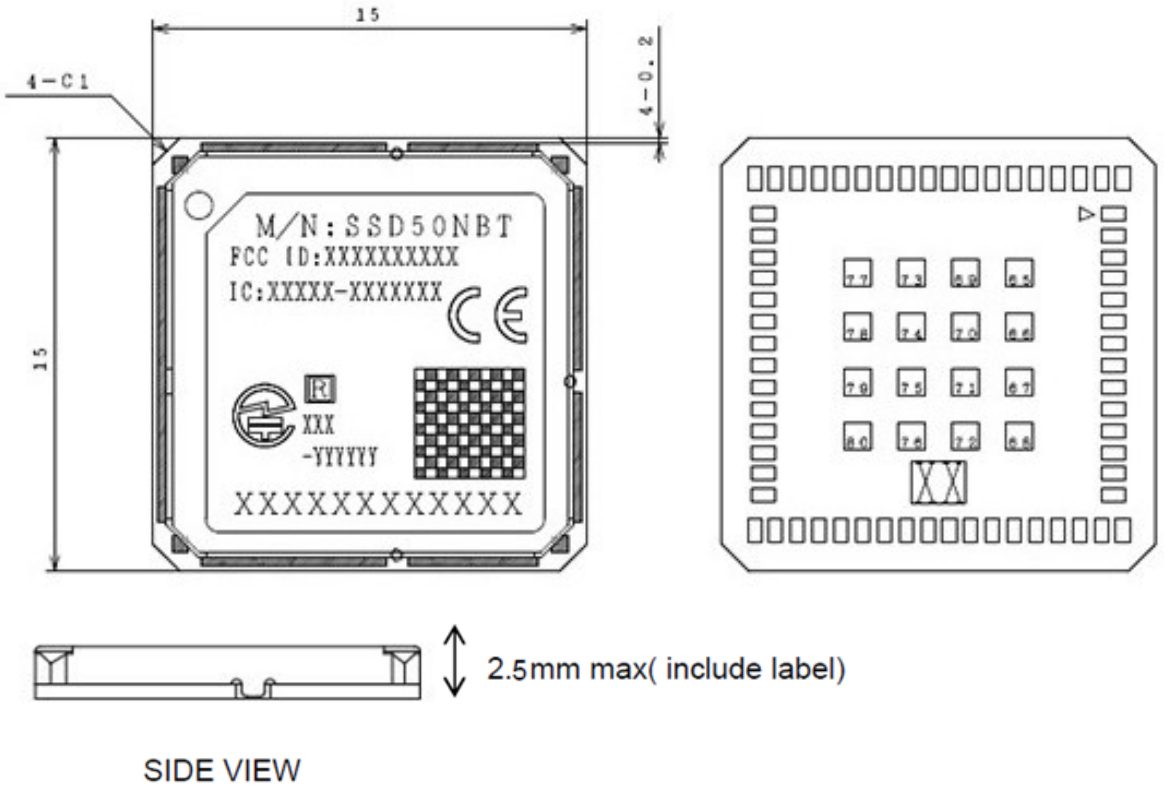


Figure 6: Module dimension of SSD50NBT

Note: The Wi-Fi MAC address is located on the product label. The BT MAC address is always numerically subsequent to the Wi-Fi MAC address. Therefore, the BT MAC address is the Wi-Fi MAC address plus one.

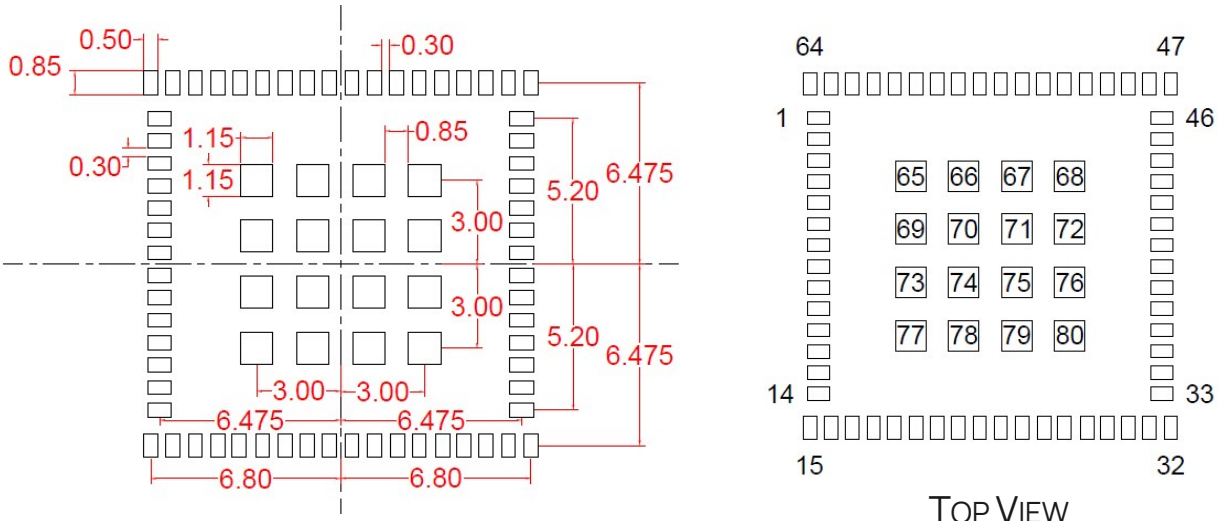
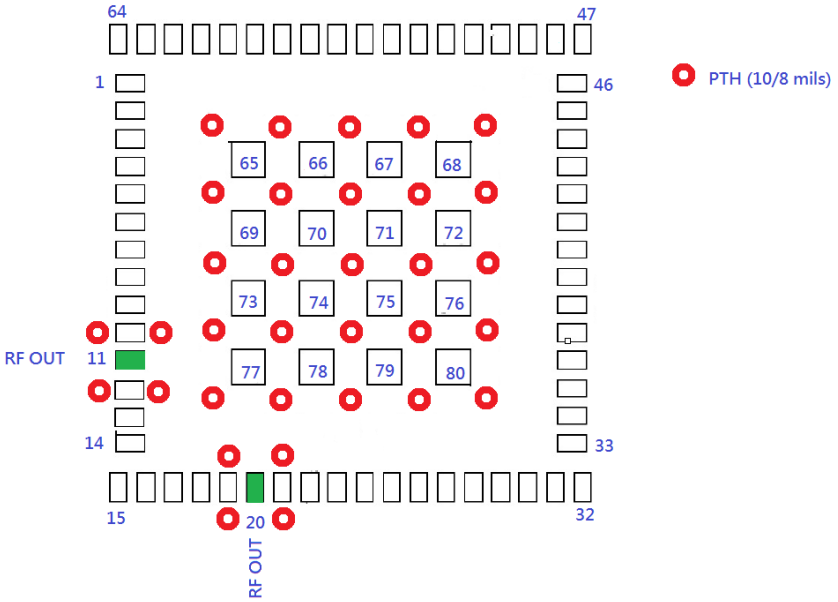


Figure 7: Pad dimensions and pin numbers



Recommend minimal via size and placement for grounding and thermal dissipation. Please double the ground via number when using laser via on HID process. More ground via and the use of 1-oz copper is recommended in our design to get better thermal dissipation.

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

14 RF Layout Design Guidelines

The following is a list of RF layout design guidelines and recommendation when installing a Ezurio radio into your device.

- Do not run antenna cables directly above or directly below the radio.
- Do not place any parts or run any high speed digital lines below the radio.
- If there are other radios or transmitters located on the device (such as a *Bluetooth* radio), place the devices as far apart from each other as possible. Also, make sure there is at least 25 dB isolation between the Bluetooth antenna and the Wi-Fi antenna.
- Ensure that there is the maximum allowable spacing separating the antenna connectors on the Ezurio radio from the antenna. In addition, do not place antennas directly above or directly below the radio.
- Ezurio recommends the use of a double-shielded cable for the connection between the radio and the antenna elements.
- Be sure to put the capacitor on the power pin as close as possible to reduce the radiation issue.
- Use proper electro-static-discharge (ESD) procedures when installing the Ezurio radio module.
- In order to get maximum throughput when operate at MIMO 2x2, two antennas with at least 25 dB isolation is recommended.
- To avoid negatively impacting Tx power and receiver sensitivity, do not cover the antennas with metallic objects or components.

15 Recommended Storage, Handling, Baking, and Reflow Profile

15.1 Required Storage Conditions

15.1.1 Prior to Opening the Dry Packing

The following are required storage conditions ***prior* to opening the dry packing**:

- Normal temperature: 5~40℃
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means Relative Humidity.

15.1.2 After Opening the Dry Packing

The following are required storage conditions ***after* opening the dry packing** (to prevent moisture absorption):

- Storage conditions for one-time soldering:
  - Temperature: 5~25℃
  - Humidity: 60% or less
  - Period: 48 hours or less after opening
- Storage conditions for two-time soldering

  Storage conditions following opening and prior to performing the 1st reflow:

  - Temperature: 5~25℃
  - Humidity: 60% or less
  - Period: 48 hours or less after opening

  Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow

  - Temperature: 5~25℃
  - Humidity: 60% or less
  - Period: 48 hours or less after completion of the 1st reflow

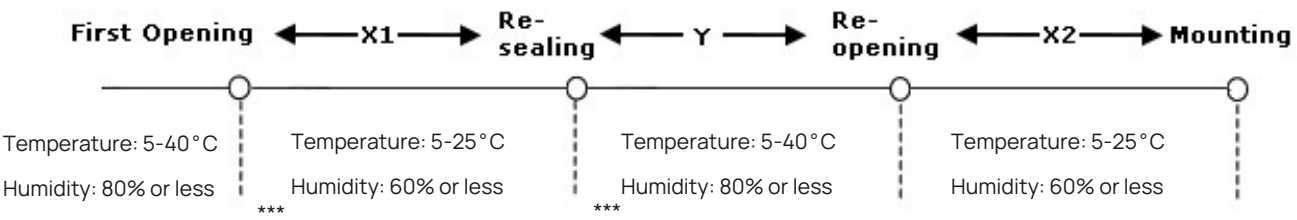
15.1.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices *once* prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

Storage temperature and humidity



*** - External atmosphere temperature and humidity of the dry packing

Storage period

- X1+X2 – Refer to After Opening the Dry Packing storage requirements.
- Y – Two weeks or less.

15.2 Baking Conditions

Baking conditions and processes for the SSD50NBT follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
- Once the packaging is opened, the SiP must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <30 ˚C and <60% relative humidity.
- If the SiP is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125 ˚C (±5 ˚C).

15.3 Surface Mount Conditions

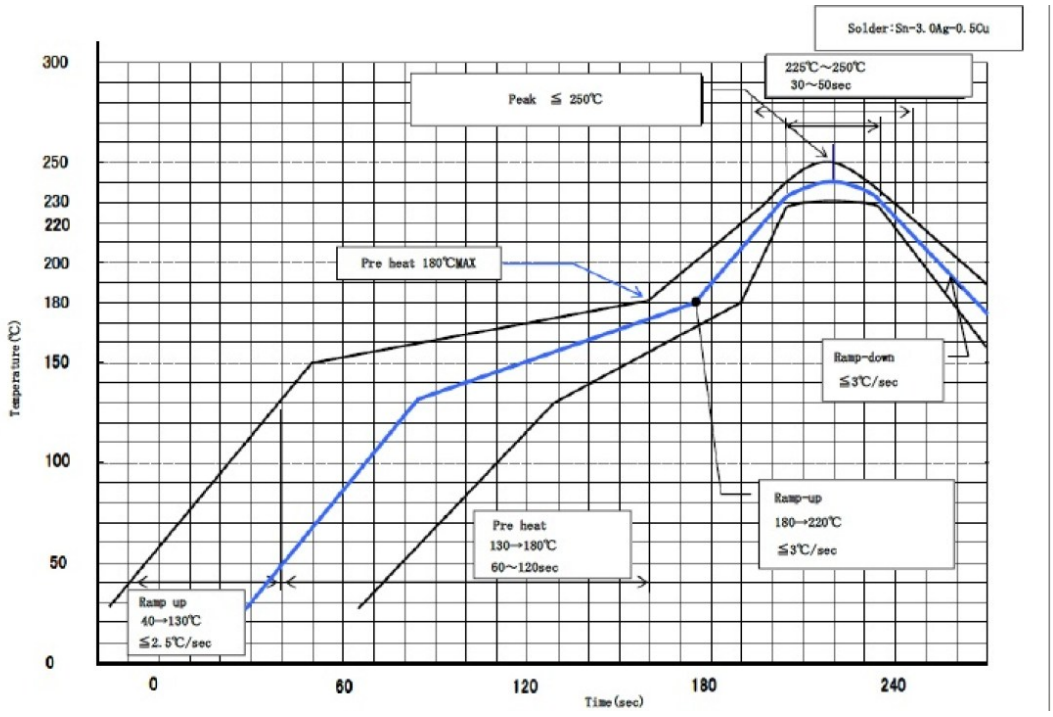
The following soldering conditions are recommended to ensure device quality.

15.3.1 Soldering

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point – IC package surface
- Temperature profile:



Ramp-up : 40 - 130 deg. Less than 2.5 deg./sec

Pre heat : 130 - 180 deg. 60 - 120 sec , 180 deg. MAX

Ramp-up : 180 - 220 deg. Less than 3 deg./sec

Peak Temperature : MAX 250 deg.

225 deg. ~ 250 deg. , 30 ~ 50 sec

Ramp-down : Less than 3 deg./sec

Figure 8: Temperature profile

15.3.2 Cautions When Removing the SIP from the Platform for RMA

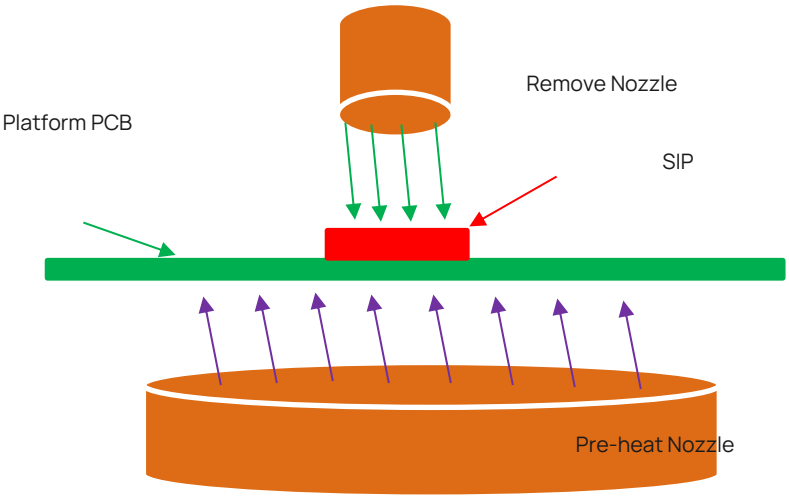
- Bake the platform before removing the SIP from the platform. Reference baking conditions.
- Remove the SIP by using a hot air gun. This process should be carried out by a skilled technician.

Suggestion conditions:

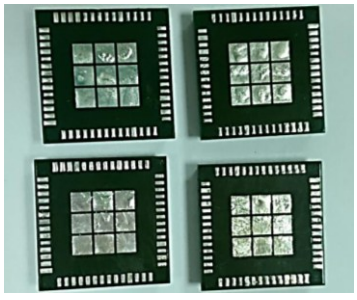
- One-side component platform:
  - Set the hot plate at 280 °C.
  - Put the platform on the hot plate for 8~10 seconds.
  - Remove the SIP from platform.

Two-side components platform:

- Use two hot air guns
- On the bottom side, use a pre-heated nozzle (temperature setting of 200~250 °C) at a suitable distance from the platform PCB.
- On the top side, apply a remove nozzle (temperature setting of 330 °C). Heat the SIP until it can be removed from platform PCB.

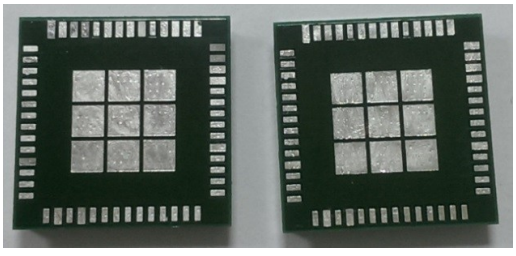


Remove the residue solder under the bottom side of SIP.



(Not accepted for RMA)

SIP with residue solder on the bottom



(Accepted for RMA analysis)

SIP without residue solder on the bottom

Remove and clean the residue flux if needed.

15.3.3 Precautions for Use

- Opening/handing/removing must be done on an anti-ESD treated workbench.
  All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.

16 Packaging Information

16.1 Inner Carton

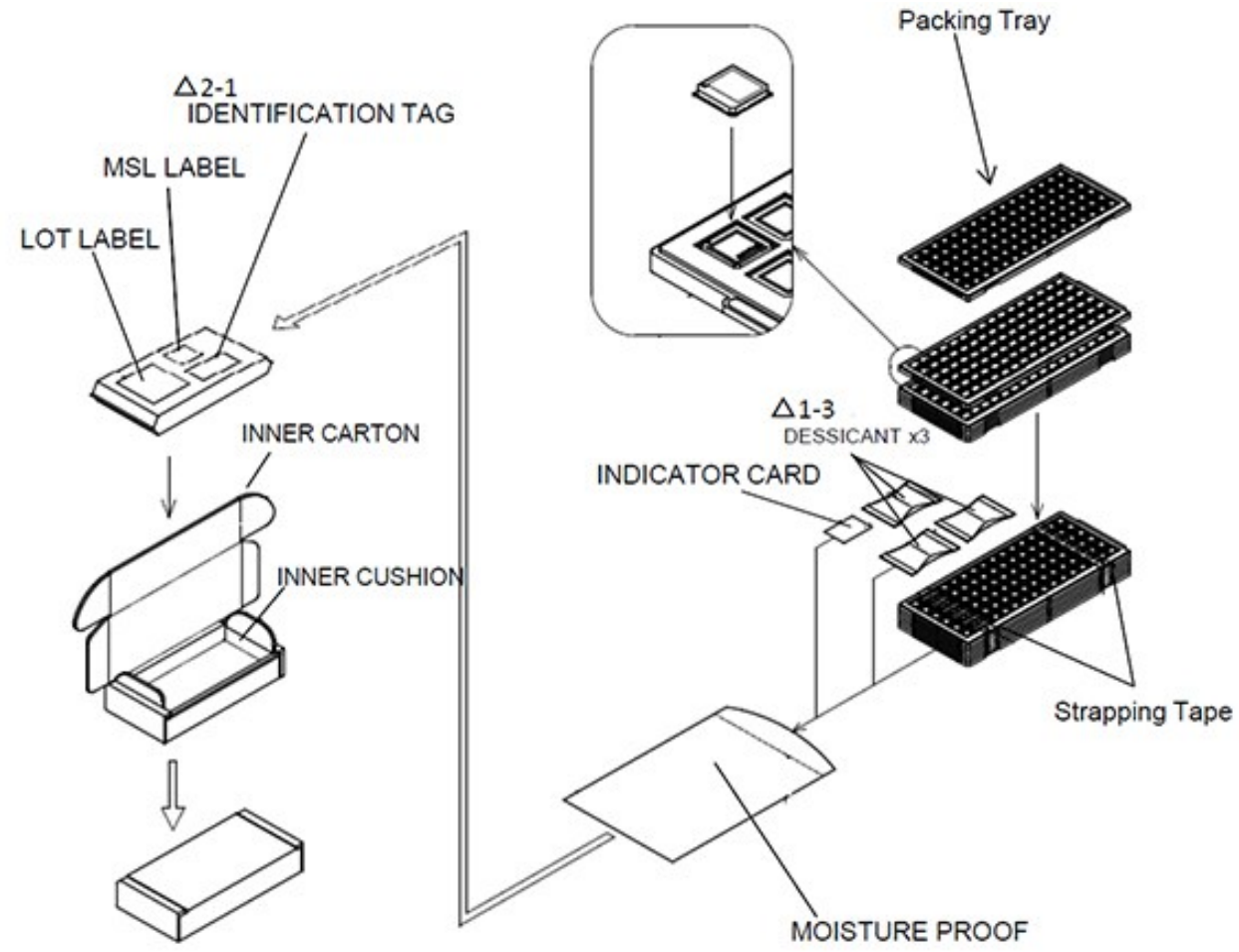
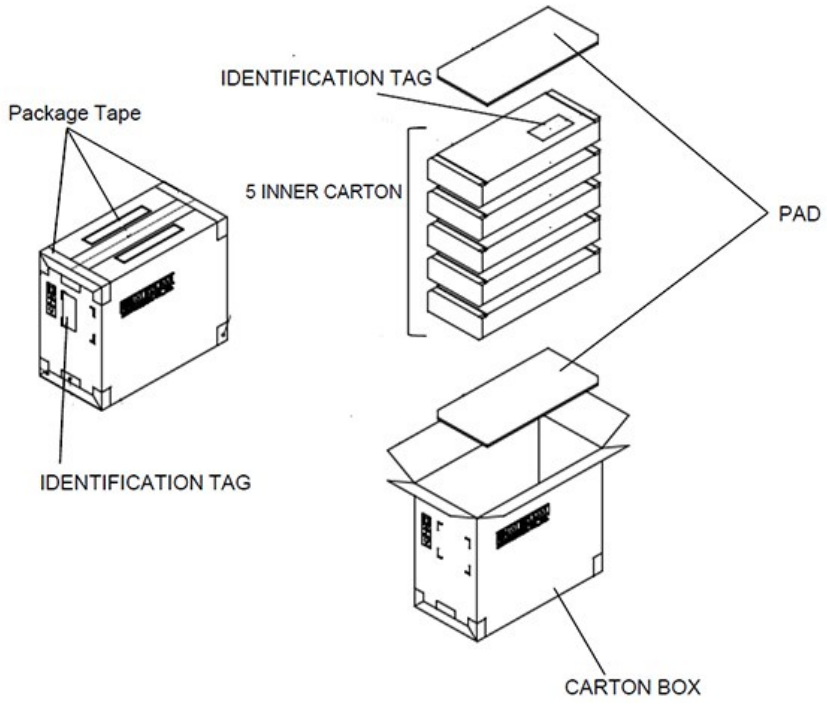


Figure 9: Inner carton

Notes:

- Each packing tray contains 96 products.
- Five packing trays (each with 96 products) are stacked with an empty packing tray on top. The stack is wrapped with strapping tape.
- The moisture-proof inner carton contains a total of 480 products (five trays).
- The MSL label, Lot label, and Identification tag are stuck on the moisture-proof carton.

16.2 Carton Box



Notes:

- The carton box holds five inner cartons (480 products in each carton).
- The carton box contains 2400 products.
- The Identification tag is stuck on the specified location of the inner carton and carton box.

Figure 10: Carton box

16.3 Labels

16.3.1 MSL Label

This product is classified as MSL4 devices.

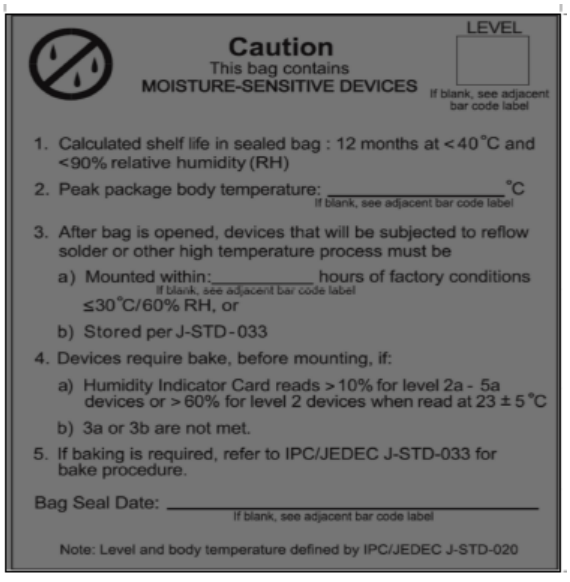


Figure 11: MSL label

16.4 Storage Condition and Baking Information

This product should be stored in a controlled temperature and humidity conditions according to Moisture Sensitivity Level (MSL) 4.

- The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
- Once the packaging is opened, the SiP must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <30 ˚C and <60% relative humidity.
- If the SiP is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125 ˚C (±5 ˚C).

17 Regulatory

Note: For complete regulatory information, refer to the SSD50NBT Regulatory Information document which is also available from the SSD50NBT product page.

The SSD50NBT holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-SSD50NBT
EU	N/A
Canada (ISED)	3147A-SSD50NBT

18 Ordering Information

Part Number	Description
SSD50NBT	2X2 802.11 a/b/g/n with BT4.0 dual mode module.

19 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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