User Guide

BL54L15µ Development Kit

Part # 453-00223-K1 and 453-00224-K1

Version 1.0

Revision History

Version	Date	Notes	Contributor(s)	Approver
0.1	29 Oct 2024	Initial version	Raj Khatri	Jonathan Kaye
0.2	19 Feb. 25	Modify the content for BL54L15u	Louis Chang	Jonathan Kaye
1.0	26 June 2025	Initial release	Louis Chang Dave Drogowski	Jonathan Kaye

Contents

1 Overview

The Ezurio DVK for the BL54L15µ modules series provides a platform for rapid wireless connectivity prototyping, providing multiple options for the development of Bluetooth Low Energy (BLE), 802.15.4 and Near Field Communication (NFC) applications.

The development kit is designed to enable customers to test and validate all the hardware interfaces of the BL54L15µ module and support the rapid development of application software using either Zephyr RTOS or Nordic Semiconductor nRFConnect SDK.

This document should be read in association with the DVK-BL54L15µ Schematics available on the BL54L15µ product page, Documentation section: https://www.ezurio .com/BL54L15µ-series

2 Ezurio BL54L15µ Development Kit Part Numbers

Part Number	Product Description
453-00223-K1	Development kit, Module, BL54L15µ (Nordic nRF54L15), Chip antenna
453-00224-K1	Development kit, Module, BL54L15µ (Nordic nRF54L15), RF Trace pin

Applicable to the following BL54L15µ module part numbers:

Part Number	Product Description
453-00223	Module, BL54L15µ, (Nordic nRF54L15), Chip antenna
453-00224	Module, BL54L15µ, (Nordic nRF54L15), RF Trace pin

3 Package Contents

All kits contain the following items:

Development Board	The development board has the required BL54L15µ module soldered onto it and exposes all available hardware interfaces.
Power Options	• USB cable (x1) – Type A to micro type C. The cable also provides serial communications via the USB – UART converter chip on the board.
Two-pin jumpers for pin headers (5)	Five jumpers for 2.54 mm pitch headers used on BL54L15µ development board.
Fly leads (6)	Supplied (1 by 1 female to female jumper cable) to allow simple connection of any BL54L15µ module pins (available on plated though holes or headers on TBD).
External BLE dipole antenna	Supplied with development kit part # 453-00224-K1 only. External antenna, 2 dBi, FlexPIFA (Ezurio part #001-0022) with integral RF coaxial cable with 100 mm length and IPEX-MHF4 compatible RF connector.
External NFC antenna	Ezurio NFC flexi-PCB antenna – Part # 0600-00061
DVK 'Legs'	4 x stand-off and 4 x associated nuts

4 BL54L15µ Development Kit – Main Development Board

This section describes the BL54L15µ development board hardware.

The BL54L15µ development board is a universal development tool that highlights the capabilities of the BL54L15µ module. The development kit is supplied in a default configuration which should be suitable for multiple experimentation options. It also offers several header connectors that help isolate on-board sensors and UART from the BL54L15µ module to create different configurations. This allows you to test different operating scenarios.

The board allows the BL54L15µ series module to physically connect to a PC via the supplied USB cable for development purposes. The development board provides USB1-to-Virtual COM port (UART0, UART1 on BL54L15µ) conversion through a Nordic nRF5340 debugger chip (U2).

4.1 Key Features

The BL54L15µ development board has the following features:

- BL54L15µ series module soldered onto the development board
- Powering the development board:
  - USB (type C) connector (J3)
- Powering the BL54L15µ module with regulated 1.8V or optional external voltage (from P6 header) anywhere between 1.7V to 3.6V.
  However, once using external voltage by P6 header, IO voltage of nRF5340 debug chip (U2) should follow this external voltage to work with BL54L15u, more detail please see 6.1 Power Supply
- USB(J3) to UART bridge (Nordic nRF5340 debugger chip, U2).
- BL54L15µ can have multiple UARTs, on DVK-BL54L15µ we have 2 UARTs that can be interfaced to:
  - USB (PC) (J3) using the USB-UART0 bridge (U2)
  - USB (PC) (J3) using the USB-UART1 bridge (U2)
- Current measuring options (BL54L15µ module only):
  - Pin header P6 (Ammeter) for measuring current.
  - Optional 10R Series resistor for differential measurement (oscilloscope).
- IO break-out 2.54 mm pitch 2pin header connectors in series on each GPIO of the BL54L15µ module – on which various interfaces UART0, UART1, SPI, High Speed SPI (32Mbps), QSPI, I2C, GPIO, AIN, NFC – and allow for plugging in external modules/sensors. These 2pin series header allows circuitry to be disconnected from BL54L15µ module (by removing jumpers).
- Multiple on-board sensors:
  - QSPI device (Nor flash) chip (U9) (connected by default)
  - Four buttons (BUTTON0, BUTTON1, BUTTON2, BUTTON3)
  - Four LEDs (LED0, LED1, LED2, LED3)
- One reset button SW1
- NFC antenna connector (J7) on-board development board for use with supplied flexi-PCB NFC antenna (0600-00061, see datasheet)
- *Optional* external 32.768 kHz crystal (X1) circuit (Not required for operation of the BL54L15µ). The 32.768 kHz crystal oscillator circuit requires load capacitor inside the nRF54L15 chipset to be enabled in software (and for X1 32.768kHz part, nRF54L15 provided load capacitance of 9pF should be used). The X1 crystal is connected by default BL54L15µ by closed solder bridges (SB3, SB4).
- *Optional* external serial (QSPI) Nor flash chip (U9). Not required for operation of the BL54L15µ; is connected by default. There is in parallel header connector J18 via open solder bridges to allow sampling of signals.
- Access to BL54L15µ Serial Wire Debug (SWD) 2-wire interface (JTAG) on P15.
- On-board SWD programmer circuitry formed by Nordic nRF5340 debugger chip (U2) that transforms USB to SWD interface (which then connects to BL54L15µ module SWD interface)
- FW upgrade or application loading HW capability:
  - Via SWD (USB to BL54L15µ SWD) using on-board SWD programmer circuitry (U2 nRF5340 debugger chip MCU) on the BL54L15µ Development Kit

5 Understanding the Development Board

Development board 453-00223-K1 (fitted with 453-00223 Module, BL54L15µ, (Nordic nRF54L15), Chip antenna)

5.1 BL54L15µ Default Configuration and Jumper Settings

Important! To ensure correct out-of-the-box configuration, the **BL54L15µ** development board switch and jumpers must be configured as shown in Figure 1.

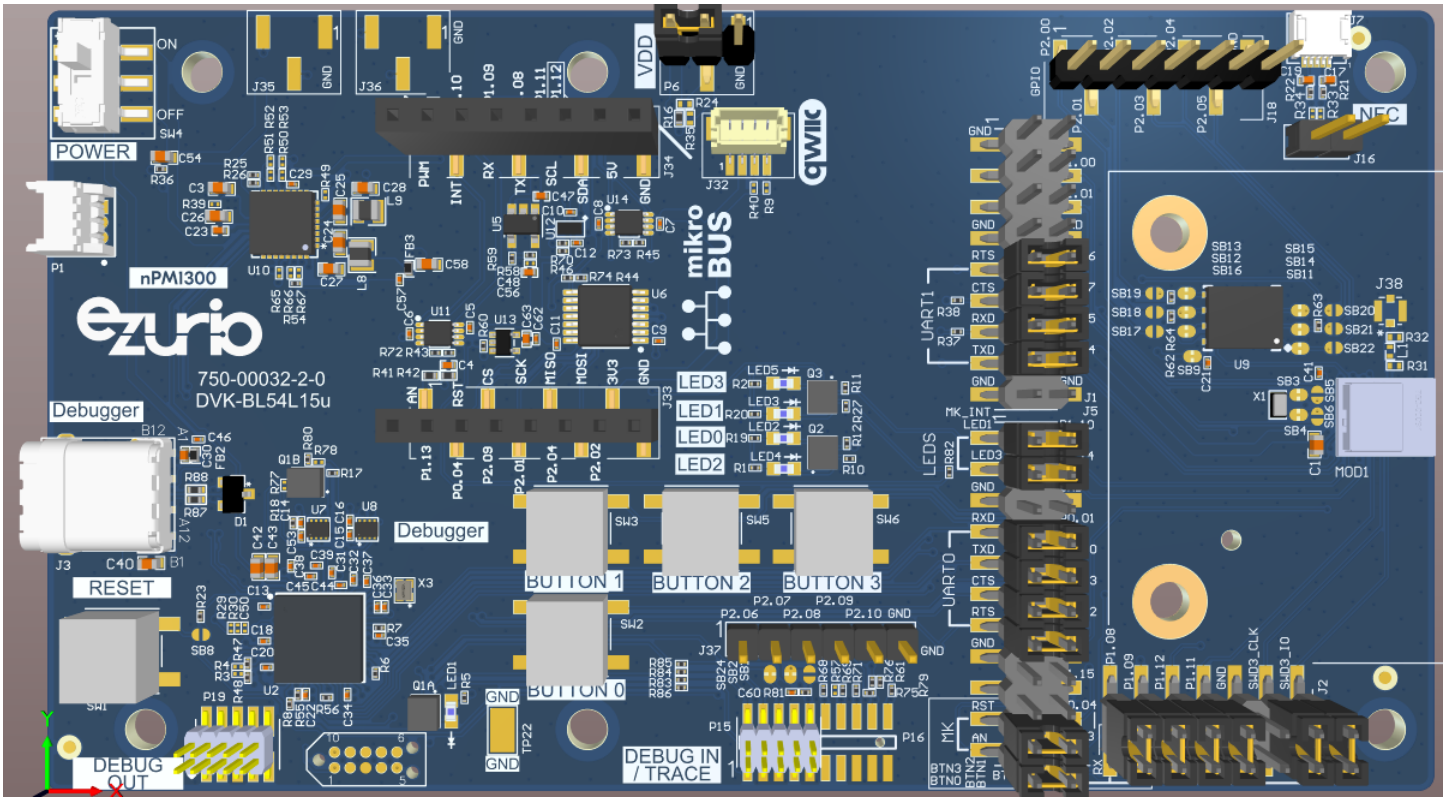


Figure 1: Correct BL54L15µ development board 453-00223-K1 or 453-00224-K1 jumper and switch settings (image for 453-00223-K1)

6 Functional Blocks

6.1 Power Supply

Figure 2 shows the BL54L15µ development board Power Supply block.

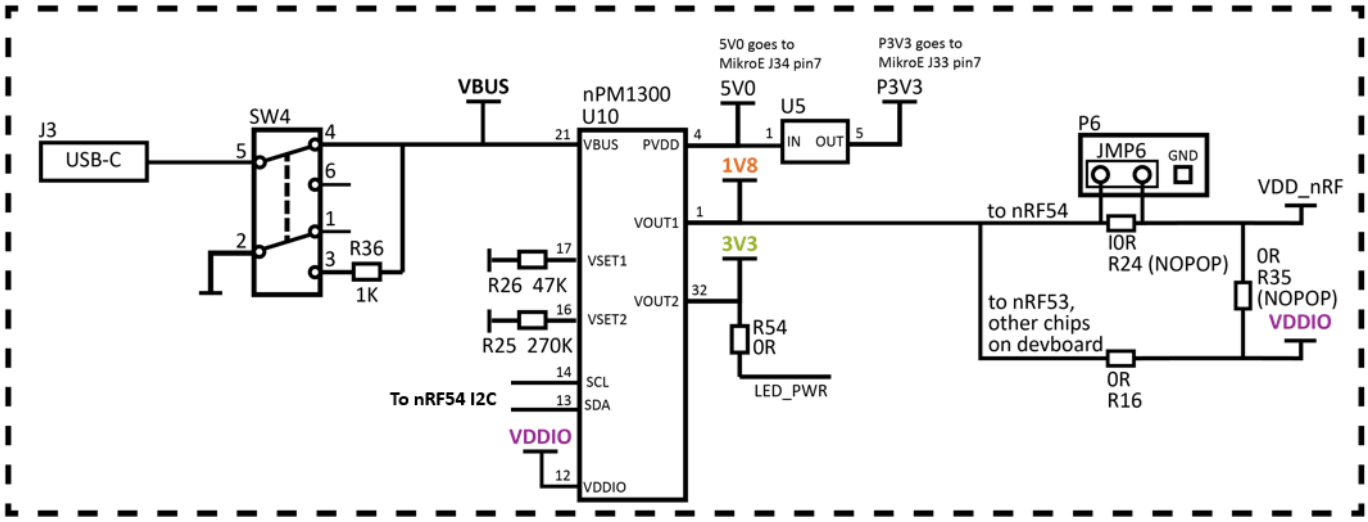


Figure 2: BL54L15µ development Kit power supply

The BL54L15µ development board is powered by:

- USB type C connector (J3)
  The USB cable supplied power (5V) goes into nPM1300 (U10) power management chip on the development board which produces 3.3V (on Vout2 pin) and 1.8V (on Vout1 pin). Please use SW4 to enable 5V goes to nPM1300 or not.

The BL54L15µ module is powered by connecting supply to following pin:

- VDD_nRF pin (operating range of 1.7V to 3.6V) – the development board generates 1.8V from the nPM1300 Vout1 pin to power the BL54L15µ module. This voltage can be adjusted with resistor R26 or by I2C command from the BL54L15µ module.

Note: The development board for BL54L15µ has on-board circuitry to allow access to BL54L15µ SWD interface (via USB connector J3). Refer to SWD (JTAG) Interface.

- VDD_nRF pin can also be powered from external power supply by using P6 header. However, in order to synchronize IO voltage between nRF5340 debug chip (U2) and BL54L15u, please depopulate R16 and fit R35 as 0 ohm. Figure 3 shows the PCB location of these two rework parts.

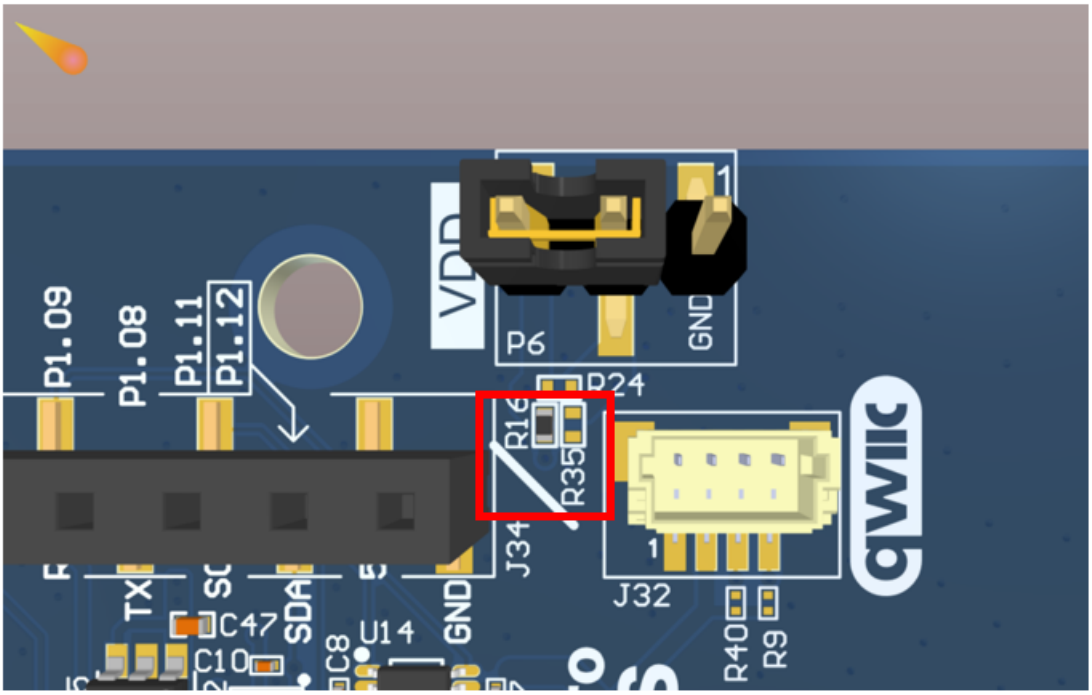


Figure 3: PCB location of these two rework parts for synchronizing the IO voltage of nRF5340 and BL54L15u

Power circuitry net names

On the development board, the power circuity net names are as follows:

- VBUS – This voltage from USB cable plugged into connector J3. The main development board power supplies nPM1300 power management chip (U10) which on output generates 3V3 on Vout2 pin and 1V8 on Vout1 pin.
- VBUSOUT – from nPM1300 (U10) used by debugger circuitry (U2) USB power pin.
- VDDIO – Supplies the IO supply of all other circuitry.
- VDD_DBGR – is just renamed VDDIO, used to power the debugger circuitry (U2).
- VDD_nRF – Supplies the BL54L15µ series module only. Current measuring block on the development board only measures the current into power domain VDD_nRF (that is current going into header P6 pin3-2).

6.2 Reset Button

The development board has a reset button (SW1) with the net name RESET_BUTTON. The RESET_BUTTON (is active low when SW1 pushed down) is used to control BL54L15µ module nRF54L15_RESET pin. The placement of the SW1 reset button and circuitry is shown in Figure 4.

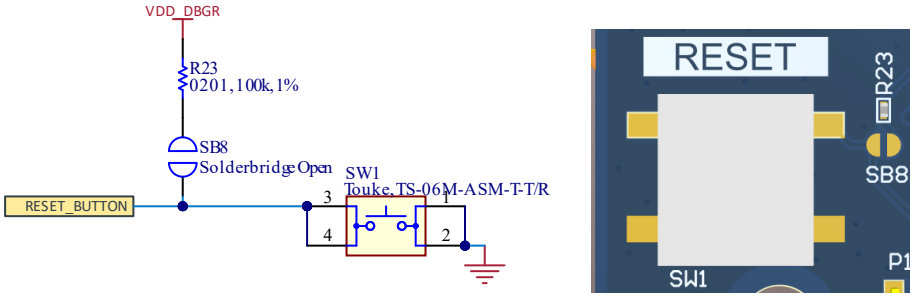


Figure 4: Reset button placement

BL54L15µ module reset (nRF54L15_RESET) can be driven by 2 sources:-

- reset button SW1 (net name RESET_BUTTON)
- P15 header pin10 (net name SWD_nRF54), see section 6.3 SWD (JTAG) Interface

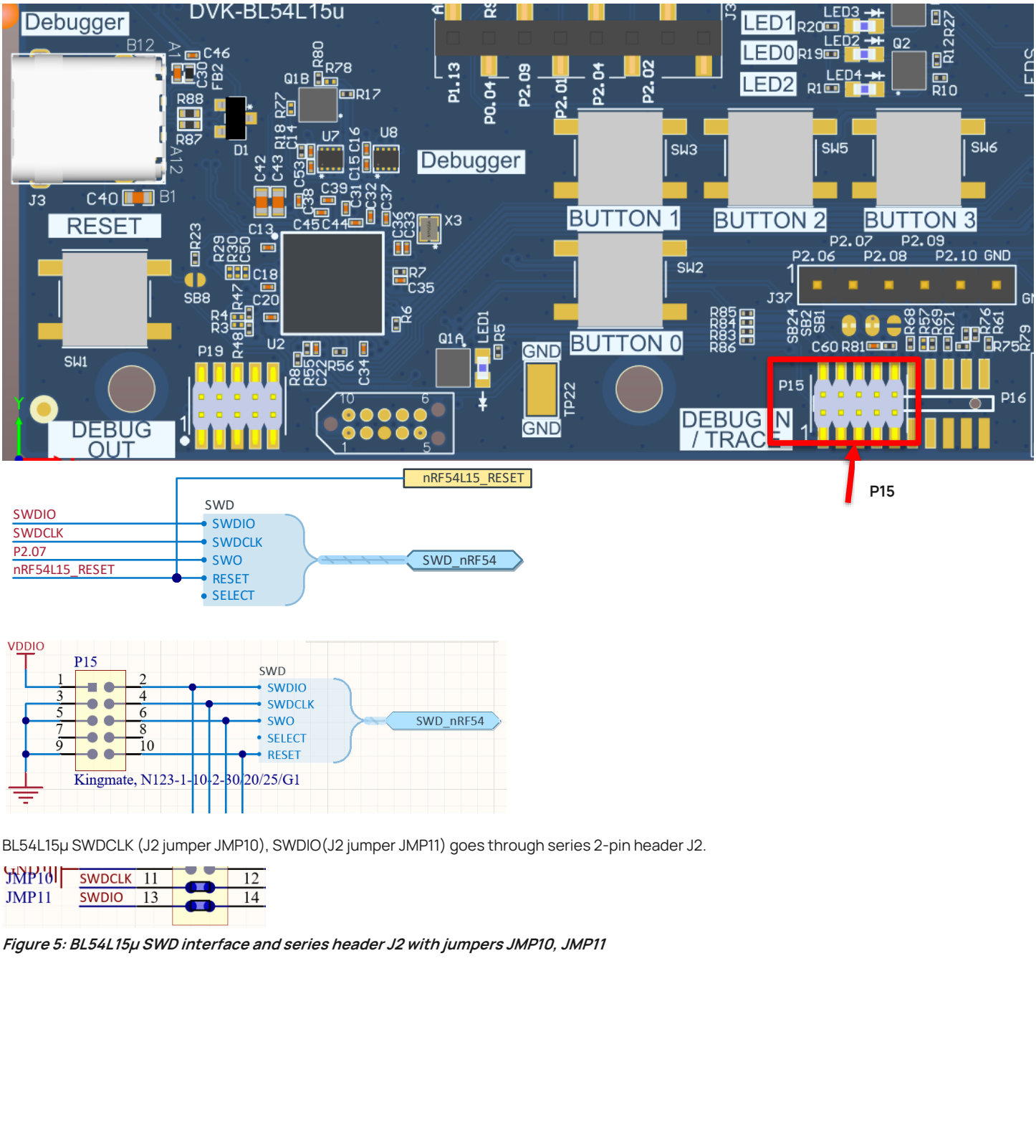
6.3 SWD (JTAG) Interface

The development board provides access to the BL54L15µ module two-wire SWD interface on P15. This SWD interface is REQUIRED for customer use for FW programming.

Note: We recommend SWD two-wire interface used for FW loading. Customer MUST wire out the SWD two-wire interface (namely SWDIO, SWDCLK, nReset, GND, and VCC).

For those customers that require access to BL54L15µ SWD (JTAG) interface, the BL54L15µ development board (see Understanding the Development Board) has on-board circuitry to allow access to BL54L15µ module SWD interface (via USB connector J3). The USB to SWD debugger circuitry is formed by Nordic nRF5340 (U2) debugger MCU).

Figure 5 shows the schematic, PCB location for USB-SWD on-board circuitry



BL54L15µ SWDCLK (J2 jumper JMP10), SWDIO (J2 jumper JMP11) goes through series 2-pin header J2.

Figure 5: BL54L15µ SWD interface and series header J2 with jumpers JMP10, JMP11

6.4 Four-wire UART Serial Interfaces

The BL54L15µ can have multiple four-wire UART's (TX, RX, CTS, RTS). On the DVK-BL54L15µ development board, 2 UARTs can be interfaced.

Note: The BL54L15µ module can provide multiple four-wire UART interfaces on the HW and the other four signals (DTR, DSR, DCD, RI), which are low bandwidth signals, can be implemented in FW (if required) using any spare digital GPIO pins.

6.4.1 UART0 Interface (on BL54L15µ) Driven by USB (J3) connector (USB to UART0 debugger chip U2)

- **USB Connector:** The development kit provides a USB Type C connector (J3) which allows connection to any USB host device. The connector also supplies power to the development kit and the USB(J3) signals are connected to debugger nRF5340 MCU (U2) to-serial converter device.
- **USB – UART0:** The development kit is fitted with a (U2) debugger nRF5340 USB-to-UART converter which provides USB-to-Virtual COM port (UART0 on BL54L15µ) on any Windows PC.

The UART0 connection on the DVK-BL54L15µ and the nRF5340 (U2) are shown in Table 1 and how the BL54L15µ series module UART0 is mapped to the breakout header connector J5.

Table 1: UART0 connections on DVK-BL54L15µ

BL54L15µ (MOD1) pin	BL54L15µ module UART0 assigned	nRF5340 (U2) IC UART0 _DBGR	Comments
P0.00 (pin38)	UART0_TX (output)	RX0	via J5 header (pins 9-10) JMP15
P0.01 (pin35)	UART0_RX (input)	TX0	via J5 header (pins 7-8) JMP14
P0.02 (pin30)	UART0_RTS (output)	CTS	via J5 header (pins 13-14) JMP17
P0.03 (pin33)	UART0_CTS (input)	RTS	via J5 header (pins 11-12) JMP16

6.4.2 UART1 Interface (on BL54L15µ) Driven by USB (J3) connector (USB to UART1 debugger chip U2)

- **USB Connector:** The development kit provides a USB Type C connector (J3) which allows connection to any USB host device. The connector also supplies power to the development kit and the USB(J3) signals are connected to debugger nRF5340 MCU (U2) to-serial converter device.
- **USB – UART1:** The development kit is fitted with a (U2) debugger nRF5340 USB-to-UART converter which provides USB-to-Virtual COM port (UART1 on BL54L15µ) on any Windows PC.

The UART1 connection on the DVK-BL54L15µ and the nRF5340 (U2) are shown in Table 2 and how the BL54L15µ series module UART1 is mapped to the breakout header connector J1.

Table 2: UART1 connections on DVK-BL54L15µ

BL54L15µ (MOD1) pin	BL54L15µ module UART1 assigned	nRF5340 (U2) IC UART1 _DBGR	Comments
P1.04 (pin17)	UART1_TX (output)	RX0	via J1 header (pins 15-16) JMP4
P1.05 (pin15)	UART1_RX (input)	TX0	via J1 header (pins 13-14) JMP3
P1.06 (pin7)	UART1_RTS (output)	CTS	via J1 header (pins 9-10) JMP1
P1.07(pin8)	UART1_CTS (input)	RTS	via J1 header (pins 11-12) JMP2

7 Software for Communicating to BL54L15µ UART0 and UART1

The development board connects the BL54L15µ module to a virtual COM port (UART0 or UART1) of a PC or other device. From a PC, you can communicate with the module using a terminal emulator like PuTTY https://www.chiark.greenend.org.uk/~sgtatham/putty/

This utility allows connections to serial devices using any combination of the communications parameters listed in Table 3. If you want to send commands via UART PuTTY settings can be seen https://developer.nordicsemi.com/nRF_Connect_SDK/doc/latest/nrf/gs_testing.html

Table 3: PuTTY communication parameters for BL54L15µ

Port (Windows)	1 to 255
Port (Mac/Linux)	Any /dev/tty device
Baud Rate	1200 to 1000000 **Note:** Baud rate default is 19200 for BL54L15µ.
Parity	None
Data Bits	8
Stop Bits	1
Handshaking	None or CTS/RTS

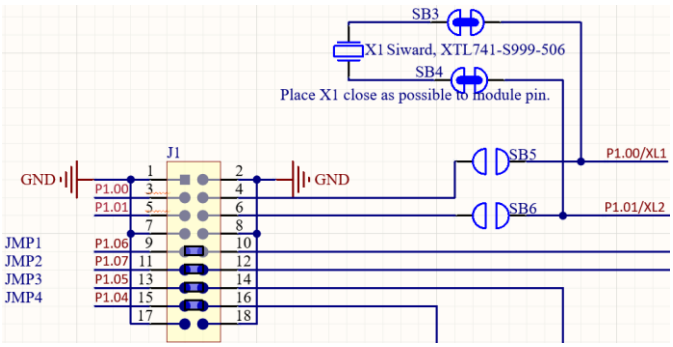
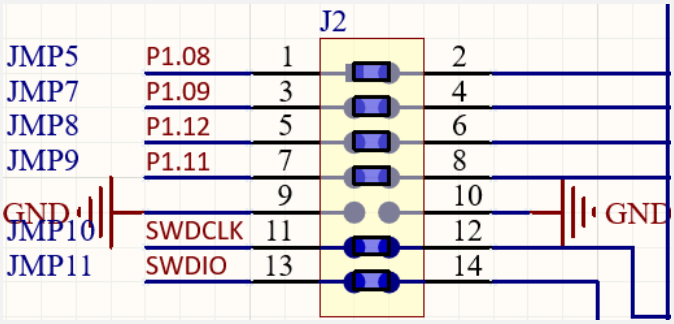
7.1 GPIO Breakout Connectors

Access to all 32 x BL54L15µ series module signal pins (GPIO = General Purpose Input /Output) is available on 2.54mm pitch header connectors on J1, J2, J5, J37, J18, J16 (2.54mm header connector).

These breakout connectors can interface to a wide array of sensors via customer developed FW, and the DVK incorporates additional fly-lead cables inside the box to enable simple, hassle-free testing of these multiple interfaces.

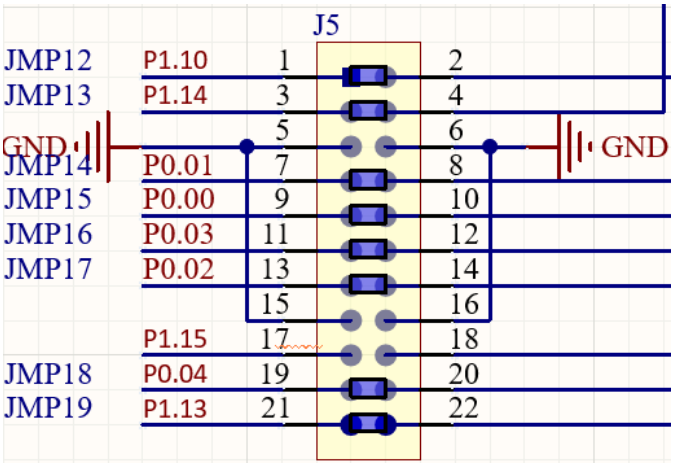
Table 4 shows the BL54L15µ module pins that are brought out to 2.54mm pitch header connectors and plated through holes (suitable for 2.54 mm pitch headers).

Table 4: Module pins exposed via in-series header pins and jumpers

Header Connector		BL54L15µ Module Signals Exposed
J1		BL54L15µ pin header J1 for access: • P1.00/XL1 • P1.01/XL2 • GND • P1.06 (via JMP1 routes UART1_RTS to debugger U2) • P1.07 (via JMP2 routes UART1_CTS to debugger U2) • P1.05 (via JMP3 routes UART1_RXD to debugger U2) • P1.04 (via JMP4 routes UART1_TXD to debugger U2) • GND BL54L15µ pins • P1.00/XL1 • P1.01/XL2 Accessed on J1 via open solder brides SB5, SB6. By default, the optional external 32.768 kHz crystal circuit is connected to BL54L15µ via closed solderbridge SB3 and SB4. To use P1.00, P1.01 as GPIO on J1 header, then cut SB3, SB4 and solder connect SB5, SB6.
J2		BL54L15µ pin header J2 for access: • P1.08 (via JMP5 to Button2) routes to UART_RX (MikroE RX) • P1.09 (via JMP7 to Button1) routes to UART_TX (MikroE TX) • P1.12 (via JMP8) routes to I2C_SDA (MikroE I2C_SDA) • P1.11 (via JMP9) routes to I2C_SCL (MikroE I2C_SCL) • GND • SWDCLK (via JMP10 routes debugger U2) • SWDIO (via JMP11 routes debugger U2)

Header Connector	BL54L15µ Module Signals Exposed

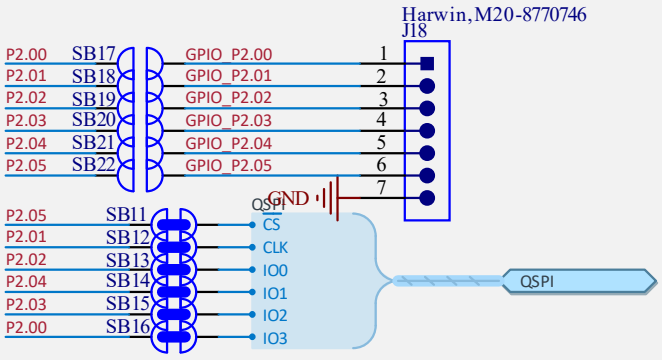
J5



BL54L15µ pin header J5 for access:

- P1.10 (via JMP12 to LED1)
- P1.14 (via JMP13 to LED3 and MikroE_PWM)
- GND
- P0.01 (via JMP14 routes UART0_RXD to debugger U2)
- P0.00 (via JMP15 routes UART0_TXD to debugger U2)
- P0.03 (via JM16 routes UART0_CTS to debugger U2
- P0.02 (via JMP17 routes UART0_RTS to debugger U2)
- P1.15
- GND
- P0.04 (via JMP18 to Button3) routes to MikroE Reset
- P1.13 (via JMP19 to Button0) routes to MikroE Analog

J18

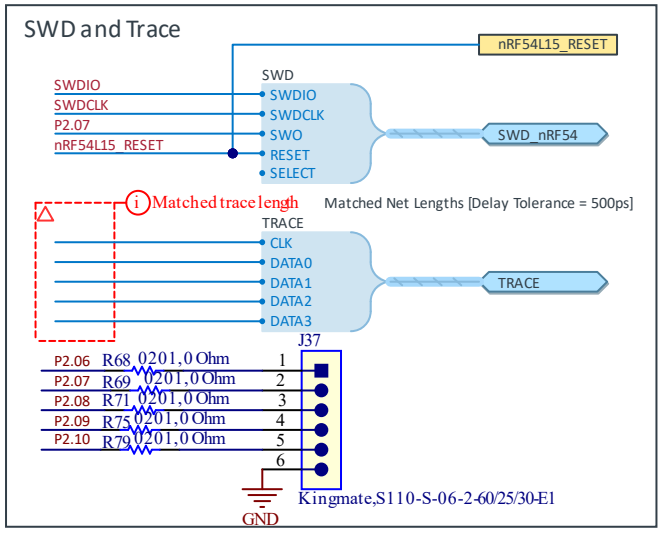


BL54L15µ pin header J18 for access provides parallel access to:

- P2.00 (via open solderbridge SB17)
- P2.01 (via open solderbridge SB18)
- P2.02 (via open solderbridge SB19)
- P2.03 (via open solderbridge SB20)
- P2.04 (via open solderbridge SB21)
- P2.05 (via open solderbridge SB22)
- GND

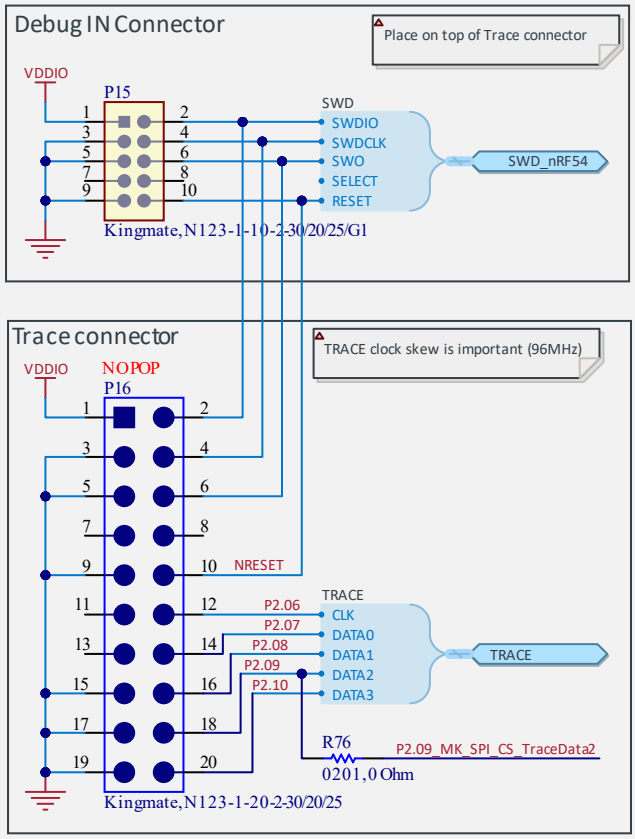
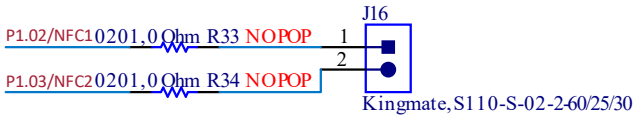
which are directly connected to QSPI chip U9. To disconnect QSPI chip U9 from BL54L15µ, cut solderbridges SB11, SB12, SB13, SB14, SB15, SB16.

J37



BL54L15µ pin header J37 for access:

- P2.06 (via R68) and traceCLK
- P2.07 (via R69) which routes to also LED2 and
  - MikroE PWM and
  - MikroE SPI_DCX and
  - SWO
  - TraceData0
- P2.08 (via R71) and TraceData1
- P2.09 (via R75) routes to also LED0 and
  - MikroE SPI_CS (via R61)
  - TraceData2
- P2.10 (via R79) and TraceData3
- GND

Header Connector	BL54L15µ Module Signals Exposed
P15 	P15 header brings access BL54L15µ module SWD interface. • SWDIO • SWDCLK • SWO • nRESET
J16 	BL54L15µ pin header for access: • P1.02 via R33 0R (default NOPOP) • P1.03 via R34 0R (default NOPOP) To use NFC1 pin as P1.02 GPIO fit R33 0R, remove R21 To use NFC2 pin as P1.03 GPIO fit RR34 0R, remove R22

7.2 Additional Peripherals/Sensors

The BL54L15µ development board provides for simple and hassle-free connectivity to a wide range of sensors, but also includes several on-board sensors and options to enable a developer to test functionality straight out of the box.

7.2.1 MikroE and Qwiic connectors

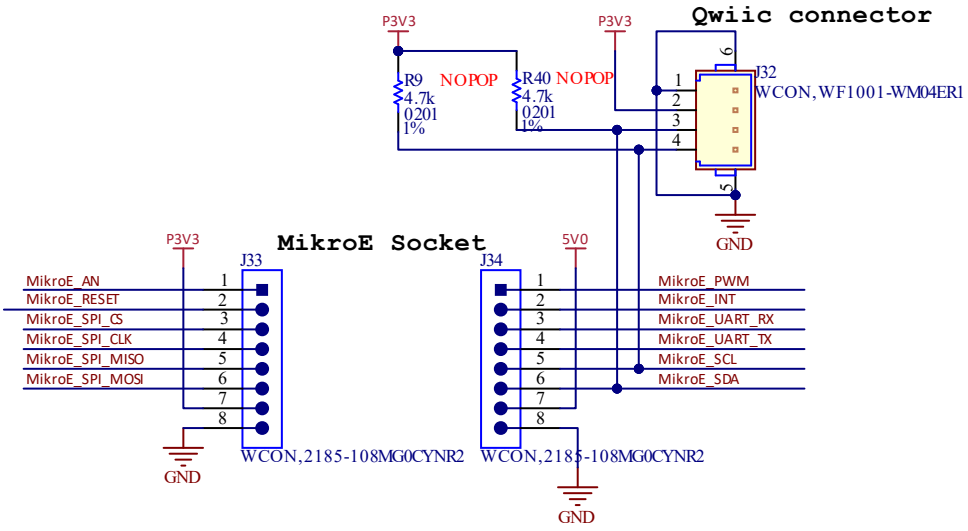


Table 5: MikroE connector J33 signal via level shifter chip (U13, U6, U5) on DVK-BL54L15µ to BL54L15µ module signal mappings

MikroE connector, pin	MikroE signal	via level shifter	BL54L15µ module (MOD1) pin signal	Comments
J33pin1	MikroE_AN	R41. R42 resistive divider	P1.13	P1.13 shared with Button0
J33pin2	MikroE_RESET	U13	P0.04	P0.04 shared with Button3
J33pin3	MikroE_SPI_CS	U6	P2.09 via R61	P2.09 shared with LED0
J33pin4	MikroE_SPI_CLK	U6	P2.01 via R62	P2.01 shared with QSPI_SCK
J33pin5	MikroE_SPI_MISO	U6	P2.04 via R63	P2.04 shared with QSPI_IO1
J33pin6	MikroE_SPI_MOSI	U6	P2.02 via R64	P2.02 shared with QSPI_IO0
J33pin7	P3V3	Generated by LDO U5		
J33pin8	GND			

Table 6: MikroE connector J34 signal via level shifter chip (U11, U14, U12) on DVK-BL54L15µ to BL54L15µ module signal mappings

MikroE connector, pin	MikroE signal	via level shifter	BL54L15µ module (MOD1) pin signal	Comments
J34pin1	MikroE_PWM	U11	P2.07 P1.14	P2.07 shared with LED2, TraeData0, SWO P1.14 shared with LED3
J34pin2	MikroE_INT	U11	P1.10	P1.10 shared with LED1
J34pin3	MikroE_UART_RX	U14	P1.08	P1.08 shared with Button2
J34pin4	MikroE_UART_TX	U14	P1.09	P1.09 shared with Button1
J34pin5	MikroE_SCL	U12	P1.11	P1.11 shared with BL54L15µ, debugger chip nRF5340 and nPM1300
J34pin6	MikroE_SDA	U12	P1.12	P1.12 shared with BL54L15µ, debugger chip nRF5340 and nPM1300
J34pin7	5V0	From nPM1300		
J34pin8	GND			

Table 7: Qwiic connector J32 signal on DVK-BL54L15µ to BL54L15µ module signal mappings

Qwiic connector, pin	MikroE signal	via level shifter	BL54L15µ module (MOD1) pin signal	Comments
J32pin1	GND			
J32pin2	P3V3			
J32pin3	MikroE_SDA		P1.11	P1.11 shared with BL54L15µ, debugger chip nRF5340 and nPM1300
J32pin4	MikroE_SCL		P1.12	P1.12 shared with BL54L15µ, debugger chip nRF5340 and nPM1300

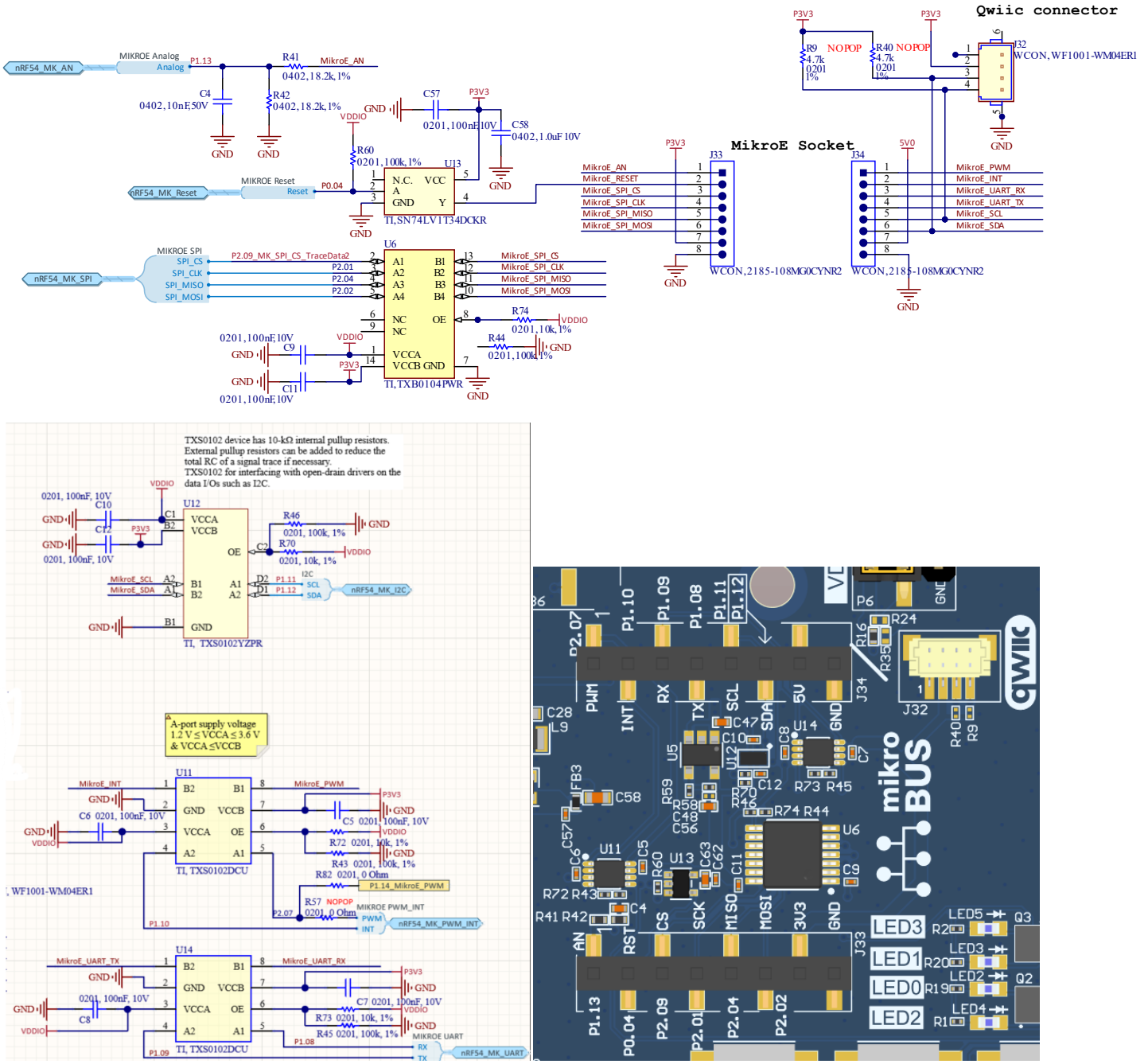


Figure 6: MikroE and Qwiic connectors, level shifters circuitry

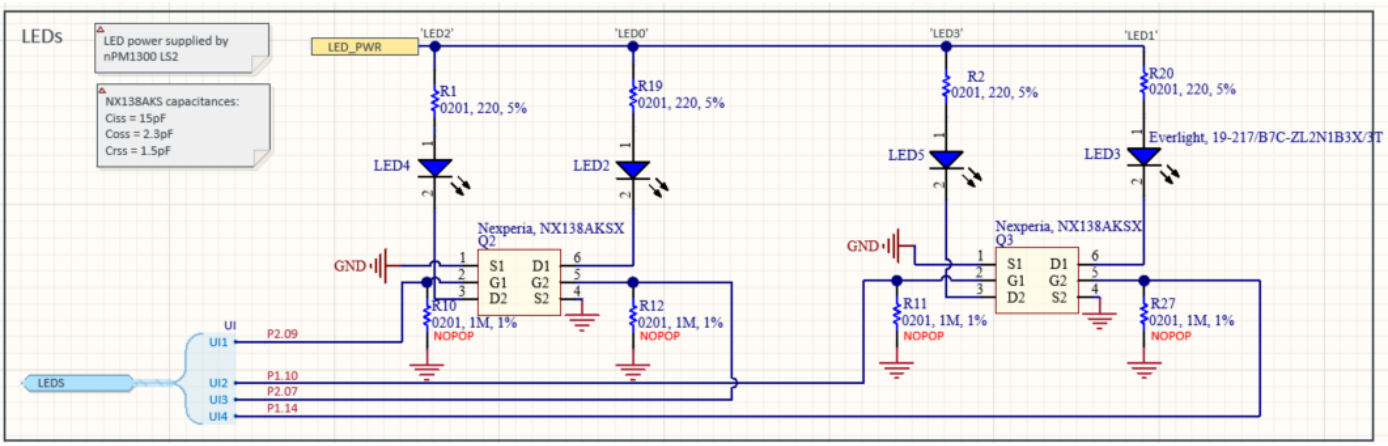
Level shifters U6 (for MikroE SPI), U11(MikroE PWM, INT), U14(MikroE UART), U12(MikroE I2C) are needed adapt 3.3V IO of MikroE to the BL54L15µ IO voltage.

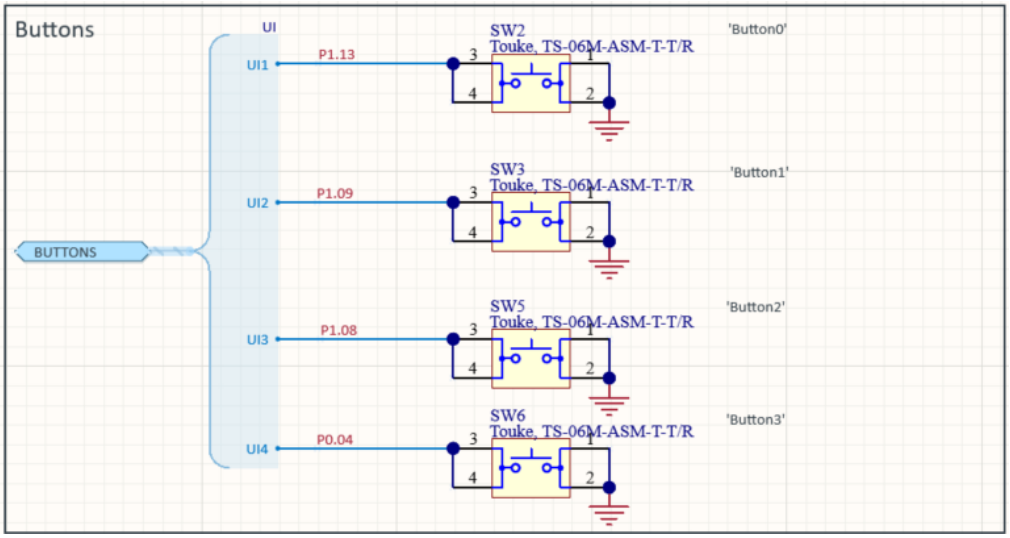
7.2.2 4 Buttons and 4 LEDs connected to BL54L15µ

Four Buttons, four LEDs are connected to the BL54L15µ pins via pin headers. Table 8 lists signal mappings

Table 8: LEDs and Buttons on BL54L15µ devboard to BL54L15µ module signal mappings

LED, Button	BL54L15µ module (MOD1) pin	Comments
LED2	P2.07	P2.07 shared with SWO, TraceData0 and with MikroE_PWM
LED3	P1.14	P1.14 shared with MikroE Reset
LED0	P2.09	P2.09 shared with TraceData2 and with MikroE_SPI_CS
LED1	P1.10	P1.10 shared with MikroE_INT
Button0	P1.13	P1.09 shared with MikroE Analog
Button1	P1.09	P1.09 shared with MikroE UART TX
Button2	P1.08	P1.08 shared with MikroE UART RX
Button3	P0.04	P0.04 shared with MikroE Reset





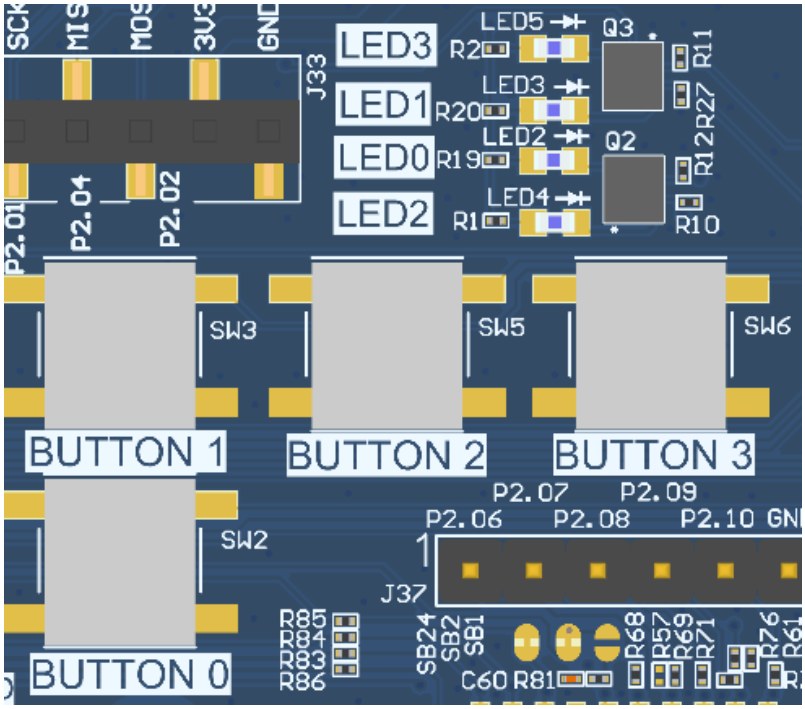


Figure 7: LEDs and Buttons schematic and PCB

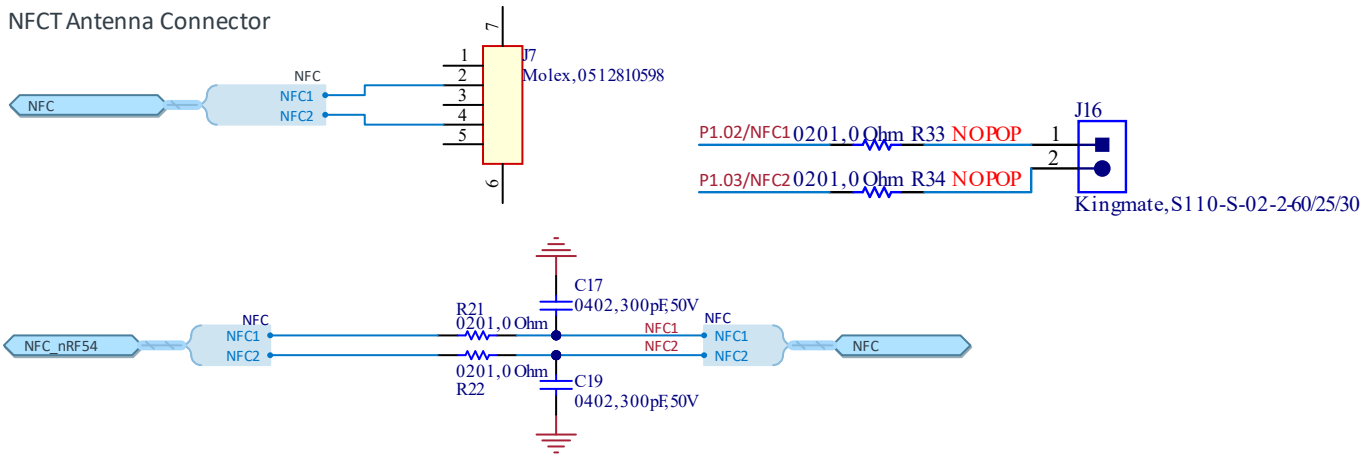
7.2.3 NFC External Antenna Connector and NFC Antenna RF Matching Circuit

The NFC antenna input connector (J7) allows the Ezurio-supplied flex-PCB NFC antenna to be plugged in. The BL54L15µ module NFC circuit uses two pins, pin 11 (**NFC1/P1.02**) and pin 9 (**NFC2/P1.03**) to connect the antenna. These pins are shared with GPIOs (**P1.02** and **P1.03).** Pin 11 (**NFC1/P0.02**) and pin 9 (**NFC2/P0.03**) are configured by default on the development board schematic to use NFC antenna, but if pin 11 (**NFC1/P1.02**) and pin 9 (**NFC2/P1.03**) are needed as normal GPIOs, R21 and R22 must be removed and R33 and R34 must be shorted by 0R.

C53 (300pF) and C54 (300pF) are RF tuning elements for the flexi-PCB NFC antenna (see datasheet).

Table 9: NFC input BL54L15µ signal mappings

BL54L15µ (MOD1) pin	Bring out P0.02 and P0.03 to NFC antenna connector (J7)	Bring out P1.02 and P1.03 to Header connector (J16)
(MOD1 pin11) **P1.02/NFC1**	default connected	Fit R33 0R
(MOD1 pin9) **P1.03/NFC2**	default connected	Fit R34 0R



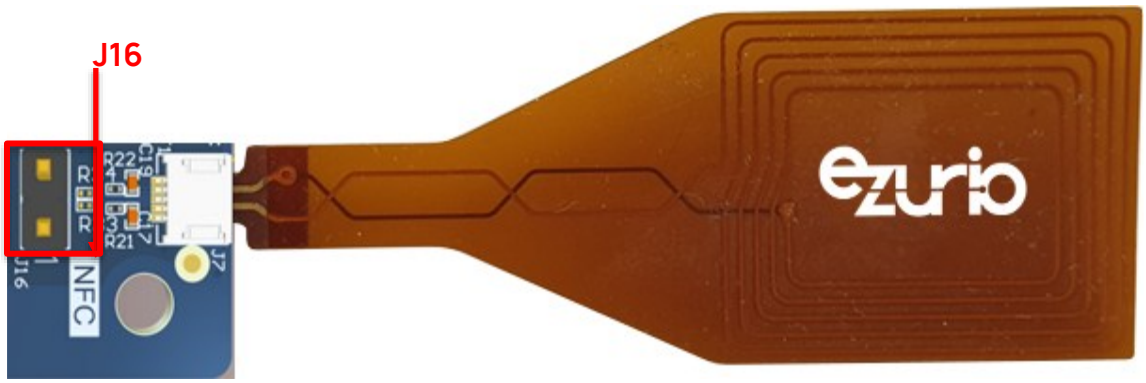


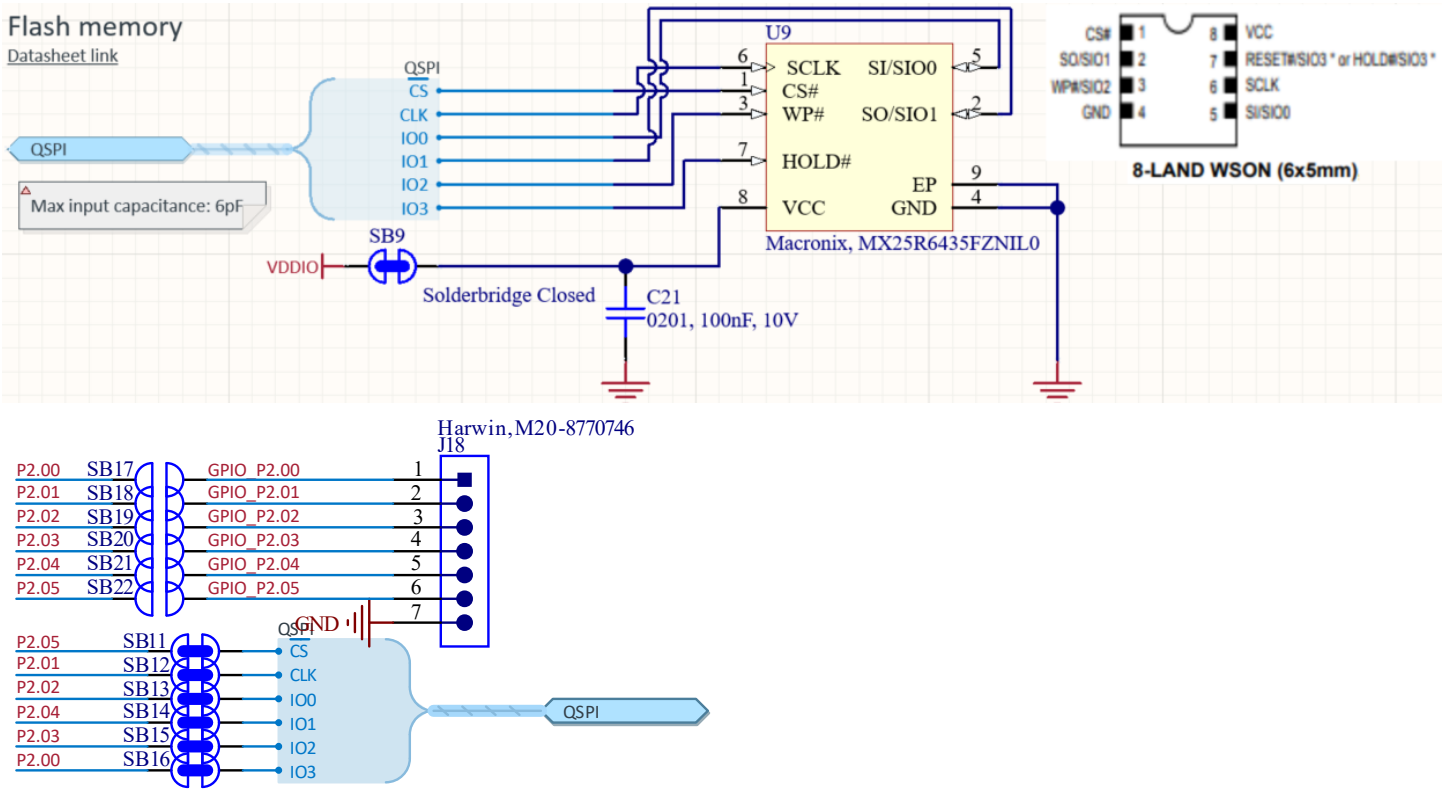
Figure 8: NFC antenna RF matching circuit, NFC antenna connector schematic and NFC plugged in to connector J7

7.2.4 Optional External Serial QSPI Flash IC

There is an optional external serial QSPI Nor flash IC (U9) that may be used, for example, for data logging purposes. U9 can also be capable of SPI mode.

Closed solder bridges SB11, SB12, SB13, SB14, SB15 and SB16 by default connects this optional external serial (QSPI) flash (U9 to the BL54L15µ module(mod1).

By default, these BL54L15µ pins are GPIO pins.



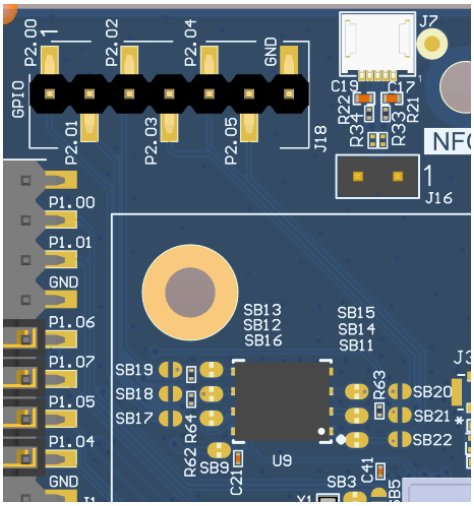


Figure 9: Optional external serial QSPI flash IC (U9) schematic and PCB

Table 10 shows the U9 pin mapping to BL54L15µ GPIO pin mapping (via closed solder bridges).

Table 10: U9 QSPI (or SPI) flash IC pin mapping to BL54L15µ GPIO mappings

BL54L15µ (MOD1) pin	BL54L15µ GPIO	U9 Pin (QSPI flash IC) and Pin Name	Via Closed Solder bridge
pin1	P2.05/QSPI_CSN	Pin 1 CS#	SB11 Drive from BL54L15µ line low to select.
pin6	P2.01/QSPI_CLK	Pin 6 SCLK	SB12
pin13	P2.02/QSPI_IO0	Pin 5 SIO0/SI	SB13
pin45	P2.04/QSPI_IO1	Pin 2 SIO1/SO	SB14
pin44	P2.03/QSPI_IO2	Pin 3 SIO2/WP#	SB15
Pin2	P2.00/QSPI_IO3	Pin 7 SIO3/HOLD#	SB16

Link to datasheet for QSPI device flash chip (U1),
http://www.macronix.com/Lists/Datasheet/Attachments/7428/MX25R6435F,%20Wide%20Range,%2064Mb,%20v1.4.pdf

Manufacturer: Macronix
Manufacturer part number: MX25R6435FZNIL0

7.2.5 Optional 32.768 kHz Crystal

The BL54L15µ on-chip 32.768kHz RC oscillator provides the standard accuracy of ±250 ppm, with calibration required every 8 seconds (default) to stay within ±250 ppm.

The BL54L15µ also allows, as an option, to connect an external higher accuracy (±20 ppm) 32.768 kHz crystal to the BL54L15µ pins P1.00/XL1 (pin 12) and P1.01/XL2 (pin 10). This provides improved protocol timing and helps with radio power consumption in the system on idle /system off sleep modes by reducing the time that the Rx window must be open.

By default, the optional external 32.768kHz crystal oscillator circuit is connected to the BL54L15µ module, cut SB3 and SB4 (to disconnect tracks going to X1).

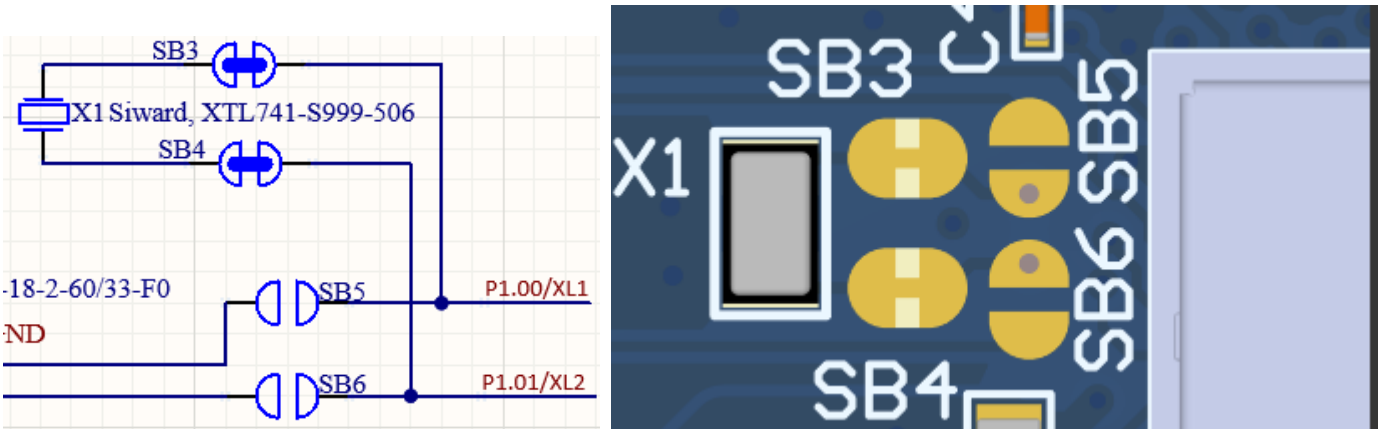


Figure 10: Optional external 32.768kHz crystal (X1) circuit schematic and PCB

The load capacitor inside the nRF54L15u for LFXO is set to 17.5pF in Firmware, customer can use Quartz Watch Analyzer by coupling method to fine tune the internal nRF54L15 capacitors on the customer board from 4 pF to 18 pF in 0.5pF step if needed.

8 Other Features

8.1 Current Consumption Measurement

A removable jumper (P6) is provided to break the power supply line directly to the module, allowing you to measure current consumption.

For BL54L15µ to measure current use header P6 (with jumper in P6pin3-2).

IMPORTANT: To achieve the optimal power consumption of the BL54L15µ series module on the development board, see the Nordic System OFF sample application https://github.com/zephyrproject-rtos/zephyr/tree/master/samples/boards/nrf/system_off DVK-BL54L15µ

Note: This measures the current consumption of the **BL54L15µ** series module ONLY.

The current drawn by the BL54L15µ series module can be monitored on the development board. Figure 11 shows the schematic and location of measuring points on the PCB related to current measurements.

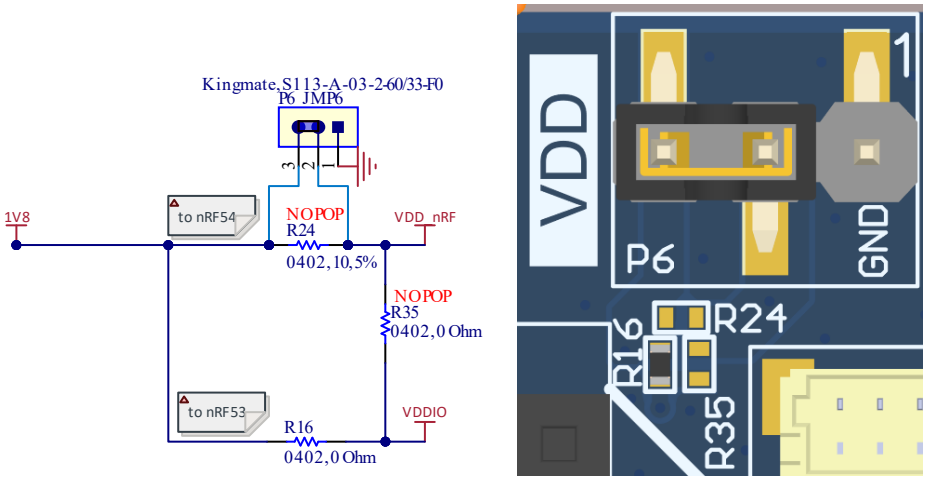


Figure 11: Current measurement schematic and PCB

There are three primary ways to measure the current consumption:

- **Using Ammeter –** the BL54L15µ is powered using the normal voltage Mode (BL54L15µ operated VDD_nRF), then remove jumper JMP6 and connect an ampere meter between the two pins of P6 pins 2-3.
- **Using Oscilloscope –** fit 10Ohm resistor R24 which is mounted across P6pins 2-3 can be used as current sense resistor.
  Connect an oscilloscope or similar with two probes on the pins on the connector P6-pin3-2 and measure the differential voltage drop. The voltage drop is proportional with current consumption. If the 10 Ohm resistor is chosen, 10 mV equals 1mA.
  This method allows the dynamic current consumption waveforms to be shown on an oscilloscope as the BL54L15µ radio operates. This can provide insight into power optimization.
- **Power Profiler Kit (PPK) from Nordic –** For more details, refer to http://www.nordicsemi.com/eng/Products/Power-Profiler-Kit/(language)/eng-GB

9 Additional Information

Please contact your local sales representative or our support team for further assistance:

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