Datasheet

Sterling™ LWB+

Version 2.2

Revision History

Version	Date	Notes	Contributors	Approver
1.0	26 Jan 2022	Initial version	Andrew Chen	Andrew Ross
1.1	17 Feb 2022	Clarified MSL Level 4 for LWB+ Series	Connie Lin	Jonathan Kaye
1.2	20 Feb 2022	Correct WL_Host_WAKE to pin-11	Andrew Chen	Andrew Ross
1.3	14 April 2022	Removed parts 001-0001 / 080-0001	Dave Drogowski	Andrew Ross
1.4	4 Oct 2022	Corrected Figure 10 to "WLAN OFF and BT OFF"	Dave Drogowski	Miles Chung
1.5	28 Nov 2022	Add LWB+ M.2 series. Added Figure 8: Sterling LWB+ M.2 2230 block diagram	Andrew Chen	Dave Drogowski
1.6	December 8, 2022	Update Figure 5: Sterling LWB+ base SiP module block diagram Figure 6: Sterling LWB+ MHF® 4 module block diagram Figure 7: Sterling LWB+ chip antenna module block diagram	Andrew Chen	Dave Drogowski
1.7	17 Feb 2023	Added updated Terms and Conditions	Dave Drogowski	Elaine Baxter
1.8	12 Mar 2024	Added section 20, Chip Antenna Performance Added Package Drawings	Adam Engelbrecht Connie Lin	Andy Ross
1.9	1 Nov 2024	Updated Bluetooth SIG Qualification.	Dave Drogowski	Jonathan Kaye
2.0	26 Mar 2025	Ezurio rebranding	Andrew Chen	Andy Ross
2.1	28 Apr 2025	Remove "Module accessories" table.	Andrew Chen	Andy Ross
2.2	12 Sep 2025	Update Figure 19: Sterling LWB+ MHF4 and chip antenna module pinout (top view)	Louis Chang	Dave Drogowski

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1 Scope

This document describes key hardware aspects of the Ezurio Sterling-LWB™ +.

2 Introduction

2.1 General Description

The Sterling LWB+ is a high performance 2.4 GHz WLAN and Bluetooth combo module based on latest-generation silicon (Infineon's AIROC™ CYW43439). With an industrial temperature rating, broad country certifications, and the availability of three different package styles, the Sterling LWB+ provides significant flexibility to meet various end user application needs. The Sterling LWB+ is the successor of Ezurio Sterling LWB product series. Two SMT type modules are even pin-to-pin and drop replacement to the platform using Sterling LWB.

The on-module chip antenna package style for the Sterling LWB+ eliminates complexity for design integration, simplifies manufacturing assembly with larger pin outs, and features an advanced chip antenna that offers greater resistance to de-tuning than typical trace or chip antennas.

The module includes the MAC, baseband, and radio to support WLAN applications and an independent, high-speed UART is provided for the Bluetooth host interface. In addition, the latest Linux and Android drivers are supported directly by Ezurio and Infineon.

Features

- IEEE 802.11 b/g/n (single stream n)
- Typical WLAN Transmit Power:
  - +18.0 dBm, 11 Mbps, CCK (b)
  - +16.0 dBm, 54 Mbps, OFDM (g)
  - +15.0 dBm, HT20 MCS7 (n)
- Typical WLAN Sensitivity:
  - -88 dBm, 8% PER,11 Mbps (b)
  - -75 dBm, 10% PER, 54 Mbps (g)
  - -72 dBm, 10% PER, MCS7 (n)
- Bluetooth v5.0 BR /EDR/LE
- Typical Bluetooth Transmit Power:
  - 6.5dBm BDR
  - 3.5dBm EDR
  - 6.5dBm BLE
- Typical Bluetooth Receive Sensitivity:
  - -91dBm, 1DH5/2DH5
  - -83dBm, 3DH5
  - -91dBm, BLE
- WLAN and Bluetooth coexistence
- Available in two footprint styles and one M.2 2230 form factor:
  - SMT Module: 15.5 mm x 21 mm
  - SiP: 12 mm x 12 mm
  - M.2 2230: 22mm x 30mm x 2.25mm
- Available with antenna trace pin, integrated chip antenna or MHF®4 connector for external antenna
- Operating voltage: VBAT 3.2V to 4.8V (3.6V typical)
- Operating temperature: -40° to +85° C
- Operating Humidity: less than 85% R.H.
- Storage temperature: -40° to +125°C
- Storage Humidity: Less than 60% R.H
- Compact design based on Infineon CYW4349_A1 SoC
- Worldwide acceptance: FCC, ISED (Canada), EU, MIC (Japan), and AS/NZS
- BT SIG QDID: D056404
- REACH and RoHS compliant

Applications

- Security and building automation
- Internet of Things/M2M connectivity
- Smart gateways

3 Module Variants

The Sterling LWB+ Module is available in three different versions. Depending on the user's antenna and footprint needs, there is a variant to suite most application requirements. Ezurio recommends that for simplicity of both the host PCB design, as well as the manufacturing process, that either the Chip Antenna or RF Connector version of the modules be used in your design.

3.1 453-00083 - Base SiP Module

This module variant is supplied in a compact, 47 pin, 0.5 mm pitch LGA footprint. Unlike the other module variants, it requires the addition of either an off-module antenna or RF connector, as well as the associated matching components. To benefit from the EMC certifications on the module, strictly following the layout in the module application guide is required. This requires adherence to the PCB stack-up and layout around the antenna. The footprint of this module may require additional care during reflow and PCB assembly.

Figure 1: Sterling LWB+ base SiP module (453-00083)

3.2 453-00084 – MHF® 4 Module

This module variant integrates the 453-00083 Base SiP Module, a MHF4 RF connector, and all associated RF matching components on a PCB. This integrated approach not only provides a MHF4 connector for connections to external antennas, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint.

Figure 2: Sterling LWB+ MHF® 4 module (453-00084)

3.3 453-00085 – Chip Antenna Module

This module variant integrates the 453-00083 Base SiP Module, a ceramic chip antenna, and all associated RF matching components on a PCB. This integrated antenna module simplifies and reduces the cost for the host integration of using the module.

Figure 3: Sterling LWB+ Chip Antenna module (453-00085)

3.4 453-00141 – Module, Sterling LWB+, M.2, Key E, SDIO, UART

This M.2 2230, E-key, SDIO/UART module variant integrates the 453-00083 Base SiP Module, a MHF4 RF connector, and all associated RF matching components on a PCB. This integrated MHF4 connector, and the M.2 2230 form factor provide an industrial standard for the host integration when using the module.

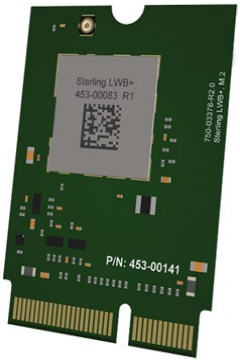


Figure 4: Sterling LWB+ M.2 2230, E-key, SDIO/UART module (453-000141)

4 Functional Description

4.1 WLAN Features

- IEEE 802.11b/g/n 1x1 2.4 GHz Radio
  - Internal Power Amplifier (PA)
  - Internal Low Noise Amplifier (LNA)
  - Internal T/R Switch
  - Simultaneous BT/WLAN reception with a single antenna
- SDIO V2.0 interface
- Media Access Controller (MAC)
- Physical Layer (PHY)
- Baseband Processor
- Standards
  - IEEE 802.11b, 802.11g, 802.11n (single stream)

4.2 Bluetooth Features

- Class 1 power amplifier with Class 1 capability
- HCI Interface using High Speed UART
- PCM for Audio Data
- High speed UART Host Controller Interface (HCI)
- Bluetooth v5.0 BR/EDR/LE

4.3 Wireless Security System Features

Supported modes:

- Open (no security)
- WEP
- WPA Personal
- WPA2 Personal
- WPA3
- WMM
- WMM-PS (U-APSD)
- WMM-SA
- WAPI
- AES (Hardware Accelerator)
- TKIP (host-computed)
- CKIP (SW Support)

5 Block Diagrams

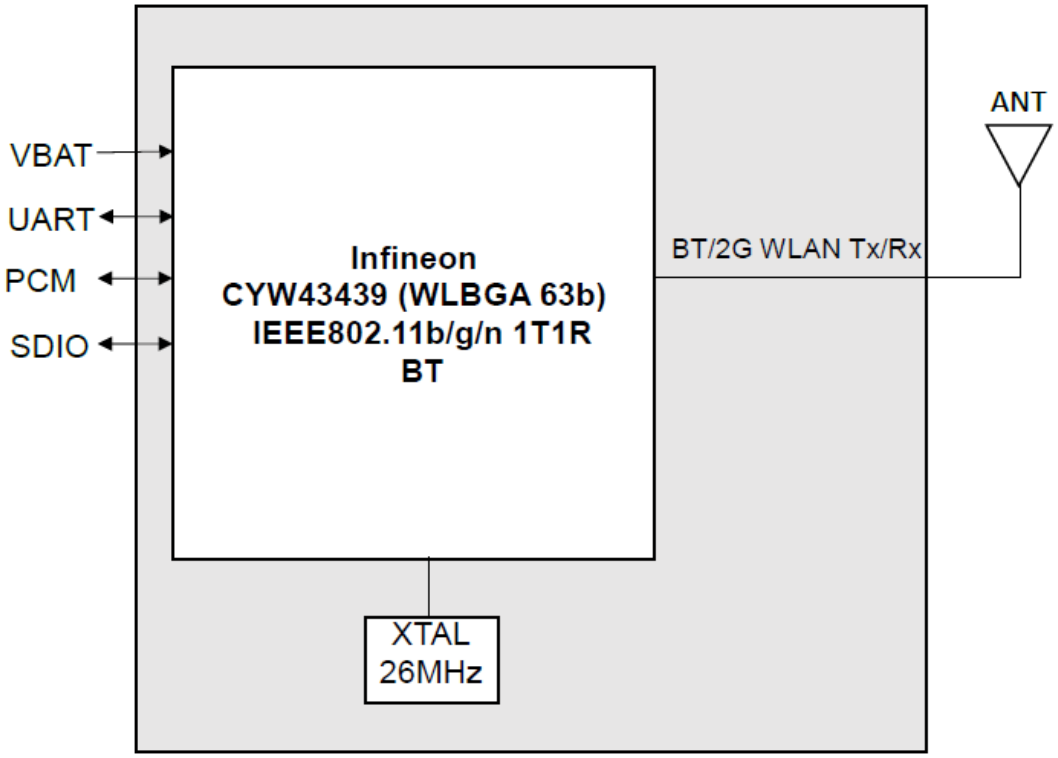


Figure 5: Sterling LWB+ base SiP module block diagram

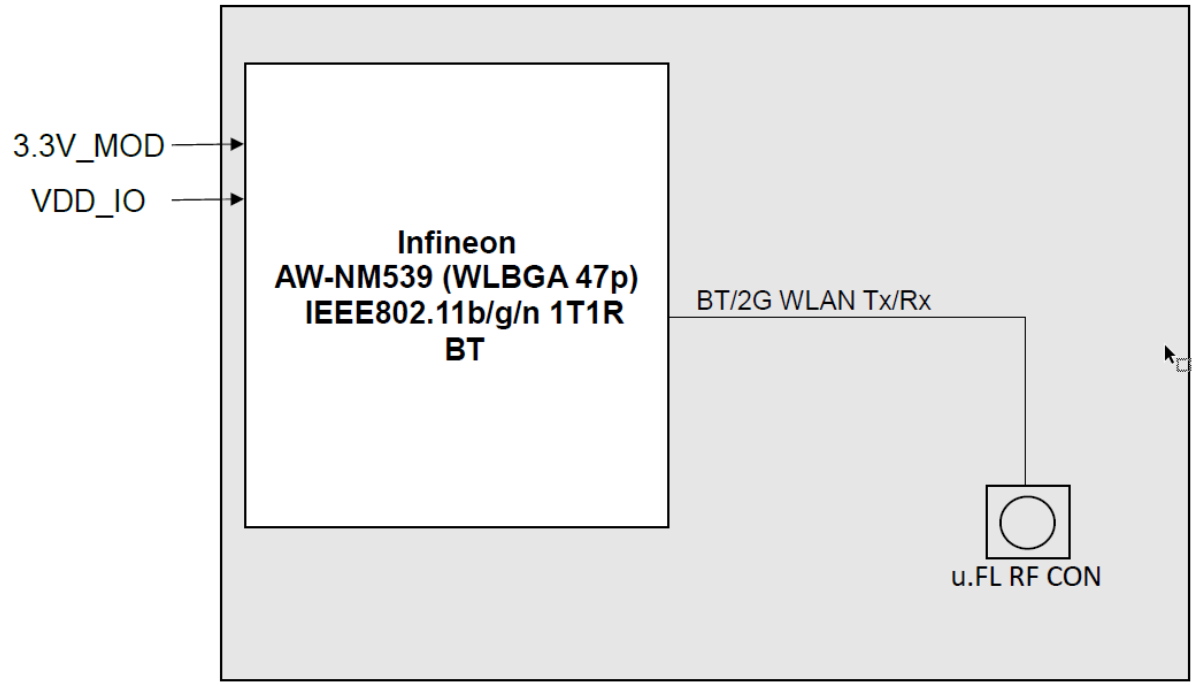


Figure 6: Sterling LWB+ MHF® 4 module block diagram

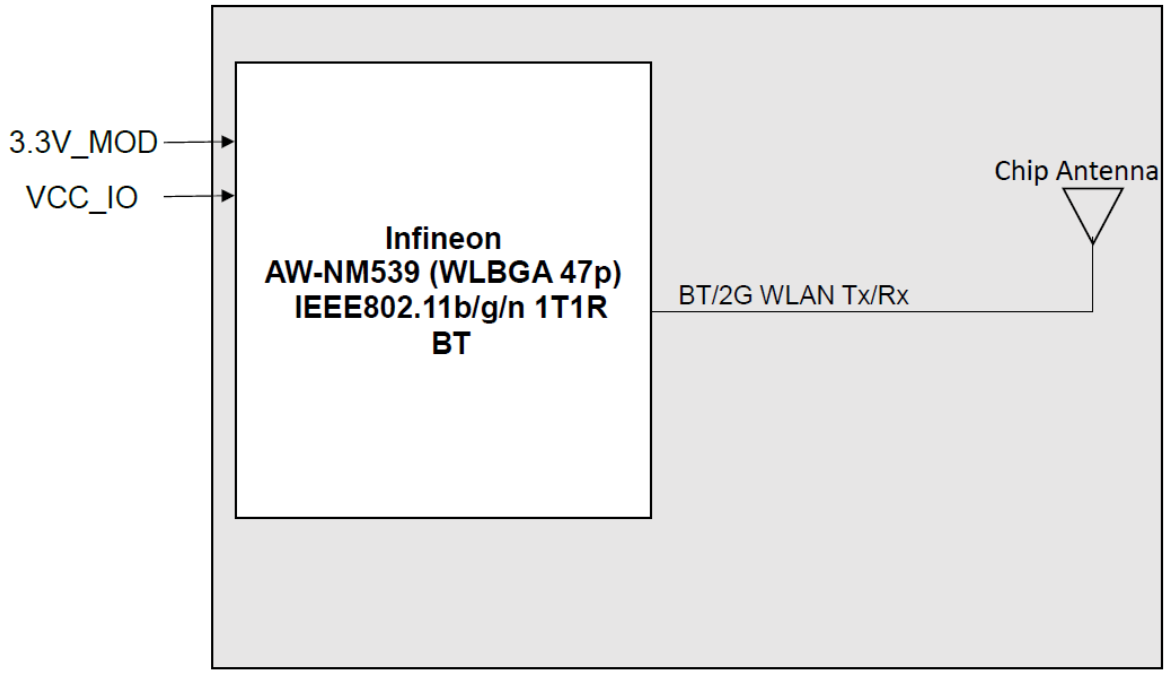


Figure 7: Sterling LWB+ chip antenna module block diagram

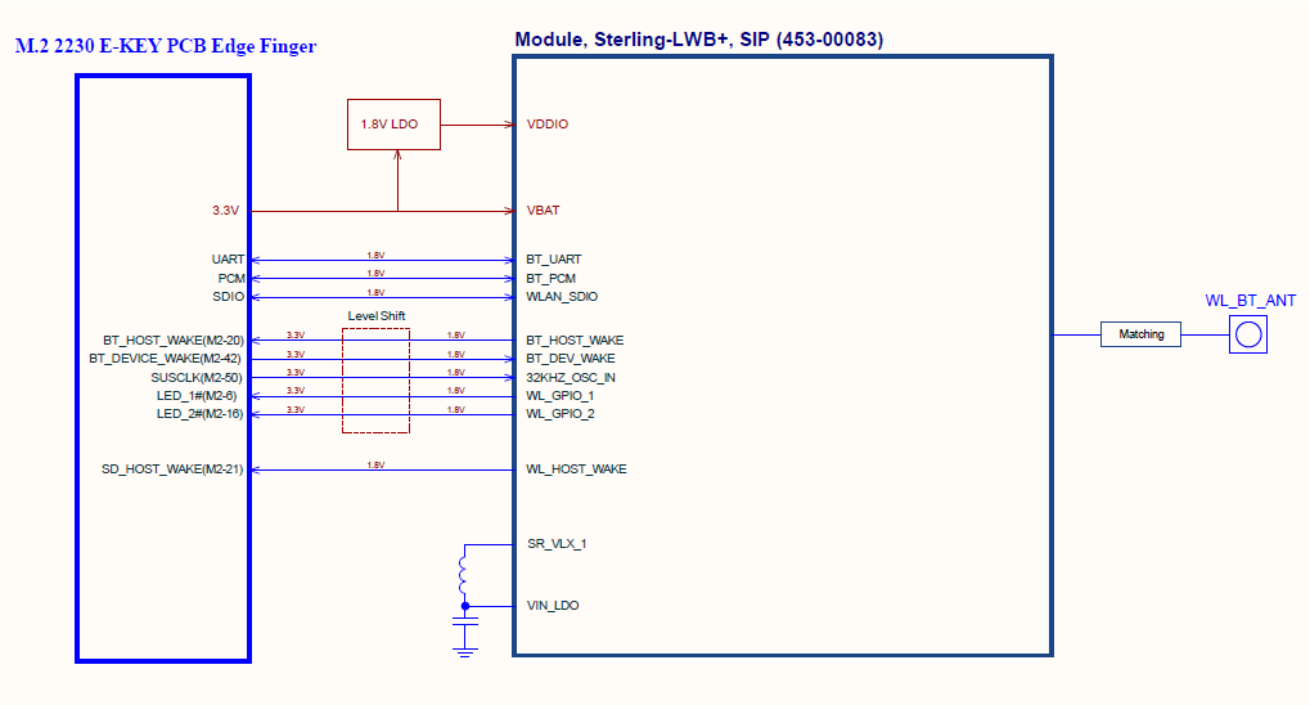


Figure 8: Sterling LWB+ M.2 2230 block diagram

6 General Characteristics

Table 1: General Characteristics

Characteristic	Description
Model Name	Sterling LWB+
Product Description	Wi-Fi and Bluetooth Wireless Module
Dimension (SiP Module)	12 mm x 12 mm x 1.5 mm (W*L*T)
Dimension (Antenna Option Module)	15.5 mm x 21 mm x 2 mm (W*L*T)
Dimension (M.2 2230 Module)	22mm x 30mm x 2.25mm (W*L*T)
Operating temperature	-40°C to 85°C
Storage temperature	-40°C to 125°C
Weight (SiP Module)	0.4g
Weight (Antenna Option Module)	1.1g
Weight (M.2 2230 Module)	3.5g

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulators	-0.5		6	V
VDDIO	DC supply voltage for digital I/O	-0.5		3.9	V

7.2 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulators	3.2*	3.6	4.8*	V

Note: *Optimal RF performance is guaranteed only for 3.2V < VBAT < 4.8V

7.3 Digital IO Pin DC Characteristics

Table 4: Digital I/O Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
For SDIO Interface VDDIO =1.8V					
VIH	Input high voltage	1.27	-	-	V
VIL	Input low voltage	-	-	0.58	V
VOH	Output High Voltage @ 2mA	1.4	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V
For SDIO Interface VDDIO =3.3V					
VIH	Input high voltage	0.625 x VDDIO	-	-	V
VIL	Input low voltage	-	-	0.25 x VDDIO	V

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VOH	Output High Voltage @ 2mA	0.75 x VDDIO	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.125 x DDIO	V
Other Digital Interface VDDIO=1.8V					
VIH	Input high voltage	0.65 x VDDIO	-	-	V
VIL	Input low voltage	-	-	0.35 x VDDIO	V
VOH	Output High Voltage @ 2mA	VDDIO – 0.45	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V
Other Digital Interface VDDIO=3.3V					
VIH	Input high voltage	2.00	-	-	V
VIL	Input low voltage	-	-	0.80	V
VOH	Output High Voltage @ 2mA	VDDIO – 0.4	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.40	V

7.4 WLAN RF Characteristics

7.4.1 WLAN RF TX Characteristics *(VBAT=3.3V, TA=25 ℃)*

Table 5: WLAN Transmitter RF Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) TX Output Power	1 Mbps BPSK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	18.0	-	dBm
11 Mbps DSSS (b) TX Output Power	11 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	18.0	-	dBm
6 Mbps OFDM (g) TX Output Power	6 Mbps BPSK 802.11(g) Mask Compliance -5 dB EVM RMS power over TX packet	-	18.0	-	dBm
54 Mbps OFDM (g) TX Output Power	54 Mbps 64-QAM 802.11(g) Mask Compliance -25 dB EVM RMS power over TX packet	-	16.0	-	dBm
MCS0 OFDM (n) TX Output Power	6.5 Mbps BPSK 802.11(n) Mask Compliance -5 dB EVM RMS power over TX packet	-	18.0	-	dBm
MCS7 OFDM (n) TX Output Power	65 Mbps 64-QAM 802.11(n) Mask Compliance -27 dB EVM RMS power over TX packet	-	15.0	-	dBm

7.4.2 WLAN RF RX Characteristics *(VBAT=3.3V, TA=25 ℃)*

Table 6: WLAN Receiver RF Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) RX Sensitivity	8% PER	-	-94	-	dBm
11 Mbps DSSS (b) RX Sensitivity	8% PER	-	-88	-	dBm
6 Mbps OFDM (g) RX Sensitivity	10% PER	-	-90	-	dBm
54 Mbps OFDM (g) RX Sensitivity	10% PER	-	-75	-	dBm
MCS0 (6.5 Mbps) OFDM (n) RX Sensitivity	10% PER	-	-89	-	dBm

Parameter	Test Conditions	Min	Typ	Max	Unit
MCS7 65 Mbps OFDM (n) RX Sensitivity	10% PER	-	-72	-	dBm
11b RX Overload Level	8% PER, 11 Mbps	-10	-	-	dBm
11g RX Overload Level	10% PER, 54 Mbps	-20	-	-	dBm
11n RX Overload Level	10% PER, MCS7	-20	-	-	dBm

7.5 Bluetooth RF Characteristics

7.5.1 Bluetooth TX RF Characteristics *(VBAT=3.3V, TA=25 ℃)*

Table 7: Bluetooth Transmitter GFSK and EDR Characteristics

Parameter	Test Conditions	Min	Typical	Max	Bluetooth Spec	Unit
GFSK RF Output Power		-	6.5	-		dBm
EDR RF Output Power		-	3.5	-		dBm
Power Control Step Size		2	4	8	2-8	dB
EDR Relative Power		-4		1	-4/+1	dB

7.5.2 Bluetooth RX RF Characteristics *(VBAT=3.3V, TA=25 ℃)*

Table 8: Bluetooth Receiver Characteristics

Parameter	Test Conditions	Min	Typical	Max	Bluetooth Spec	Unit
GFSK Sensitivity	BER=0.1%	-	-91	-	-70	dBm
EDR 2 Mbps Sensitivity	BER=0.01%	-	-91	-	-70	dBm
EDR 3 Mbps Sensitivity	BER=0.01%	-	-83	-	-70	dBm
BLE	PER = 30.8%	-	-91	-	-70	dBm

7.6 Current Consumption

7.6.1 WLAN Current consumption

Test Condition

1. All results are with the **Bluetooth off** (BT_REG_ON=LOW).
2. All results are run to **take 3 minutes** then record the test **average** and maximum value.
3. Power Save mode record 1 DTIM interval.

Table 9: Bluetooth Test conditions (VBAT = VDDIO = 3.6VDC)

No.	Item	VBAT=3.6V(mA)	
		Max	Avg.
1	Leakage (OFF) *(1)	3.9μA	
2	Sleep*(3)	8.1μA	5.5μA
3	Power Save DTIM1 (2.4GHz)*(4)(6)	27mA	1.2mA
4	Power Save DTIM3 (2.4GHz)*(5)(6)	31mA	773uA

Band (GHz)	Mode	BW (MHz)	RF Power (dBm)	Transmit		
				Max.	Avg.	Duty(%)
2.4	11b@1Mbps	20	18	303	301	96
	11g@54Mbps	20	16	194	192	49
	11n@MCS7	20	15	182	181	54

Band (GHz)	Mode	BW(MHz)	Receive	
			Max.	Avg.
2.4	11b@1Mbps	20	37	35
	11n@MCS7	20	37	34

**Transmit Option: Packet Interval=500 / Packet length=1000*

Table 10: Bluetooth Test Conditions (VDDIO = 1.8VDC)

No.	Item			VDDIO=1.8 V	
				Max	Avg.
1	Leakage (OFF)*(1)			0.08μA	
2	Sleep*(3)			94μA	86μA
3	Power Save DTIM1 (2.4GHz)*(4)(6)			158μA	79μA
Band (GHz)	**Mode**	**BW (MHz)**	**RF Power (dBm)**	**Transmit**	
				Max.	**Avg.**
2.4	11b@1Mbps*(7)	20	18	52μA	48μA
Band (GHz)	**Mode**	**BW(MHz)**		**Receive**	
				Max.	**Avg.**
2.4	11b@1Mbps*(7)	20		62μA	48μA

(1) WLAN and Bluetooth OFF (WL_REG_ON=LOW, BT_REG_ON=LOW),DUT do not connected to VUB300 and ttyUSB0.
(2) No.2~6 Load the WLAN normal driver/firmware
(3) Run command "wlfmac_x86 deepsleep 1" into sleep
(4) Associated with AP use ASUS RT-AC66U, DTIM = 1, Beacon Interval = 100ms
(5) Associated with AP use ASUS RT-AC66U, DTIM = 3, Beacon Interval = 100ms
(6) Run the following command and measured a current consumed across the DTIM
duration "wlfmac_x86 mpc 1"
"wlfmac_x86 PM 2"
"wlfmac_x86 bcntrim 9"
(7) *Host SDIO-1.8V ,JP4 #1 #2*

7.6.2 Bluetooth Current consumption

Test Condition

1. The Bluetooth is in test mode run transmit or receive with a specified output power measure current consumption.
2. All results are with the **WLAN OFF (WL_REG_ON=LOW)**
3. All results are run to **take 3 minutes** then record the test **average** and maximum value.

Table 11: Bluetooth Current Consumption

No.	Mode	Packet Type	RF Power (dBm)	VBAT=3.6 V	
				Max.	Avg.
1	Sleep	n/a	n/a	39.8μA	18μA
2	Transmit*(1)	DH5	9.3	25.3mA	25.1mA
3	Receive*(1)	3DH5	n/a	11.2mA	11.1mA
4	Transmit*(2)	LE	8.9	28.1mA	28.0mA
5	Receive	LE	n/a	12.1mA	12.1mA

(1) BlueTool BB_Packet_Length=65535
(2) BlueTool Length_of_Test_Data=37

8 Pin Definitions

8.1 Base SIP Pin Definitions

Note: PO = Power Output, PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, RF = Bi-directional RF Port, GND = Ground

Table 12: Sterling LWB+ SiP pin Description (453-00083)

Pin No.	Name	I/O Type	Voltage Domain	Basic Description
1	GND	GND		Ground
2	GND	GND		Ground
3	WL_BT_ANT	RF		WLAN/BT RF TX/RX path
4	GND	GND		Ground
5	NC	Floating		Floating Pin, No connect to anything
6	BT_WAKE_DEV	DI	VDDIO	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	DO	VDDIO	Bluetooth device to wake-up HOST
8	CLK_REQ	DO	VDDIO	External system clock request—Used when the system clock is not provided by a dedicated crystal (for example, when a shared TCXO is used). Asserted to indicate to the host that the clock is required. Shared by BT, and WLAN.
9	GND	GND		Ground
10	NC	Floating		Floating Pin, No connect to anything
11	VBAT	PI	VBAT	3.2 to 4.8V power pin
12	WL_REG_ON	DI	VDDIO	Used by PMU to power up or power downthe internal regulators used by the WLAN section. Also, when de-asserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabledthrough programming.
13	WL_ HOST_WAKE (WL_GPIO_0)	DO	VDDIO	WLAN device to wake-up HOST
14	SDIO_DATA_2 (JTAG_TDO)	DIO	VDDIO	SDIO Data Line 2
15	SDIO_DATA_3 (JTAG_TRS TN)	DIO	VDDIO	SDIO Data Line 3
16	SDIO_CMD	DIO	VDDIO	SDIO Command Input
17	SDIO_DATA_0 (JTAG_TMS)	DIO	VDDIO	SDIO Data Line 0
18	SDIO_CLK (JTAG_TCK)	DI	VDDIO	SDIO Clock Input
19	SDIO_DATA_1 (JTAG_TDI)	DIO	VDDIO	SDIO Data Line 1
20	GND	GND		Ground

Pin No.	Name	I/O Type	Voltage Domain	Basic Description
21	SR_VLX_1	PO	1.4V	Internal Buck voltage generation output pin. **Note:** An external low pass filter with inductor (0603,2.2uH +/-20%, DCR< =0.2Ω) and capacitor (Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, 4.7 µF ±20%, 10V) is needed. Keep the L-C ground return loop as smaller as possible and feed the voltage to the VIN_LDO pin with trace that rating up to 1.4A.
22	VDDIO	PWR	VDDIO	1.8V-3.3V VDDIO supply for WLAN and BT
23	VIN_LDO	PI	1.4V	Power input for internal LDO
24	32KHZ_OSC_IN	DI	0.2~3.3V	External 32K or RTC clock
25	BT_PCM_OUT	DO	VDDIO	PCM data Out
26	BT_PCM_CLK	DIO	VDDIO	PCM Clock
27	BT_PCM_IN	DI	VDDIO	PCM data Input
28	BT_PCM_SYNC	DO	VDDIO	PCM Synchronization control
29	NC	Floating		Floating Pin, No connect to anything
30	NC	Floating		Floating Pin, No connect to anything
31	GND	GND		Ground
32	NC	Floating		Floating Pin, No connect to anything
33	GND	GND		Ground
34	BT_REG_ON	DI	VDDIO	Used by PMU to power up or power downthe internal regulators used by the Bluetooth section. Also, when de-asserted, this pinholds the Bluetooth section in reset. This pin hasan internal 200k ohm pull down resistor that is enabled by default. It can be disabledthrough programming.
35	NC	Floating		Floating Pin, No connect to anything
36	GND	GND		Ground
37	NC	Floating		Floating Pin, No connect to anything
38	NC	Floating		Floating Pin, No connect to anything
39	WL_GPIO_2	DIO	VDDIO	PROGRAMMABLE GPIO PIN
40	WL_GPIO_1	DIO	VDDIO	PROGRAMMABLE GPIO PIN
41	BT_UART_TXD	DO	VDDIO	High-Speed UART Data Out
42	BT_UART_RTS_N	DO	VDDIO	High-Speed UART RTS
43	BT_UART_RXD	DI	VDDIO	High-Speed UART Data In
44	BT_UART_CTS_N	DI	VDDIO	High-Speed UART CTS
45	NC	Floating		Floating Pin, No connect to anything
46	NC	Floating		Floating Pin, No connect to anything
47	NC	Floating		Floating Pin, No connect to anything

8.2 MHF4 and Chip Antenna Module Pin Definitions

Note: PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

Table 13: Sterling LWB+ MHF® 4 (453-00084) and chip antenna (453-00085) module pin descriptions

Pin No.	Name	I/O Type	Voltage Domain	Description
1	GND	GND	GND	GROUND
2	BT_PCM_SYNC	DIO	VDD_VIO	PCM SYNC; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
3	BT_PCM_IN	DI	VDD_VIO	PCM DATA INPUT SENSING
4	BT_PCM_OUT	DO	VDD_VIO	PCM DATA OUTPUT
5	VDD_3V3	PI	VDD_VIO	WIFI AND BLUETOOTH POWER SUPPLY
6	GND	GND	GND	GROUND
7	NC	Floating	Floating	Floating Pin, No connect to anything
8	NC	Floating	Floating	Floating Pin, No connect to anything
9	WL_GPIO_2	DIO	VDD_VIO	PROGRAMMABLE GPIO PIN
10	WL_GPIO_1	DIO	VDD_VIO	PROGRAMMABLE GPIO PIN
11	WL_ HOST_WAKE (WL_GPIO_0)	DO	VDD_VIO	WLAN device to wake-up HOST
12	WL_REG_ON	DI	VDD_VIO	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE WLAN SECTION. **Note:** When de-asserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.
13	CLK_REQ	DO	VDD_VIO	External system clock request—Used when the system clock is not provided by a dedicated crystal (for example, when a shared TCXO is used). Asserted to indicate to the host that the clock is required. Shared by BT, and WLAN.
14	GND	GND	GND	GROUND
15	NC	Floating	Floating	Floating Pin, No connect to anything
16	NC	Floating	Floating	Floating Pin, No connect to anything
17	NC	Floating	Floating	Floating Pin, No connect to anything
18	GND	GND	GND	GROUND
19	32KHZ_OSC_IN	DI	VDD_VIO	EXTERNAL SLEEP CLOCK INPUT **Note:** the clock signal level is accepted from 0.2 to 3.3V
20	VDD_VIO	PI	VDD_VIO	DC SUPPLY FOR I/O Note: 1.8V or 3.3V
21	BT_REG_ON	DI	VDD_VIO	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE BLUETOOTH SECTION. **Note:** When de-asserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.
22	SDIO_D0 (JTAG_TMS)	DIO	VDD_VIO	SDIO DATA LINE 0
23	SDIO_D1	DIO	VDD_VIO	SDIO DATA LINE 1

Pin No.	Name	I/O Type	Voltage Domain	Description
	(JTAG_TDI)			
24	GND	GND	GND	GROUND
25	SDIO_D2 (JTAG_TDO)	DIO	VDD_VIO	SDIO DATA LINE 2
26	SDIO_CMD	DIO	VDD_VIO	SDIO COMMAND LINE
27	SDIO_D3 (JTAG_TRSTN)	DIO	VDD_VIO	SDIO DATA LINE 3
28	GND	GND	GND	GROUND
29	SDIO_CLK (JTAG_TCK)	DIO	VDD_VIO	SDIO CLOCK LINE
30	GND	GND	GND	GROUND
31	BT_UART_RTS_L	DO	VDD_VIO	BT UART REQUEST-TO-SEND
32	BT_UART_CTS_L	DI	VDD_VIO	BT UART CLEAR-TO-SEND
33	BT_UART_TXD	DO	VDD_VIO	BT UART TRANSMIT OUTPUT
34	BT_UART_RXD	DI	VDD_VIO	BT UART RECEIVE INPUT
35	NC	Floating	Floating	Floating Pin, No connect to anything
36	NC	Floating	Floating	Floating Pin, No connect to anything
37	NC	Floating	Floating	Floating Pin, No connect to anything
38	BT_PCM_CLK	DIO	VDD_VIO	PCM CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
39	BT_DEV_WAKE	DI	VDD_VIO	DEV_WAKE OR GENERAL-PURPOSE I/O SIGNAL
40	BT_HOST_WAKE	DO	VDD_VIO	HOST_WAKE OR GENERAL-PURPOSE I/O SIGNAL
41	GND	GND	GND	GROUND
42	GND	GND	GND	GROUND
43	GND	GND	GND	GROUND
44	GND	GND	GND	GROUND
45	GND	GND	GND	GROUND
46	GND	GND	GND	GROUND
47	GND	GND	GND	GROUND

8.3 M.2 2230, E-key, SDIO/UART module Pin Definitions

Note: PO = Power Output, PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, RF = Bi-directional RF Port, GND = Ground

Table 14: Sterling LWB+ M.2 2230, E-key, SDIO/UART pin Description (453-00141)

Pin No.	Name	Type	Voltage Ref.	Function	If Not Used
1	GND	-	-	Ground	GND
2	3.3V	PI	3.3V	DC supply voltage for module.	--
3	USB_D+	DIO	-	NC	NC
4	3.3V	PI	3.3V	DC supply voltage for module.	--

Pin No.	Name	Type	Voltage Ref.	Function	If Not Used
5	USB_D-	DIO	-	NC	NC
6	LED1#	DO	3.3V	NC	NC
7	GND	-	-	Ground	GND
8	PCM_CLK	DIO	1.8V	PCM clock. Can be master (Output) or slave (Input)	NC
9	SDIO CLK	DI	1.8V	SDIO clock input	NC
10	PCM_SYNC	DIO	1.8V	PCM Sync. Can be master (Output) or slave (Input); Or SLIM bus data.	NC
11	SDIO CMD	DIO	1.8V	SDIO command line	NC
12	PCM_OUT	DO	1.8V	PCM data output.	NC
13	SDIO DATA0	DIO	1.8V	SDIO data lin0	NC
14	PCM_IN	DI	1.8V	PCM data input.	NC
15	SDIO DATA1	DIO	1.8V	SDIO data lin1	NC
16	LED2#	DO	3.3V	NC	NC
17	SDIO DATA2	DIO	1.8V	SDIO data lin2	NC
18	GND	-	-	Ground	GND
19	SDIO DATA3	DIO	1.8V	SDIO data lin3	NC
20	UART WAKE#	DO	3.3V	Reserved for BT_HOST_WAKE. Output signal to wake up Host.	NC
21	SDIO WAKE#	DO	1.8V	Reserved for feature support Reserved for WL_HOST_WAKE. Output signal to wake up host.	NC
22	UART_TXD	DO	1.8V	Serial data output for the HCI UART interface.	NC
23	SDIO RESET#	DI	1.8V	NC	NC
32	UART_RXD	D	1.8V	Serial data input for the HCI UART interface.	NC
33	GND	-	-	Ground	GND
34	UART_RTS	DO	1.8V	Active-Low request-to-send signal for the HCI UART interface.	NC
35	PERp0	-	-	NC	NC
36	UART_CTS	DI	1.8V	Active-Low clear-to-send signal for the HCI UART interface.	NC
37	PERn0	-	-	NC	NC
38	VENDER DEFINED38	-	-	NC	NC
39	GND	-	-	Ground	GND
40	VENDER DEFINED40	DI	3.3V	Reserved for feature support BT_DEVICE_WAKE. Input signal from Host.	NC
41	PETp0	-	-	No connection for this module	NC
42	VENDER DEFINED42	DI	3.3V	Reserved for feature support Reserved for WL_DEVICE_WAKE. Input from Host to wake up WLAN module.	NC
43	PETn0	-	-	NC	NC
44	COEX3	-	-	NC	NC

Pin No.	Name	Type	Voltage Ref.	Function	If Not Used
45	GND	-	-	Ground	GND
46	COEX2	DIO	1.8V	NC	NC
47	REFCLKp0	-	-	NC	NC
48	COEX1	DIO	1.8V	GPIO 2	NC
49	REFCLKn0	-	-	NC	NC
50	SUSCLK	DI	-	EXTERNAL SLEEP CLOCK INPUT Note: the clock signal level is accepted from 0.2 to 3.3V	--
51	GND	-	-	Ground	GND
52	PERST0#	-	-	NC	NC
53	CLKREQ0#	-	-	NC	NC
54	W_DISABLE2#	DI	3.3V	Enables BT regulators (BT_REG_ON). Internal 10K pull-up to enable BT by default. Ground to disable BT.	NC
55	PEWAKE0#	-	-	NC	NC
56	W_DISABLE1#	DI	3.3 V	Enables WLAN regulators (WL_REG_ON). Internal 10K pull-up to enable WLAN by default. Ground to disable WLAN.	NC
57	GND	-	-	Ground	GND
58	I2C DATA	-	-	NC	NC
59	RESERVED	-	-	NC	NC
60	I2C CLK	-	-	NC	NC
61	RESERVED	-	-	NC	NC
62	ALERT#	-	-	NC	NC
63	GND	-	-	Ground	GND
64	RESERVED	-	-	NC	NC
65	RESERVED	-	-	NC	NC
66	UIM_SWP	-	-	NC	NC
67	RESERVED	-	-	NC	NC
68	UIM_POWER_SNK	-	-	NC	NC
69	GND	-	-	Ground	GND
70	UIM_POWER_SRC	-	-	NC	NC
71	RESERVED	-	-	NC	NC
72	3.3V	PI	3.3V	DC supply voltage for module.	--
73	RESERVED	-	-	NC	NC
74	3.3V	PI	3.3V	DC supply voltage for module.	--
75	GND	-	-	Ground	GND

9 Power States

9.1 Module Power States

The Sterling-LWB+ WLAN power states are described as follows:

- **Active mode** – All WLAN blocks in the Sterling LWB+ powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- **Doze mode** – The radio, analog domains, and most of the linear regulators are powered down. The rest of the LWB+ remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- **Deep-sleep mode** – Most of the chip, including analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved to retention memory in the always-on domain before the digital core is powered off. To avoid lengthy hardware re-initialization, the logic states in the digital core are restored to their pre-deep-sleep settings when a wake-up event is triggered by an external interrupt, a host resume through the SDIO bus, or by the PMU timers.
- **Power-down mode** –The LWB+ effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators

9.2 MHF® 4 and Chip Antenna Module Pin I/O States

Table 15: Sterling LWB+ MHF4 and Chip Antenna Module Pin I/O States

Pin No.	Name	Keeper (b)	Active Mode	Low Power State/Sleep *(All Power Present)*	Power Down(c) WL_REG_ON =0 BT_REG_ON = 0	Out of Reset: (VDD_VIO is present)		
						WL_REG_ON=1 BT_REG_ON= any	WL_REG_ON =1 BT_REG_ ON = 0	WL_REG_ON =0 BT_REG_ON = 1
2	BT_PCM_SYNC	Y	Input No Pull (d)	Input No Pull (d)	High –Z No Pull	-	Input,PD	Input,PD
3	BT_PCM_I N	Y	Input No Pull (d)	Input No Pull (d)	High –Z No Pull	-	Input,PD	Input,PD
4	BT_PCM_ OUT	Y	Input No Pull (d)	Input No Pull (d)	High –Z No Pull	-	Input,PD	Input,PD
7	WIFI_GPIO_4	Y	TBD	Active Mode	High –Z No Pull (f)	Input,GCI GPIO[1] PU	Active Mode	Input,PU
8	WIFI_GPIO_3	Y	TBD	Active Mode	High –Z No Pull (f)	Input,GCI GPIO[0] PU	Active Mode	Input,PU
9	WIFI_GPIO_2	Y	TBD	Active Mode	High –Z No Pull (f)	Input,GCI GPIO[7] NoPull	Active Mode	Input, Strap, NoPull
10	WIFI_GPIO_1	Y	TBD	Active Mode	High –Z No Pull (f)	Input,PD	Active Mode	Input, Strap, PD
11	WIFI_GPIO_0	Y	TBD	Active Mode	High –Z No Pull (f)	Input,SDIO OOB Int. NoPull	Active Mode	Input,NoPull
12	WL_REG_ ON	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (200K)	Input; PD (200K)	-
13	CLK_REQ	Y	Open drain or push-pull (Active high)	Open drain or push-pull (Active high)	PD	Open drain, (Active high)	Open drain, (Active high)	Open drain, (Active high)
21	BT_REG_ ON	N	Input; PD (pull-down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (200K)	Input; PD (200K)	Input; PD (200K)
22	SDIO_D0	N	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE -> Pull UP	SDIO MODE > No Pull	Input,PU
23	SDIO_D1	N	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE -> Pull UP	SDIO MODE > No Pull	Input,PU
25	SDIO_D2	N	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE -> Pull UP	SDIO MODE > No Pull	Input,PU
26	SDIO_CMD	N	SDIO MODE -> No Pull	SDIO MODE -> No Pull	SDIO MODE -> No Pull	SDIO MODE ->Pull UP	SDIO MODE ->	Input,PU

Pin No.	Name	Keeper (b)	Active Mode	Low Power State/Sleep *(All Power Present)*	Power Down(c) WL_REG_ ON =0 BT_REG_O N = 0	Out of Reset: (VDD_VIO is present)		
						WL_REG_ON=1 BT_REG_ON= any	WL_REG_ ON =1 BT_REG_ ON = 0	WL_REG_O N =0 BT_REG_O N = 1
							No Pull	
27	SDIO_D3	N	SDIO MODE › No Pull	SDIO MODE › No Pull	SDIO MODE › No Pull	SDIO MODE - › Pull UP	SDIO MODE › No Pull	Input,PU
29	SDIO_CLK	N	SDIO MODE › No Pull	SDIO MODE › No Pull	SDIO MODE › No Pull	SDIO MODE - › No Pull	SDIO MODE › No Pull	Input
31	BT_UART_ RTS_L	Y	Output: No Pull	Output: No Pull	High-Z, No Pull	-	Input: PU	Output: NoPull
32	BT_UART_ CTS_L	Y	Input: NoPull	Input: No Pull	High- Z,No Pull	-	Input: PU	Input: NoPull
33	BT_UART_ TXD	Y	Output: No Pull	Output: No Pull	High- Z,No Pull	-	Input: PU	Output: NoPull
34	BT_UART_ RXD	Y	Input:PU	Input: No Pull	High- Z,No Pull	-	Input: PU	Input: NoPull
35	BT_I2S_CL K	Y	Input: No Pull (e)	Input: No Pull (e)	High-Z, No Pull	-	Input, PD	Output: Drive Low
36	BT_I2S_D0	Y	Input: No Pull (e)	Input: No Pull (e)	High-Z, No Pull	-	Input, PD	Input, PD
37	BT_I2S_W S	Y	Input: No Pull (e)	Input: No Pull (e)	High-Z, No Pull	-	Input, PD	Input, PD
38	BT_PCM_ CLK	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull	-	Input, PD	Input, PD
39	BT_DEV_ WAKE	Y	I/O: PU,PD, No Pull (Programmable)	I/O: PU,PD, No Pull (Programmable)	High-Z, No Pull	-	Input, PD	Input, PD
40	BT_HOST_ WAKE	Y	I/O: PU,PD, No Pull (Programmable)	I/O: PU,PD, No Pull (Programmable)	High-Z, No Pull	-	Input, PD	Output, Drive Low

The following notations are used:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- No Pull = Neither pulled up nor pulled down

Notes:

1. PU = pulled up, PD = pulled down.
2. N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in the power-down state. If there is no keeper, and it is an input and there is NoPull, then the pad should be driven to prevent leakage due to floating pad, for example, SDIO_CLK.
3. In the Power-down state (xx_REG_ON = 0): High-Z; NoPull =› The pad is disabled because power is notsupplied.
4. Depending on whether the PCM interface is enabled and the configuration is master or slave mode, it can be either an output or input.
5. Depending on whether the I2S interface is enabled, and configuration is master or slave mode, it can be either an input or output.
6. The GPIO pull states for the active and low-power states are hardware defaults. They can all be subsequently programmed as a pull-up or pull-down.
7. Strap state enables Serial Wire Debugging.

10 Crystal Oscillator Requirement

Table 16: Crystal Oscillator Specification

32.768 KHz Oscillator	
Frequency Accuracy	200 ppm
Duty Cycle	30% – 70%
Input Signal Amplitude	200-3300 mV, peak-peak
Signal Type	Square or Sine Wave
Clock Jitter	<10,000 ppm

IMPORTANT: A 32.768 KHz crystal is required for the module to be functional. The module will not boot without this crystal.

11 Power-On Signal Timing Diagrams

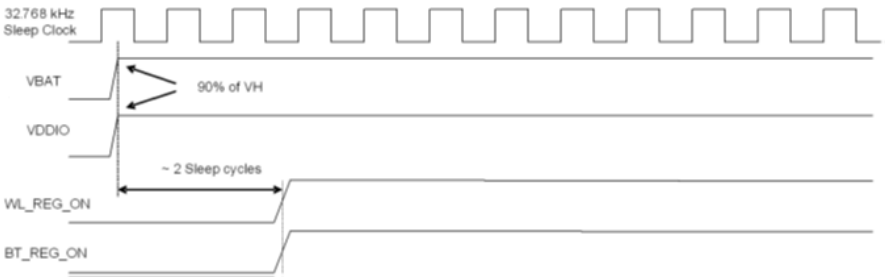


Figure 9: WLAN = ON, Bluetooth = ON

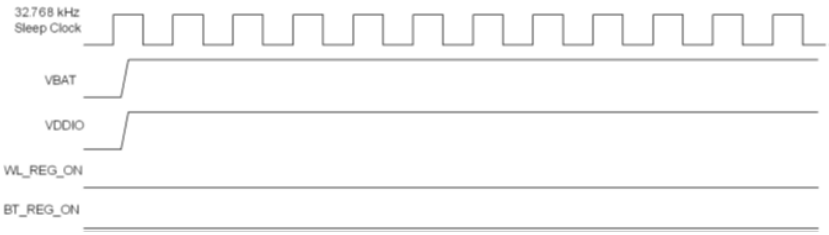


Figure 10: WLAN = OFF, Bluetooth = OFF

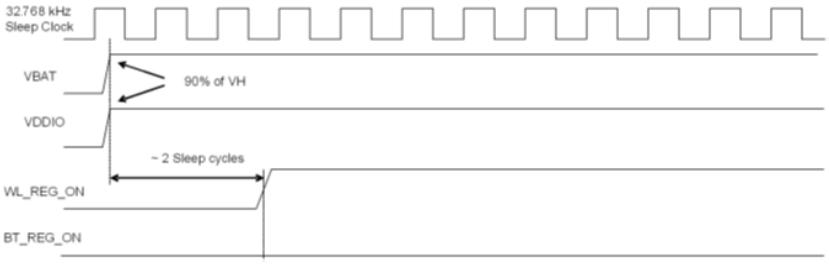


Figure 11: WLAN = ON, Bluetooth = OFF

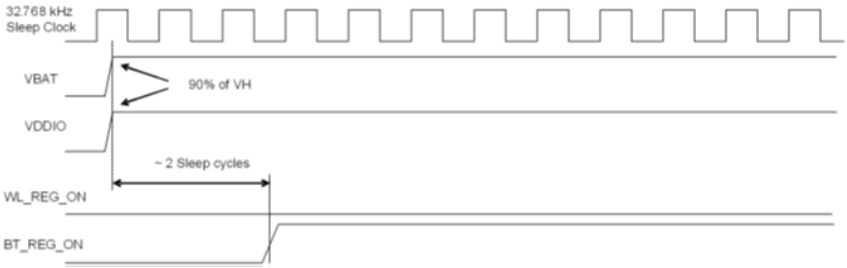


Figure 12: WLAN = OFF, Bluetooth = ON

Note: For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10ms time delay between consecutive toggles (where both signals have been driven low). This allows time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

12 Host Interface

12.1 WLAN SDIO interface

The Sterling LWB+ module WLAN section supports SDIO version 2.0. for both 1-bit (25 Mbps) and 4-bit modes (100 Mbps), as well as high speed 4-bit mode (50 MHz clocks—200 Mbps).

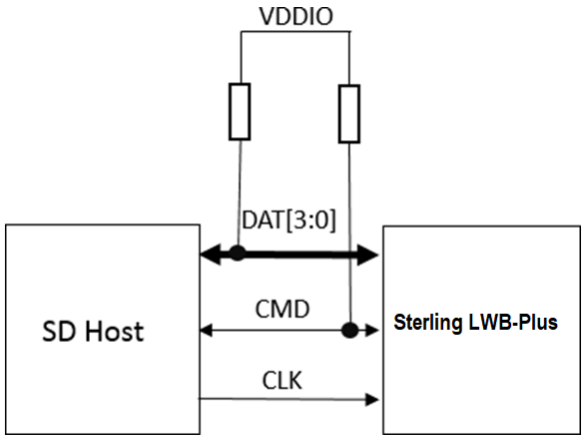


Figure 13: Signal connections to SDIO host (SD 4-bit mode)

Note: Pull-ups (10K to 100K) are required on data and CMD lines. This is required during all operating states by either external resistors or through pull-ups on the host device.

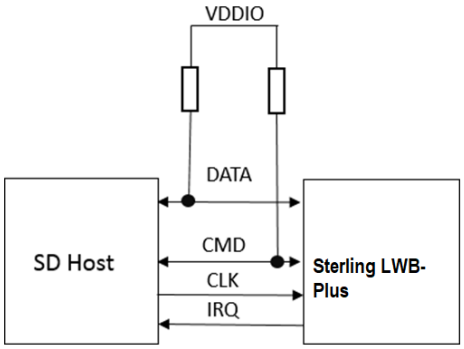


Figure 14: Signal connections to SDIO host (SD 1-bit mode)

Note: Pull-ups (10K to 100K) are required on data and CMD lines. This is required during all operating states by either external resistors or through pull-ups on the host device.

12.2 Bluetooth UART interface

The Sterling LWB+ uses a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. The baud rate may be selected through a vendor specific UART HCI command to a value other than the default rate of 115.2 kbps.

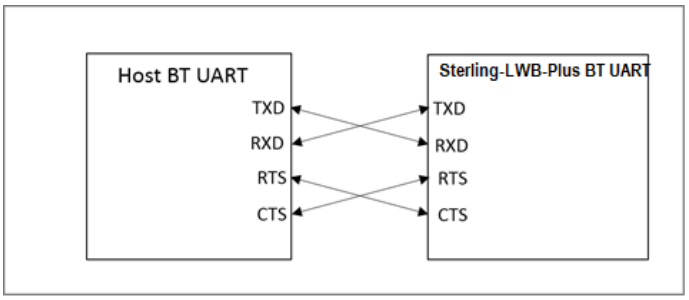


Figure 15: UART connection from Sterling-LWB to host

13 Mechanical Specifications

13.1 Base SIP Module Footprint

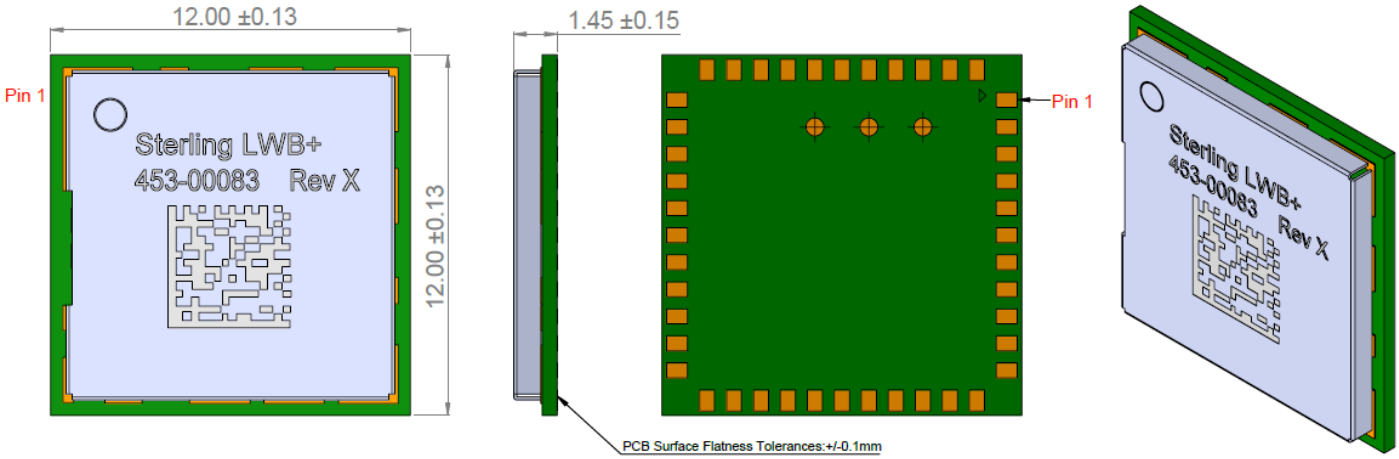


Figure 16: Sterling LWB+ base SiP module dimension

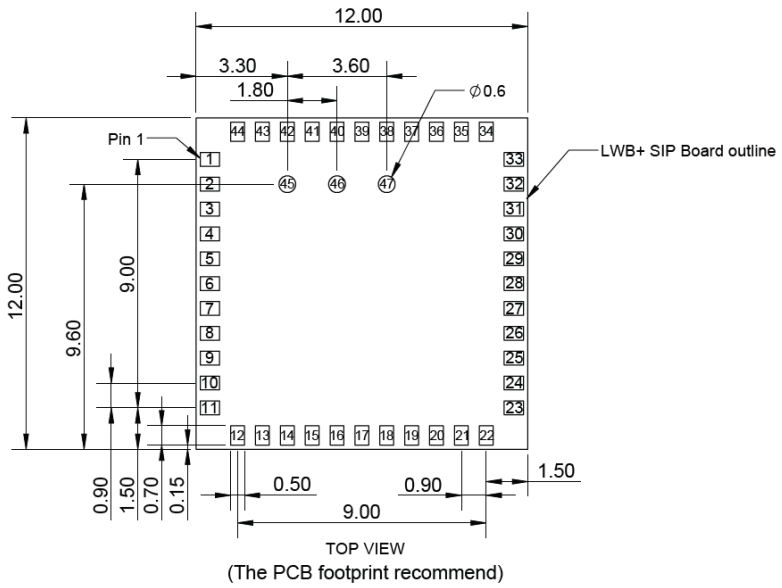


Figure 17: Sterling LWB+ base SiP module pinout (top view)

13.2 MHF4 and Chip Antenna module footprint

Note that the following footprint and pin definitions apply to the Sterling LWB+ MHF4 and Chip Antenna variants of the module (453-00084). There are two module footprints depending on which variant of the module is being used, so it is important to make certain you are using the correct version on your design.

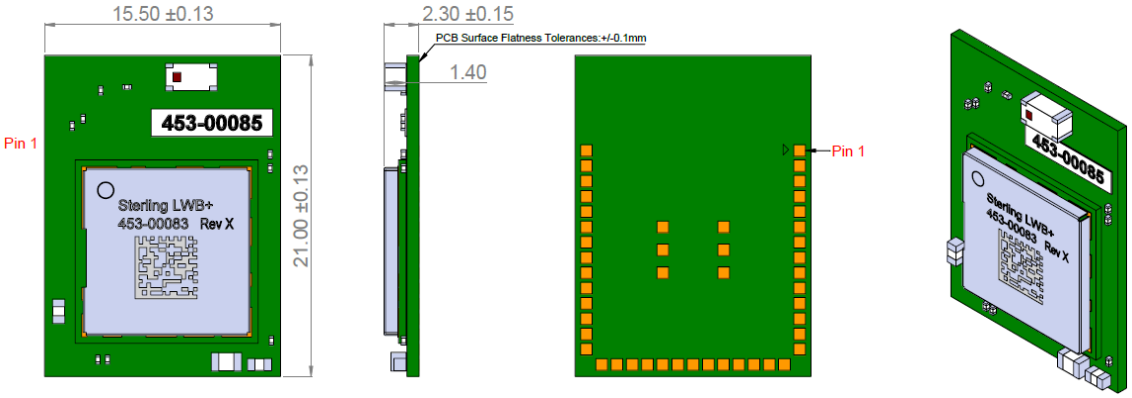


Figure 18: Sterling LWB+ MHF4 and chip antenna module dimension

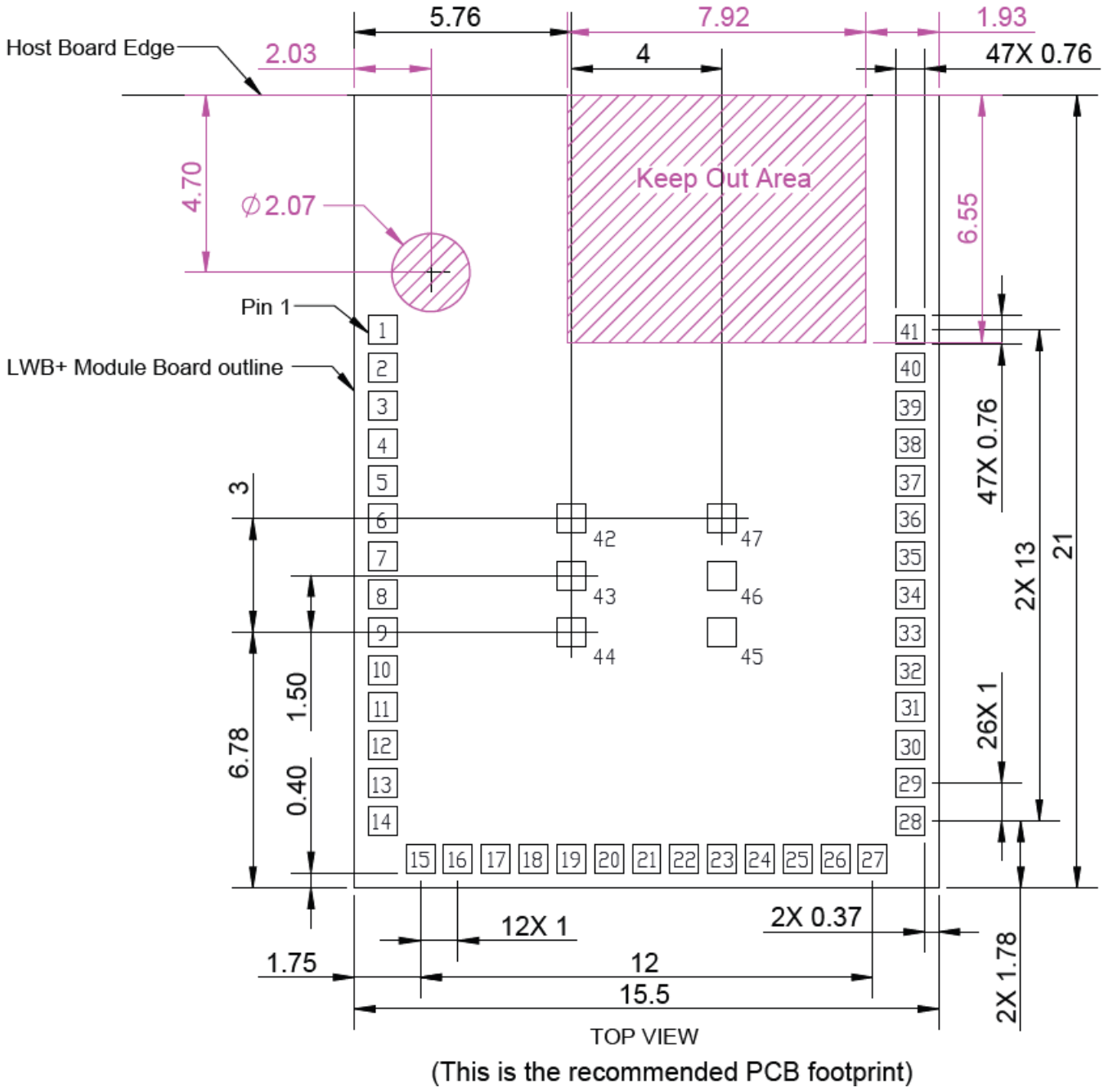


Figure 19: Sterling LWB+ MHF4 and chip antenna module pinout (top view)

13.3 M.2 2230, E-key, SDIO/UART module drawing.

The following drawing shows the dimension of the M.2 2230, E-key, SDIO/UART module variant.

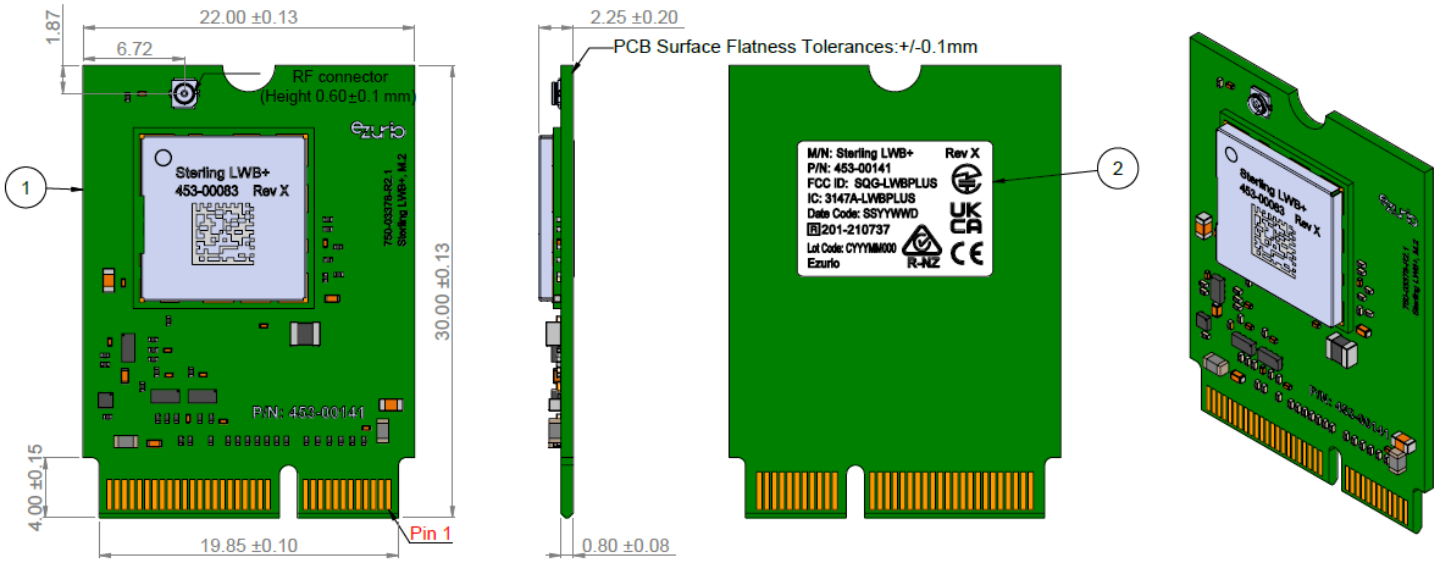


Figure 20: Sterling LWB+ M.2 2230, E-key, SDIO/UART module dimension

14 Application Note for Surface Mount Modules

14.1 Introduction

Ezurio's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

Sterling LWB+ part numbers – 453-00083R are shipped as Tape / Reel, with a reel containing 1,500 pcs. 453-00084R and 453-00085R are shipped as Tape / Reel, with a reel containing 800 pcs.

14.2 Module Packaging Configuration

14.2.1 SIP Module (453-00083)

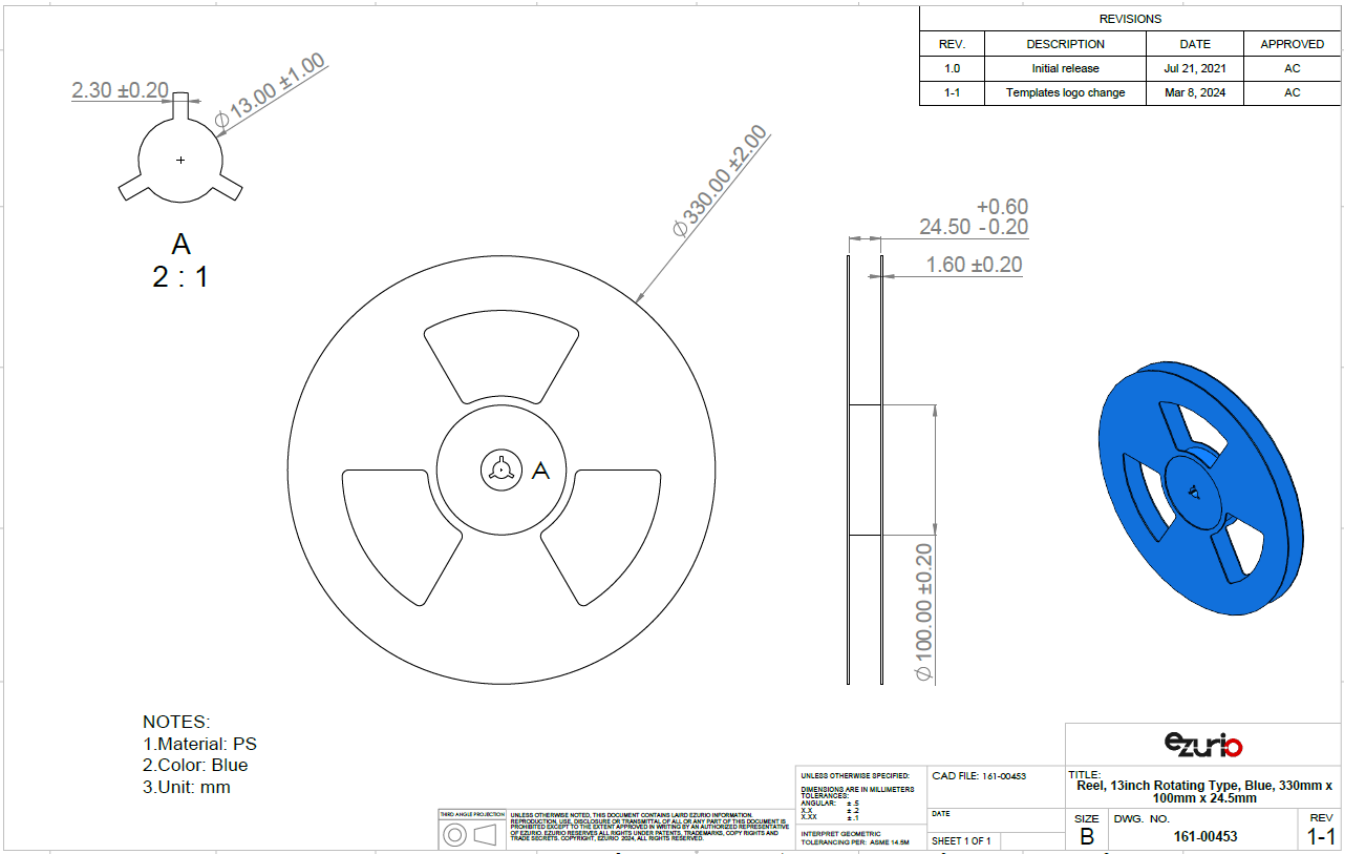
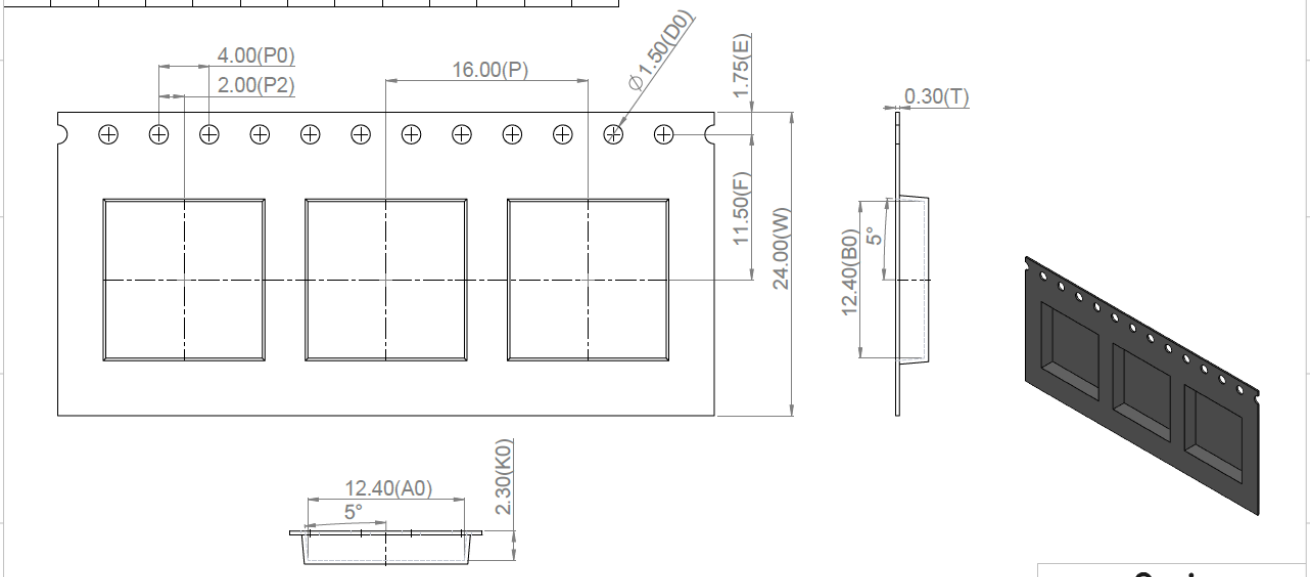


Figure 20: Reel specifications – SIP, 1,500 pieces per Reel

ITRM	W	A0	B0	K0	P	F	E	D0	P0	10P0	P2	T
DIM	24	12.40	12.40	2.30	16	11.50	1.75	1.50	4.00	40.00	2.00	0.30
TOLE	+0.30 -0.30	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.00	+0.10 -0.10	+0.20 -0.20	+0.10 -0.10	+0.05 -0.05

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1.0	Initial release	Jul 19, 2021	AC
1-1	Templates logo change	Mar 8, 2024	AC



NOTES:
1.Material: Conductive polystyrene, Black
2.The number of meters per package:25.6M
3.Unit: mm

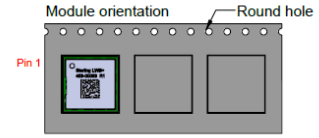
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS TOLERANCES: ANGULAR: ± 5 X.X ± .2 X.XX ± .1 INTERPRET GEOMETRIC TOLERANCING PER: ASME Y14.5M
CAD FILE: 161-00449
DATE
SHEET 1 OF 1

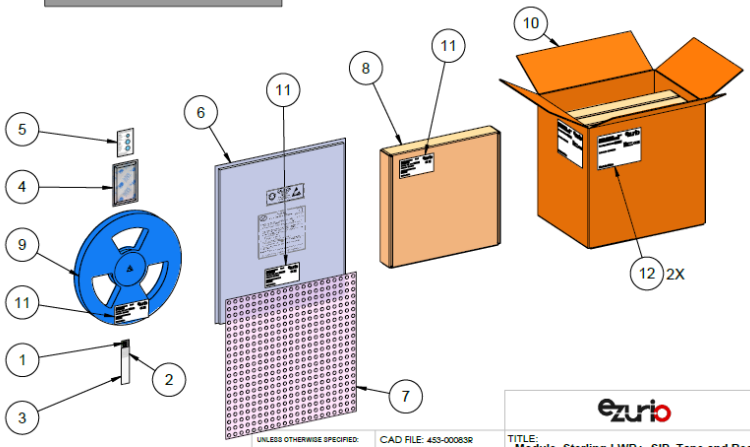
TITLE: Carrier Tape, Conductive Polystyrene, Black, 12.4mm x 12.4mm x 2.3mm
SIZE B | DWG. NO. 161-00449 | REV 1-1

Figure 21: Carrier Tape specifications for SIP

ITEM NO.	PART NUMBER	REV.	DESCRIPTION	QTY.
1	453-00083	1-1	Module, Sterling-LWB+, SIP	1500
2	161-00449	1-1	Carrier Tape, Conductive Polystyrene, Black, 12.4mm x 12.4mm x 2.3mm	1
3	161-00450	1-1	Cover Tape, Anti-static Polyester, 21.3mm x 0.05mm	1
4	161-00438	1-1	Desiccant, Silica Gel, 56g, 125mm x 80mm	1
5	161-00236	1-1	Card, Humidity Indicator, Minimum 60% RH Spot, Three Spot Indication	1
6	161-00522	1-1	Bag, ESD and Moisture Barrier, Silver, MSL4, 465mm x 400mm x 0.15mm	1
7	161-00436	1-1	Bag, ESD Barrier, Bubble, Pink, 420mm x 420mm	1
8	161-00452	1-1	Box, Single-Wall Corrugated B Flute, 355mm x 335mm x 51mm	1
9	161-00453	1-1	Reel, 13inch Rotating Type, Blue, 330mm x 100mm x 24.5mm	1
10	161-00454	1-1	Carton, Double-Wall, AB Flute, 373mm x 285mm x 360mm	1
11	160-02209	1-2	Label, Product Identifier, Sterling LWB+ SIP, 110mm x 55mm	3
12	160-02210	1-3	Label, Carton Product Identifier, Sterling LWB+ SIP, 101mm x 140mm	2

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1.0	Initial release	Jul 22, 2021	AC
1.1	Update Sterling LWB+ Top Level Parts to Remove 5GHz CE Pictogram	Sep 15, 2021	AC
1.2	ESD bag added MSL4 print	Feb 21, 2022	AC
1-3	Templates logo change	Mar 8, 2024	AC





Notes:
1.Put the Module in the carrier tape and cover the tape.
2.Put the Reel, Desiccant and Humidity Indicator Card in the ESD bag.
3.Put the packed ESD bag (vacuum) and Bubble bag in the box.
4.Put four boxes in the carton.
5.Module packaging quantity:
Per Reel: 1500 PCS
Per Carton: 6000 PCS

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS TOLERANCES: ANGULAR: ± – X.X ± – X.XX ± – INTERPRET GEOMETRIC TOLERANCING PER: ASME Y14.5M
CAD FILE: 453-00083R
DATE
SHEET 1 OF 1

TITLE: Module, Sterling-LWB+, SIP, Tape and Reel
SIZE B | DWG. NO. 453-00083R | REV 1-3

Figure 22: Sterling LWB+ Packaging Process for SIP

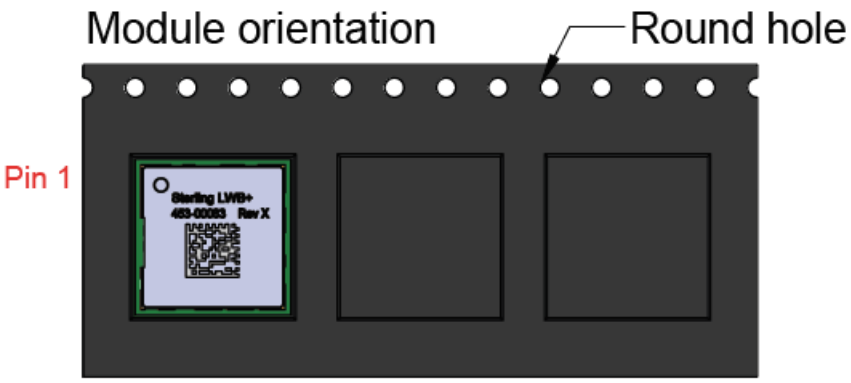


Figure 23: Module Orientation in Carrier Tape Pocket › SIP 453-00083

14.2.2 Module (453-00084 and 453-00085)

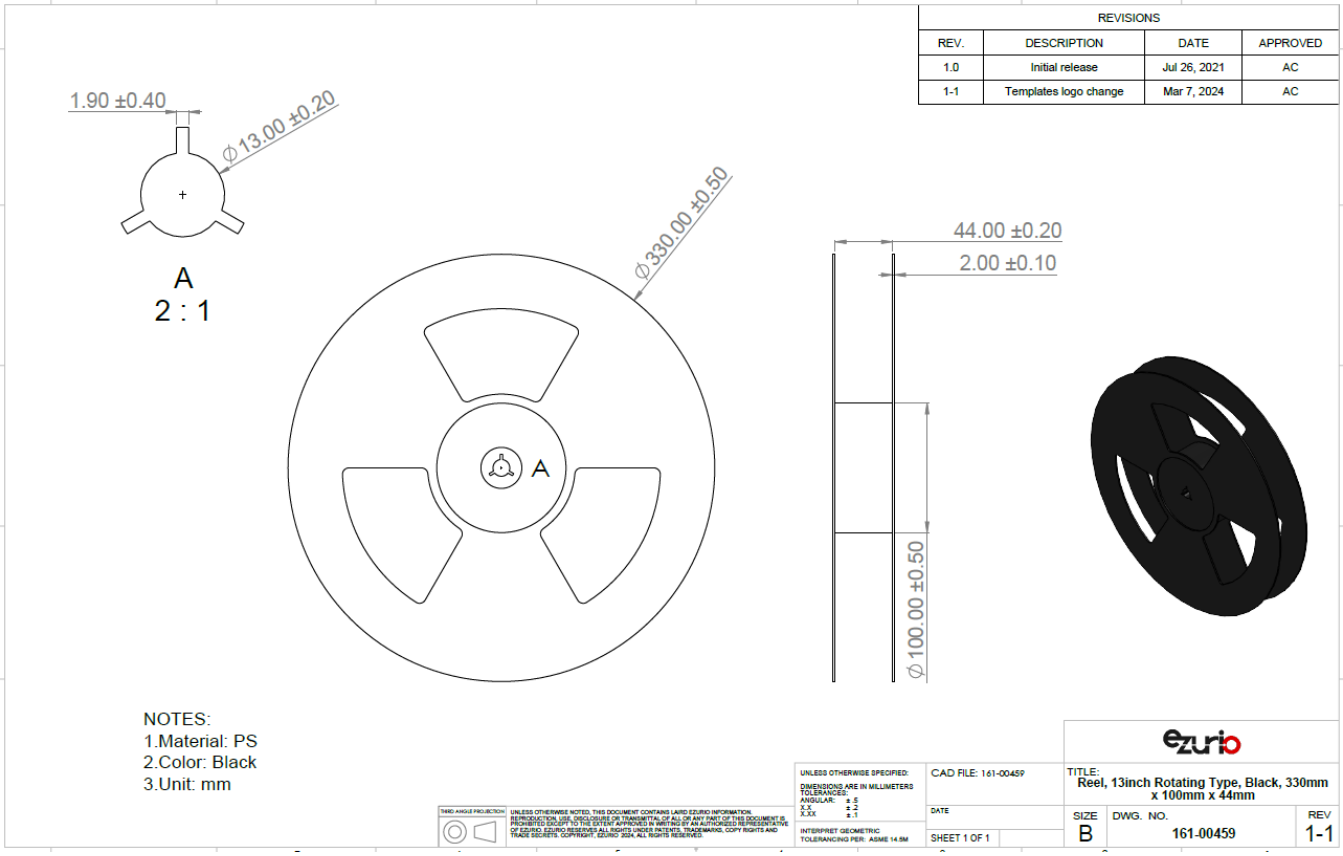
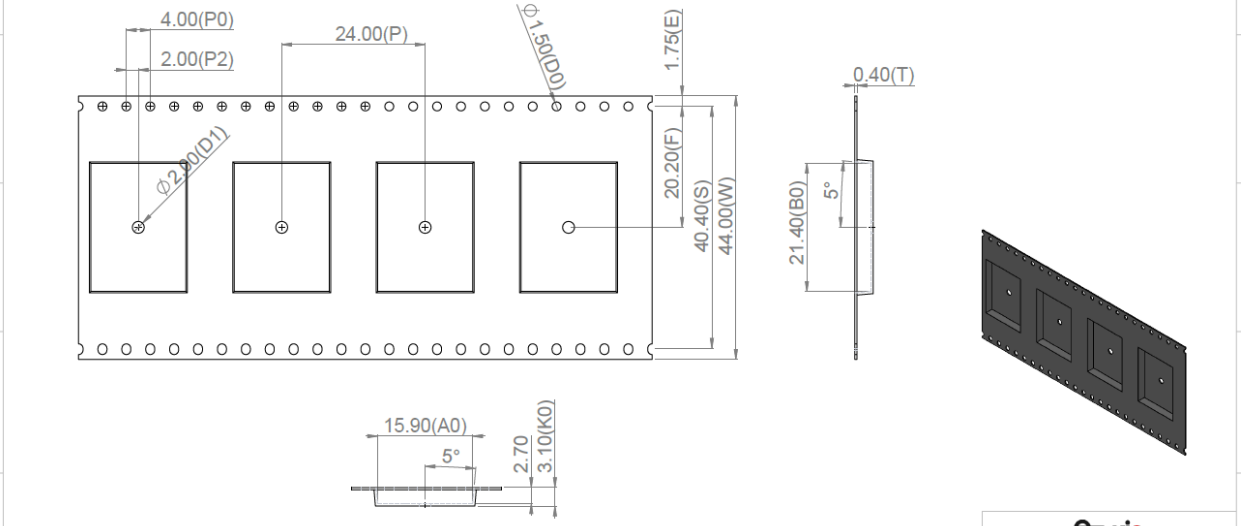


Figure 24: Reel specifications – Module, 800 pieces per Reel

ITRM	W	A0	B0	K0	P	F	E	D0	D1	P0	10P0	P2	T	S
DIM	44	15.90	21.40	3.10	24	20.20	1.75	1.50	2.00	4.00	40.00	2.00	0.4	40.40
TOLE	+0.30 -0.30	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.10 -0.10	+0.15 -0.15	+0.10 -0.10	+0.10 -0.00	+0.10 -0.00	+0.10 -0.10	+0.20 -0.20	+0.15 -0.15	+0.05 -0.05	+0.10 -0.10

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1.0	Initial release	Jul 26, 2021	AC
1-1	Drawing Templates logo change	Mar 7, 2024	AC



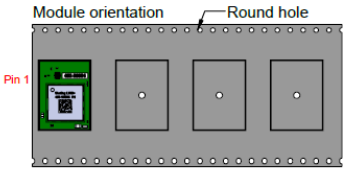
NOTES:
1.Material: Conductive polystyrene, Black
2.The number of meters per package:19.2M
3.Unit: mm

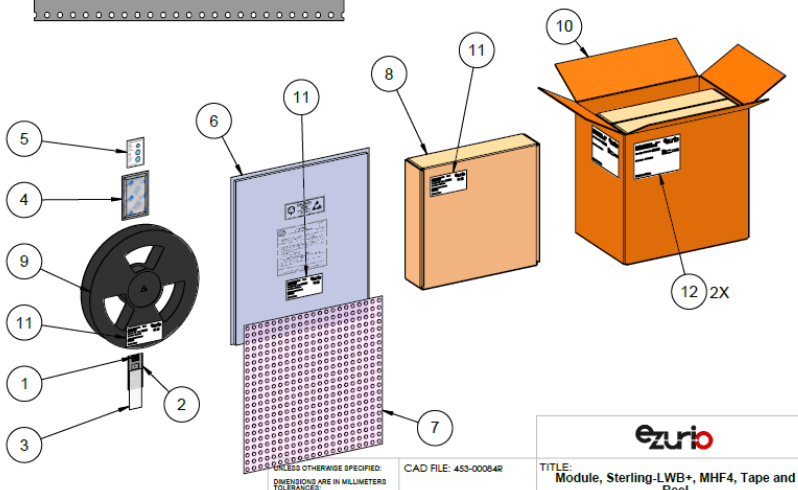
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS TOLERANCES: ANGULAR: ± ° X.X ± .2 X.XX ± .1 INTERPRET GEOMETRIC TOLERANCING PER: ASME 14.5M
CAD FILE: 161-00455
DATE
SHEET 1 OF 1
TITLE: Carrier Tape, Conductive Polystyrene, Black, 15.9mm x 21.4mm x 3.1mm
SIZE B | DWG. NO. 161-00455 | REV 1-1

Figure 25: Carrier Tape specifications for Module

ITEM NO.	PART NUMBER	REV.	DESCRIPTION	QTY.
1	453-00084	1-1	Module, Sterling-LWB+, MHF4	800
2	161-00455	1-1	Carrier Tape, Conductive Polystyrene, Black, 15.9mm x 21.4mm x 3.1mm	1
3	161-00456	1-1	Cover Tape, Anti-static Polyester, 37.5mm x 0.05mm	1
4	161-00438	1-1	Desiccant, Silica Gel, 56g, 125mm x 80mm	1
5	161-00236	1-1	Card, Humidity Indicator, Minimum 60% RH Spot, Three Spot Indication	1
6	161-00522	1-1	Bag, ESD and Moisture Barrier, Silver, MSL4, 465mm x 400mm x 0.15mm	1
7	161-00436	1-1	Bag, ESD Barrier, Bubble, Pink, 420mm x 420mm	1
8	161-00458	1-1	Box, Single-Wall Corrugated B Flute, 358mm x 340mm x 80mm	1
9	161-00459	1-1	Reel, 13inch Rotating Type, Black, 330mm x 100mm x 44mm	1
10	161-00460	1-1	Carton, Double-Wall, AB Flute, 376mm x 261mm x 366mm	1
11	160-02211	1-2	Label, Product Identifier, Sterling LWB+ Module, 110mm x 55mm	3
12	160-02212	1-3	Label, Carton Product Identifier, Sterling LWB+ Module, 101mm x 140mm	2

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1.0	Initial release	Jul 27, 2021	AC
1.1	Update Sterling LWB+ Top Level Parts to Remove 5GHz CE Pictogram	Sep 15, 2021	AC
1.2	Changed ESD bag	Jan 11, 2022	AC
1.3	Changed ESD bag(MSL4 print)	Feb 21, 2022	AC
1-4	Templates logo change	Mar 11, 2024	AC





Notes:
1.Put the Module in the carrier tape and cover the tape.
2.Put the Reel, Desiccant and Humidity Indicator Card in the ESD bag.
3.Put the packed ESD bag (vacuum) and Bubble bag in the box.
4.Put three boxes in the carton.
5.Module packaging quantity:
Per Reel: 800 PCS
Per Carton: 2400 PCS

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS TOLERANCES: ANGULAR: ± ° X.X ± .2 X.XX ± .1 INTERPRET GEOMETRIC TOLERANCING PER: ASME 14.5M
CAD FILE: 453-00084R
DATE
SHEET 1 OF 1
TITLE: Module, Sterling-LWB+, MHF4, Tape and Reel
SIZE B | DWG. NO. 453-00084R | REV 1-4

Figure 26: Sterling LWB+ Packaging Process for Module

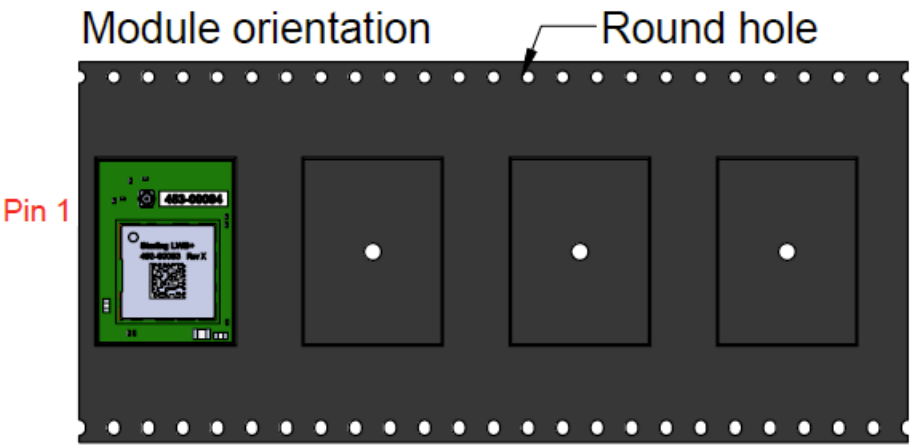


Figure 27: Module Orientation in Carrier Tape Pocket, MHF4 Variant 453-00084

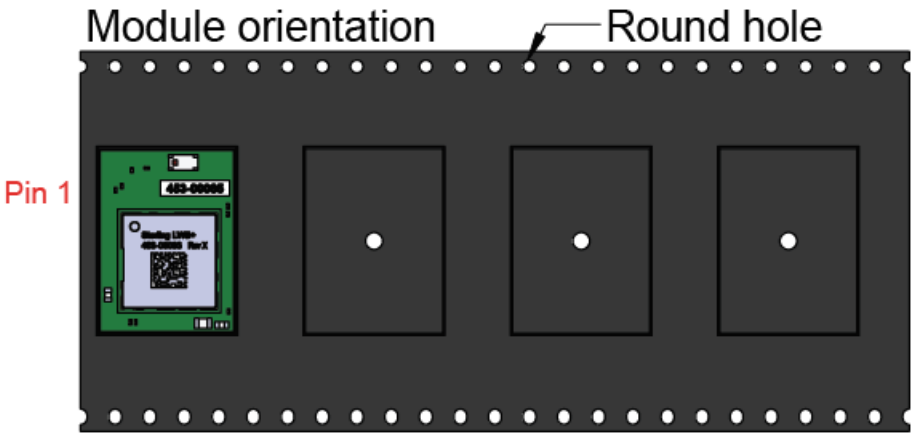


Figure 28: Module Orientation in Carrier Tape Pocket, Integrated Antenna Variant 453-00085

14.3 Module Shipping

All modules are shipped in tape and reel package and sealed in ESD Bags.

14.4 Labelling

The MSL information is printed on the anti-static bag. The Sterling LWB+ solder-down SIP and modules are classified as MSL4 devices.

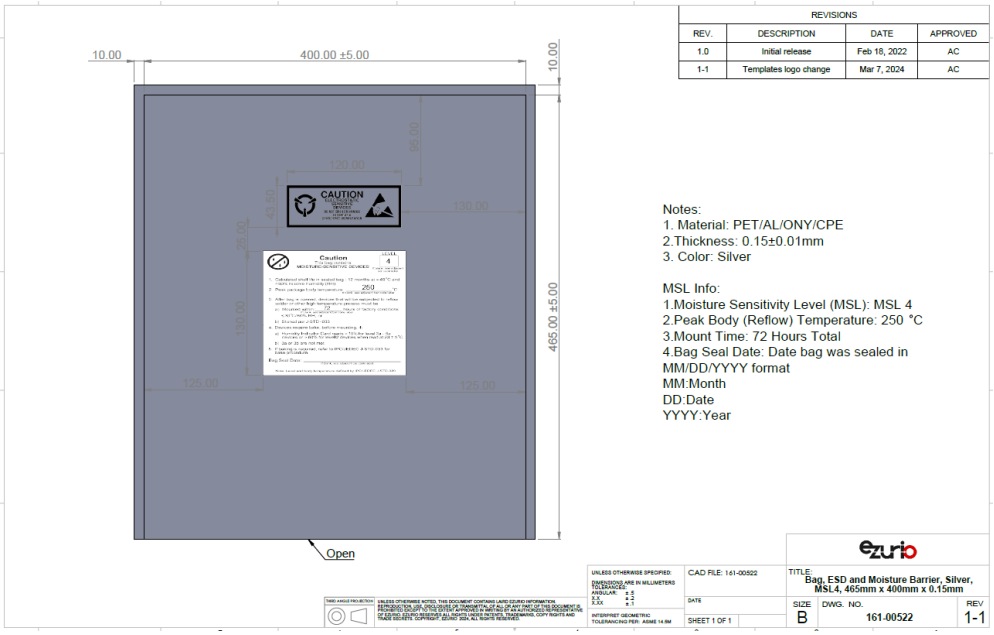


Figure 29: Anti-static Bag Containing MSL Information

The following labels are placed on the reel, anti-static bag, and pizza box.

Figure 30: Product Identifier Label (Left: SIP, 453-00083; Right: Modules, 453-00084 and 453-00085)

The following labels are placed on the master shipping carton.

Figure 31: Carton Product Identifier Label (Left: SIP, 453-00083; Right: Modules, 453-00084 and 453-00085)

15 Soldering Recommendations

15.1 Reflow for lead Free Solder Paste

- Optimal solder reflow profile depends on solder paste properties and should be optimized as part of an overall process development.
- It is important to provide a solder reflow profile that matches the solder paste supplier'srecommendations.
- Temperature ranges beyond that of the solder paste supplier's recommendation could result in poorsolderability.
- All solder paste suppliers recommend an ideal reflow profile to give the best solderability.

15.2 Recommended Reflow Profile for lead Free Solder Paste

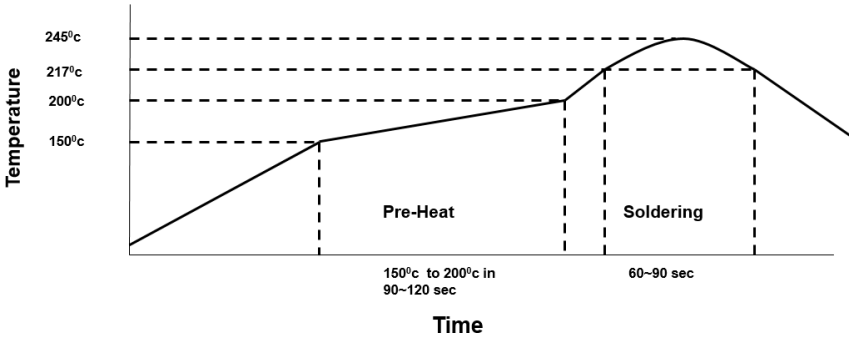


Figure 21: Recommended Reflow Profile

16 Wi-Fi / Bluetooth MAC ID

For the Sterling LWB+, the Wi-Fi MAC ID and Bluetooth MAC ID is preprogrammed during production for each module. The Bluetooth MAC ID is the Wi-Fi MAC ID plus one and Wi-Fi MAC ID is shown in the barcode on the shielding can.

Table 17: Example MAC ID assignments

	Wi-Fi MAC ID	Bluetooth MAC ID
Module 1	C0EE40B00000	C0EE40B00001
Module 2	C0EE40B00002	C0EE40B00003
Module 3	C0EE40B00004	C0EE40B00005
Module 4	C0EE40B00006	C0EE40B00007

17 Miscellaneous

17.1 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently

17.2 Rework

The Sterling LWB+ module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions terminate warranty coverage.

17.3 Handling and Storage

17.3.1 Handling

The Sterling LWB+ modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently

17.3.2 Moisture Sensitivity Level (MSL)

The Sterling-LWB+ SIP and SMT modules are MSL level 4.

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

17.3.3 Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX. Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

17.3.4 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

18 Reliability Test

18.1 Climatic Reliability Test

Table 18: Climatic Test Results for Sterling LWB+ Modules

Test Item	Specification	Standard	Test Result
Temperature Cycling	Temperature: -40 ~ 85℃ Ramp time: 15°C/min Dwell Time: 20 minutes Number of Cycles: 550 times Checkpoint: 350 Cycles	JESD22-A113	Pass

18.2 Reliability MTBF Prediction

Table 19: MTBF Predictions for Sterling LWB+ Modules

Ezurio Part Number	Environment	Standard	Test Result 25 ℃ (Hours)
453-00083R 453-00083C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	58,745,329
453-00084R 453-00084C 453-00085R 453-00085C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	44,637,151
Ezurio Part Number	**Environment**	**Standard**	**Test Result 40 ℃ (Hours)**
453-00083R 453-00083C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	32,385,965
453-00084R 453-00084C 453-00085R 453-00085C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	23,544,797
Ezurio Part Number	**Environment**	**Standard**	**Test Result 85 ℃ (Hours)**
453-00083R 453-00083C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	6,006,824

19 Regulatory

Note: For complete regulatory information, refer to the Sterling LWB+ Regulatory Information document which is also available from the Sterling LWB+ product page.

The Sterling LWB+ holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-LWBPLUS
EU	N/A
Canada (ISED)	3147A-LWBPLUS
Japan (MIC)	201-210737
Australia	N/A
New Zealand	N/A

20 Ordering information

Table 20: Orderable Sterling-LWB+ part numbers

Order Number	Description
453-00083C	Module, Sterling-LWB+, SIP, Cut Tape
453-00083R	Module, Sterling-LWB+, SIP, Tape and Reel
453-00084C	Module, Sterling-LWB+, MHF4, Cut Tape
453-00084R	Module, Sterling-LWB+, MHF4, Tape and Reel
453-00085C	Module, Sterling-LWB+, Chip Antenna, Cut Tape
453-00085R	Module, Sterling-LWB+, Chip Antenna, Tape and Reel
453-00141	Module, Sterling LWB+, M.2, Key E, SDIO, UART
453-00084-K1	Development Kit, Sterling-LWB+, MHF4
453-00085-K1	Development Kit, Sterling-LWB+, Chip Antenna

21 Bluetooth SIG Qualification

21.1 Overview

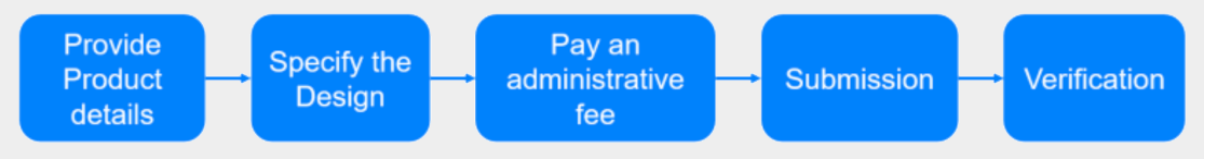
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

21.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference multiple existing designs, that have not been modified, (refer to Section 3.2.2.1 of the Qualification Program Reference Document v3).

For a Product that includes a new Design created by combining two or more unmodified designs that have DNs or QDIDs into one of the permitted combinations in Table 3.1 of the QPRDv3, a Member must also provide the following information:

- DNs or QDIDs for Designs included in the new Design
- The desired Core Configuration of the new Design (if applicable, see Table 3.1 below)
- The active TCRL Package version used for checking the applicable Core Configuration (including transport compatibility) and evaluating test requirements

Any included Design must not implement any Layers using withdrawn specification(s).

When creating a new Design using Option 2a, the Inter-Layer Dependency (ILD) between Layers included in the Design will be checked based on the latest TCRL Package version used among the included Designs.

For the purposes of this document, it is assumed that the member is combining unmodified Core-Controller Configuration and Core-Host Configuration designs, to complete a Core-Complete Configuration.

21.3 Qualification Steps When Referencing multiple existing designs, (unmodified) – Option 2a in the QPRDv3

For this qualification option, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number
    - Product Publication Date (the product publication date may not be later than 90 days after submission)

- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
  - If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the multiple DNs or QDIDs used in your, (for Option 2a two or more DNs or QDIDs must be referenced)
   - Select 'I'm finished entering DN's
   - Once the DNs or QDIDs are selected they will appear on the left-hand side, indicating the layers covered by the design (should show Core-Controller and Core Host Layers covered).
   - What do you want to do next? Answer, 'Combine unmodified Designs'.
   - The Qualification Workspace Tool will indicate that a new Design will be created and what type of Core-Complete configuration is selected.
   - An active TCRL will be selected for the design.
   - Perform the Consistency Check, which should result in no inconsistencies
   - If there are any inconsistencies these will need to be resolved before proceeding
   - Save and go to Test Plan and Documentation
5. Test Plan and Documentation
   a. As no modifications have been made to the combined designs the tool should report the following message:
   'No test plan has been generated for your new Design. Test declarations and test reports do not need to be submitted. You can continue to the next step.'
   b. Save and go to Product Qualification fee
6. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
7. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
8. Download Product and Design Details (SDoC):
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

21.4 Example Design Combinations

The following gives an example of a design possible under option 2a:

Ezurio Controller Subsystem + BlueZ 5.50 Host Stack (Ezurio Sterling-LWB+ based design)

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
Sterling-LWB+	Ezurio	D056404	162924	https://qualification.bluetooth.com/ListingDetails/142637
BlueZ 5.50 Host Stack	Ezurio	D046330	138224	https://qualification.bluetooth.com/ListingDetails/93911

21.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

22 Chip Antenna Performance

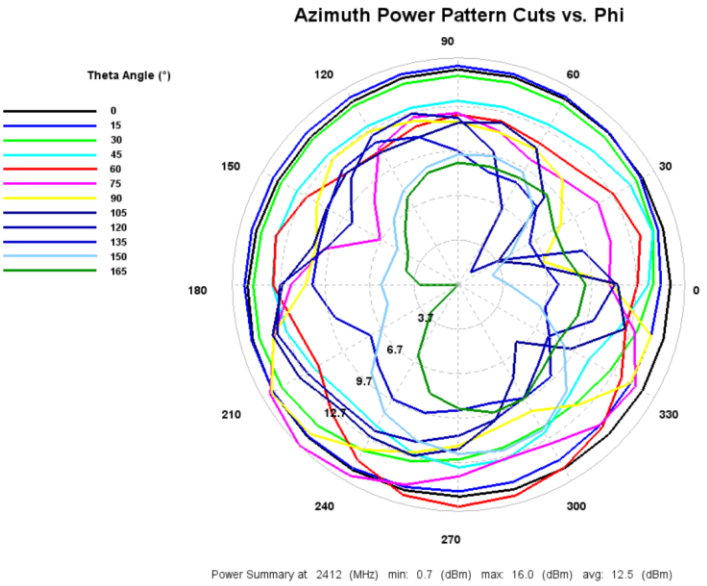
22.1 Summary of Antenna Performance

Table 21: Typical Antenna Performance

Channel	Frequency (MHz)	Antenna P (dBm)	TRP (dBm)	Max EIRP (dBm)	Efficiency (dB)	Gain (dBi)
1	2412	15.7	12.1	16.0	-3.6	0.3
7	2442	16.6	13.6	12.3	-3.0	0.8
13	2472	14.8	12.2	9.6	-2.6	1.5

22.2 2.4GHz Radiated Performance

EIRP Azimuth Cut



3D Plots:

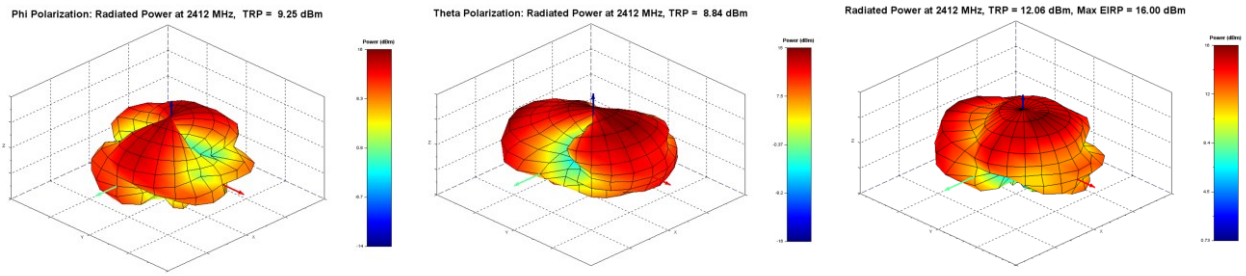
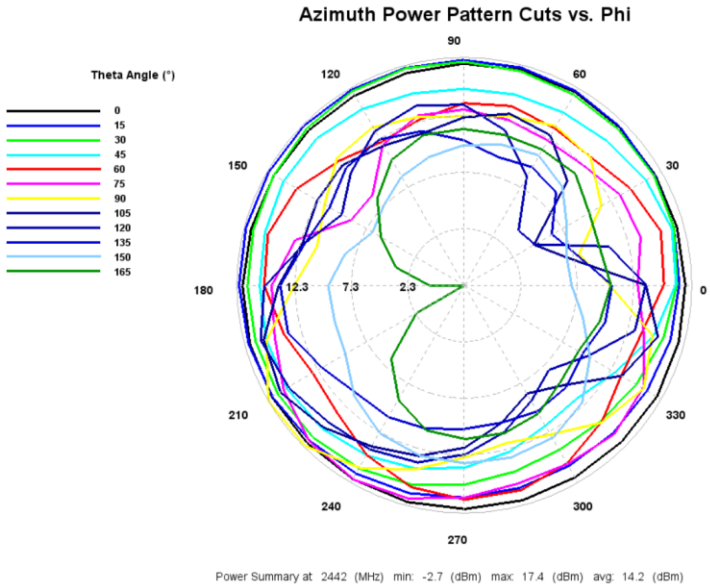


Figure 32: Channel 1 - 2412 MHz Horizontal, Vertical, and Total Patterns

EIRP Azimuth Cut



3D Plots:

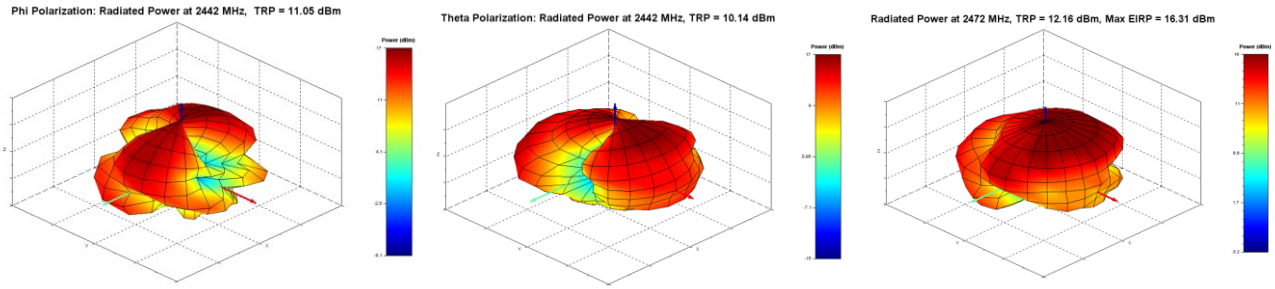
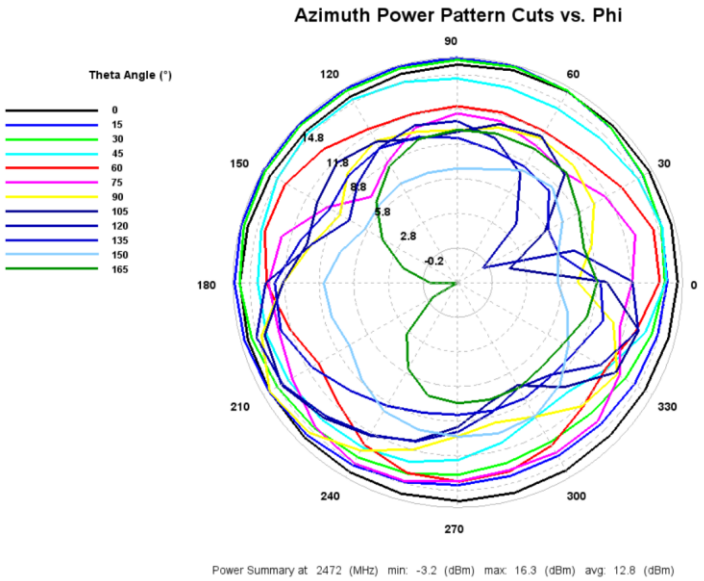


Figure 33: Channel 7 - 2442 MHz Horizontal, Vertical, and Total Patterns

EIRP Azimuth Cut



3D Plots:

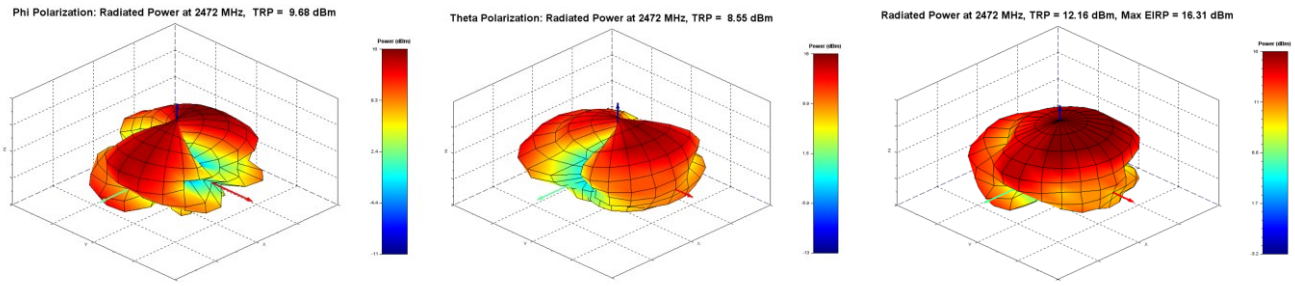


Figure 34: Channel 13 - 2472 MHz Horizontal, Vertical, and Total Patterns

23 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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