User Guide

Nitrogen8M_Nano

Version 1.0

Revision History

Version	Date	Notes	Contributors	Approver
0.1	11/27/2019	First Draft		KG
0.2	07/15/2020	Added Links		PK
0.3	01/07/2021	Added RS485		PK
1.0	23 July 2024	Ezurio rebranding	Sue White	Dave Drogowski

Contents

1 Overview

1.1 General Information

The Nitrogen8 family of SBCs and SOMs are the latest in Ezurio's i.MX based embedded computing solutions.

The different Nitrogen8 series of SBCs and SOMs include offerings designed to best leverage the advantages of the i.MX8M applications processors to fit a variety of embedded and IoT applications including: consumer/ industrial automation, aviation & aerospace, HMI, industrial control, robotics, building control, digital displays, infotainment, telematics, and more.

The Nit8M_Nano is designed for mass production use with a guaranteed 10-year life span, FCC Pre-scan results, and a stable supply chain. Industrial temperature and conformal coating options are available. It can also include from 1GB up to 2GB of LPDDR4 RAM.

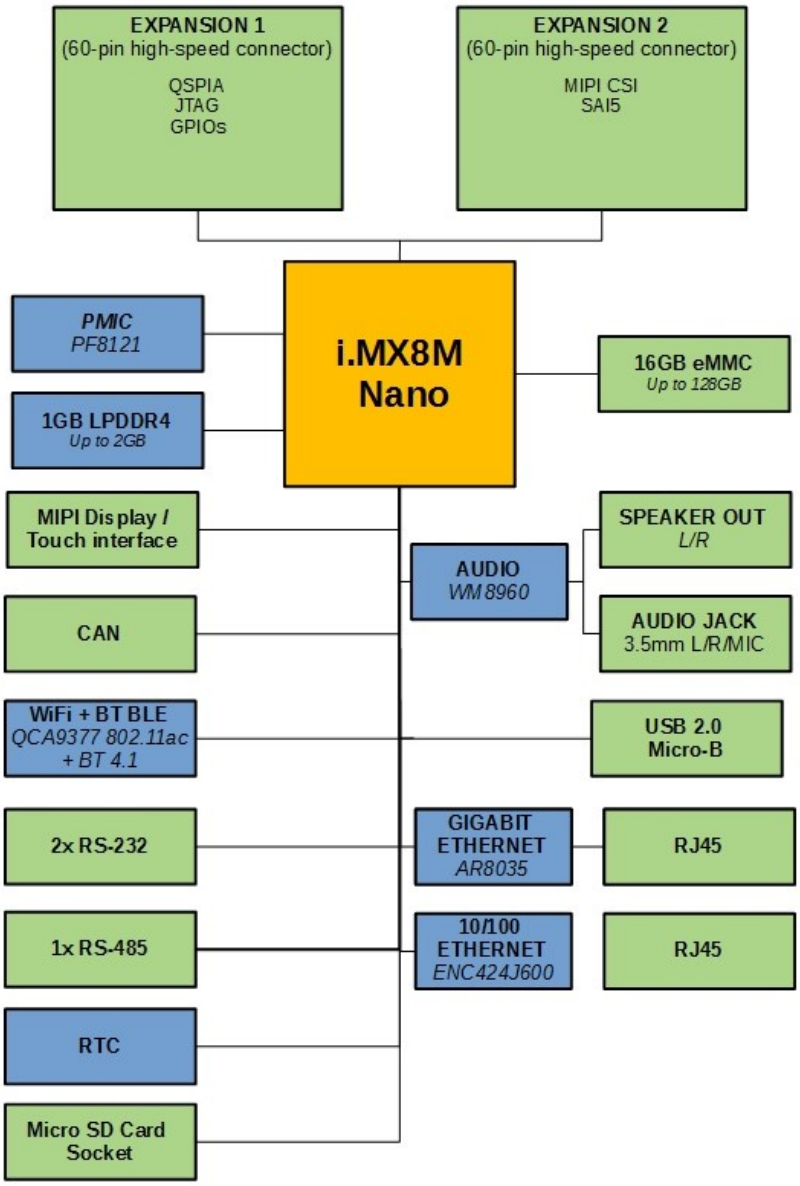
Software Support:

Industry leading OS-Level support can be found on the Ezurio website via the Wiki (https://bdwiki.ezurio.com/index.php/Main_Page). You can also find images for the latest versions of popular OS supported by the Nitrogen platforms including: Android, Linux (Yocto, Debian, Ubuntu), and FreeRTOS,

1.2 Feature Summary

- Quad-Core ARM® Cortex-A53 (64-bit) processor at 1.5GHz
- General purpose Cortex M7 core processor for low-power processing
- PF8121 PMIC (For low power consumption)
- 1GB of LPDDR4. Expandable to 2GB LPDDR4
- 16GB eMMC – Expandable to 128GB
- 1x USB 2.0
- 1x 1GB Ethernet + 1x 10/100 Ethernet
- 1x 4-LaneMIPI DSI Display Port
- 1x 4-Lane MIPI CSI Camera Interface (via daughterboard)
- CAN Bus
- RS-485 + 2 x RS-232
- Wi-Fi + BT (802.11 AC & BT 5.0)
- Temperature: 0 °C to +70 °C (Industrial available)

1.3 Block Diagram

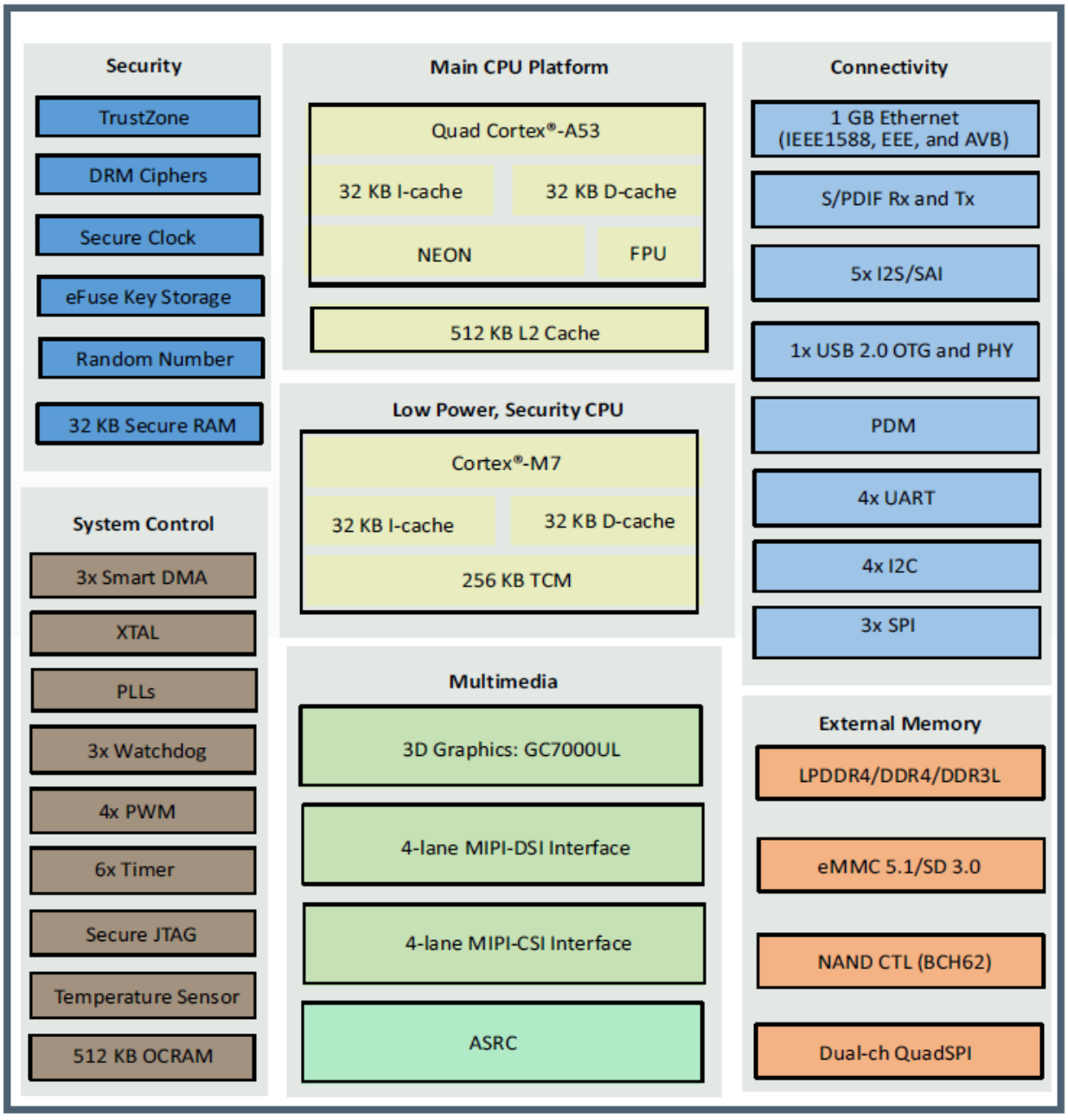


1.4 NXP I.MX8 Nano Processor

1.4.1 Overview

The i.MX 8M Nano family of processors features advanced implementation of a quad Arm® Cortex®-A53 core, which operates at speeds of up to 1.5 GHz. A general-purpose Cortex®-M4 700 MHz core processor is for low-power processing. The DRAM controller supports 16-bit LPDDR4, DDR4, and DDR3L memory. A wide range of audio interfaces are available, including I2S, AC97, TDM, and S/PDIF. There are several other interfaces for connecting peripherals, such as USB and Ethernet.

1.4.2 I.MX8 Nanoblock Diagram



1.4.3 CPU

The i.MX 8M Nano applications processor represents NXP's latest video and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption.

- Arm Cortex-A53 MP Core Platform
- Quad symmetric Cortex-A53 processors:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture:
  - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
  - Support of 64-bit Armv8-A architecture
  - 512 KB unified L2 cache
- Arm Cortex-M7 core platform
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - 256 KB tightly coupled memory (TCM)
- Low power microcontroller available for customer application
  - low power standby mode
  - IoT features including Weave
  - Manage IR or Wireless Remote
  - ML interface applications

1.4.4 Memory

The on-chip memory system consists of the following:

- Boot ROM (256KB)
- On-chip RAM (512KB + 32KB)

The external memory interfaces supported on this chip include:

- 16-bit DRAM Interface:
  - LPDDR4-3000
- eMMC 5.1 FLASH
- FlexSPI FLASH

The i.MX 8M Nano supports the following boot devices:

- SDIO / MMC / SDXC
- eSD 3.0/eMMC 5.1 (fast boot)

1.4.5 Display

The chip has the following display support:

LCDIF Display Controller:

- Supports up to 2 layers of overlay
- Support up to 1080p60 display through MIPI DSI

MIPI Interface:

- 4-lane MIPI CSI interface
- 4-lane MIPI DSI interface
- Supports 4 cameras using MIPI-CSI2 Virtual Channel support (ISI module)

1.4.6 Graphics Processing Unit

The chip incorporates the following Graphics Processing Unit (GPU) features:

- 2D/3D acceleration
- 2 Shader
- Support OpenGL ES 1.1, 2.0, 3.0
- Supports OpenCL
- Supports OpenVG 1.1
- Supports Vulkan

2 Connector Details

2.1 Custom Connectors

J15: Expansion Connector #1 (Molex 52991-0608)			
PIN#	**Signal**	**Voltage Domain**	**Voltage Level**
1	CSI_D0_N	VDD_MIPI_1P8	1.8V
2	GND	-	-
3	CSI_D0_P	VDD_MIPI_1P8	1.8V
4	SAI5_RXD0	NVCC_SAI5	3.3V
5	GND	-	-
6	SAI5_RXD1	NVCC_SAI5	3.3V
7	CSI_D1_N	VDD_MIPI_1P8	1.8V
8	SAI5_RXD2	NVCC_SAI5	3.3V
9	CSI_D1_P	VDD_MIPI_1P8	1.8V
10	SAI5_RXD3	NVCC_SAI5	3.3V
11	GND	-	-
12	SAI5_FXFS	NVCC_SAI5	3.3V
13	CSI_CK_N	VDD_MIPI_1P8	1.8V
14	GND	-	-
15	CSI_CK_P	VDD_MIPI_1P8	1.8V
16	SAI5_MCLK	NVCC_SAI5	3.3V
17	GND	-	-
18	GND	-	-
19	CSI_D2_N	VDD_MIPI_1P8	1.8V
20	-	-	-
21	CSI_D2_P	VDD_MIPI_1P8	1.8V
22	-	-	-
23	GND	-	-
24	-	-	-
25	CSI_D3_N	VDD_MIPI_1P8	1.8V
26	-	-	-

J15: Expansion Connector #1 (Molex 52991-0608)			
27	CSI_D3_P	VDD_MIPI_1P8	1.8V
28	-	-	-
29	GND	-	-
30	-	-	-
31	-	-	-
32	-	-	-
33	-	-	-
34	-	-	-
35	-	-	-
36	-	-	-
37	-	-	-
38	GND	-	-
39	-	-	-
40	-	-	-
41	-	-	-
42	-	-	-
43	-	-	-
44	-	-	-
45	-	-	-
46	-	-	-
47	GND	-	-
48	-	-	-
49	LDO3_1P8V_TO_3P3V	Power Output	DEFAULT 1.8V FOR CUSTOMER USE 350 MA MAX
50	-	-	-
51	LDO3_1P8V_TO_3P3V	Power Output	DEFAULT 1.8V FOR CUSTOMER USE 350 MA MAX
52	-	-	-
53	LDO3_1P8V_TO_3P3V	Power Output	DEFAULT 1.8V FOR CUSTOMER USE 350 MA MAX
54	GND	-	-
55	LDO3_1P8V_TO_3P3V	Power Output	DEFAULT 1.8V FOR CUSTOMER USE 350 MA MAX
56	1.8V	-	1.8V
57	3.3V	-	3.3V
58	1.8V	-	1.8V
59	3.3V	-	3.3V
60	1.8V	-	1.8V

J16: Expansion Connector #2 (Molex 52991-0608)			
PIN#	**Signal**	**Voltage Domain**	**Voltage Level**
1	GND	-	-
2	RTC_RESET_B	NVCC_SNVS_1P8	-
3	QSPIA_SCLK	-	-
4	TP17	-	-
5	GND	-	-
6	GND	-	-
7	QSPIA_DATA3	NVCC_NAND	1.8V
8	BI2C3_SCL		
9	QSPIA_DATA2	NVCC_NAND	1.8V
10	BI2C3_SDA		
11	QSPIA_DATA1	NVCC_NAND	1.8V
12	GND	-	-
13	QSPIA_DATA0	NVCC_NAND	1.8V
14	GND	-	-
15	QSPIA_NSS0	NVCC_NAND	1.8V
16	ON_OFF	NVCC_SNVS_1P8	1.8V
17	NAND_CLE	NVCC_NAND	1.8V
18	GPIO_IO11	NVCC_GPIO1	3.3V
19	GND	-	-
20	GND	-	-
21	CLKIN1	NVCC_CLK	1.8V
22	-	-	-
23	CLKOUT1	NVCC_CLK	1.8V
24	GND	-	-
25	GND	-	-
26	-	-	-
27	CLKIN2	NVCC_CLK	1.8V
28	-	-	-
29	CLKOUT2	NVCC_CLK	1.8V
30	-	-	-
31	GND	-	-
32	GND	-	-
33	JTAG_NTRST	NVCC_JTAG	3.3V
34	SPDIF_EXT_CLK/PWM1		
35	JTAG_TDO	NVCC_JTAG	3.3V
36	GND	-	-

J16: Expansion Connector #2 (Molex 52991-0608)			
37	JTAG_TCK	NVCC_JTAG	3.3V
38	-	-	-
39	JTAG_TDI	NVCC_JTAG	3.3V
40	GND	-	-
41	JTAG_TMS	NVCC_JTAG	3.3V
42	GPIO1_IO8	NVCC_GPIO1	3.3V
43	GND	-	-
44	GPIO1_IO5/M4NMI	NVCC_GPIO1	3.3V
45	EXT_RESET_N	NVCC_SNVS_1P8V	1.8V
46	-	-	-
47	GND	-	-
48	PMIC_ON_REQ	NVCC_SNVS_1P8	1.8V
49	TP18	-	-
50	TP20	-	-
51	TP19	-	-
52	GND	-	-
53	TP21	-	-
54	GND	-	-
55	TP22	-	-
56	+5V	-	5V Power
57	3P3V	-	3.3V
58	+5V	-	5V Power
59	3P3V	-	3.3V
60	+5V	-	5V Power

J2: CAN (Molex 53398-0371)	
PIN#	**Function**
1	CANH
2	CANL
3	GND

2.2 Pin MUX

There are many pin muxing options on the i.MX8M Nano processor to change pins to GPIO, or other functions. If you need more GPIO, or need other signals, please contact us to discuss pin muxing options. Please also register on the NXP website to get the i.MX8M Nano reference manual.

3 Interfaces

3.1 Display Interfaces

3.1.1 Overview

The Nit8M_Nano consists of the following display interfaces:

- One MIPI/DSI port - driven by the MIPI/DSI transmitter; four data lane 1080p60 with a maximum bit rate of 1.5 Gbps.

3.1.2 DSI

Nit8M_Nano MIPI DSI Host Controller supports up to 4 D-PHY data lanes:

J8: MIPI-DSI + Touch Connector (Omron XF2M-3315-1A)	
PIN#	**Function**
1	GND
2	GND
3	+5V
4	+5V
5	+5V
6	+5V
7	SPDIF_TX/PWM3
8	GPIO1_IO01
9	TOUCH_INT
10	TOUCH_RESET
11	GPIO_IO09
12	GND
13	DSI_D3_N
14	DSI_D3_P
15	GND
16	DSI_D2_N
17	DSI_D2_P
18	GND
19	DSI_CLK_N
20	DSI_CLK_P
21	GND
22	DSI_D1_N
23	DSI_D2_P
24	GND
25	DSI_D0_N
26	DSI_D0_P
27	GND

J8: MIPI-DSI + Touch Connector(Omron XF2M-3315-1A)	
28	I2C2_SCL
29	I2C2_SDA
30	3P3V
31	3P3V
32	3P3V
33	3P3V

3.1.3 HDMI

HDMI is available using Ezurio DSI to HDMI converter daughter board.

BD_DSIHD Product Link: https://ezurio.com/product/db_8mm_dsihd/

3.1.4 LVDS

LVDS is available using Ezurio DSI to LVDS converter daughter board.

BD_DSIHD Product Link: https://ezurio.com/product/db_8mm_dsihd/

3.2 Camera Interfaces

3.2.1 MIPI CSI

MIPI CSI2 (four-lane)- This module provides one four-lane MIPI camera serial interfaces, which operates up to a maximum bit rate of 1.5 Gbps. The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

MIPI CSI-2signals: (J15 expansion Connector)		
Pin #	**Signal**	**Description**
1	CSI_D0_N	Negative CSI-0 Clock Differential
3	CSI_D0_P	Positive CSI-0 Clock Differential
7	CSI_D1_N	Negative CSI-1 Clock Differential
9	CSI_D1_P	Positive CSI-1 Clock Differential
13	CSI_CK_N	Negative Clock Differential
15	CSI_CK_P	Positive Clock Differential
19	CSI_D2_N	Positive CSI-2 Clock Differential
21	CSI_D2_P	Negative CSI-2 Clock Differential
25	CSI_D3_N	Negative CSI-3 Clock Differential
27	CSI_D3_P	Positive CSI-3 Clock Differential

3.3 Ethernet

Gigabit Ethernet Features:

The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external Gigabit magnetics is required to complete the interface to the media.

Vendor	Part Number	Package
Microchip	ENC424J600	10/100 Ethernet Controller
Link PP	LPJ16211AENL	RJ45 Ethernet Jack

GigabIt Ethernet:

Vendor	Part Number	Package
Qualcomm	AR8035-AL1A	PHY Transceiver
Link PP	LPJ1014AHNL	RJ45 Ethernet Jack

3.4 Wi-Fi and Bluetooth

The Nit8M_Nano is populated with the BD-SDMAC is a dual-band 1×1 802.11a/b/g/n/ac plus Bluetooth 5.0+HS “Smart Ready” SDIO module based on the Silex SX-SDPAC/Qualcomm Atheros QCA9377 System-on-Chip (SoC). The BD-SDMAC is a pre-certified module with a compact 13mm x 18mm footprint. BD-SDMAC provides an SDIO3.0 interface for WLAN and a hi-speed UART interface for BT. The module can be evaluated with any Ezurio single board computer and driver support is integrated in all Ezurio kernels.

3.5 USB 2.0 OTG

High-speed OTG core:

- HS/FS/LS UTMI compliant interface
- High speed, full speed and low speed operation in host mode (with UTMI transceiver)
- High speed, and full speed operation in peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional end points
- Integrated HS USBPHY

3.6 MMC/SD/SDIO

i.MX8M Nano SoC characteristics:

All the MMC/SD/SDIO controller IPs are based on the uSDHC IP.

They are designed to support:

- SD/SDIO standard, up to version 3.0
- MMC standard, up to version 5.1
- Support for SDXC (extended capacity)
- 1.8 V and 3.3 V operation, but do not support 1.2 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode

One uSDHC controller (SD1) can support up to an 8-bit interface, the other controller (SD2) can only support up to a 4-bit interface.

SDMMC2 Signals:

Pin #	Signal	Description
1	SD2_DATA2	SD Data 2 Line
2	SD2_DATA3	SD Data 3 Line

Pin #	Signal	Description
3	SD2_CMD	CMD Line Connect to Card
4	3P3V	3.3V
5	SD2_CLK	Clock
6	GND	Ground
7	SD2_DATA0	SD2 Data 0 Line
8	SD2_DATA1	SD2 Data 1 Line
9	GND	Ground
10	SD2_CD	Connect to SD2 CD Pin on SD Card
11	GND	Ground

3.7 Audio

The Nit8M_Nanofeatures these audio interfaces:

- WM8960CGEFL/V Audio codec interfaces
  - Analog outputs/inputs:
    - Stereo HP out
    - Lineout L/R
    - Built-In 2W Amplifier

*Reference the Cirrus Website for technical specifications. https://statics.cirrus.com/pubs/proDatasheet/WM8960_v4.4.pdf

J4: 2W Amplified Audio – Left Channel (Molex 53047-0210	
PIN#	**Function**
1	SPK_LN
2	SPK_LP

J5: 2W Amplified Audio – Right Channel (Molex 53047-0210)	
PIN#	**Function**
1	SPK_RN
2	SPK_RP

J18: Microphone (Molex 53047-0310)	
PIN#	**Function**
1	GND
2	MIC_IN2_P
3	3P3VMIC DETECT

3.8 UARTINTERFACES

All 4 UART interfaces are supported, based on pin mux configurations of the UART interface.

UART Features:

- High-speed TIA/EIA-232-F compatible, up to Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9-bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Edge-selectable RTS_B and edge-detect interrupts
- Status flags for various flow control and FIFO states
- Voting logic for improved noise immunity (16x oversampling)
- Transmitter FIFO empty interrupt suppression
- UART internal clocks enable/disable
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode
- DCE/DTE capability
- RTS_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode
- Maskable interrupts
- Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
- Escape character sequence detection
- Software reset (SRST_B)
- Two independent, 32-entry FIFOs for transmit and receive
- The peripheral clock can be totally asynchronous with the module clock. The module clock determines baud rate. This allows frequency scaling on peripheral clock (such as during DVFS mode) while remaining the module clock frequency and baud rate

UART1 Signals: reserved for Wifi/BT Module

UART2 Signals:

J9: COM1 & COM2 Connector (Molex 53047-0610)	
PIN#	**Function**
1	-
2	+5V
3	GND
4	UART2_TXD
5	UART2_RXD
6	-

*UART2 is used as the U-Boot and O/S console. UART2 is mapped to /dev/ttymxc0.

J20: RS485/UART4 Connector (Molex 53047-0310)	
PIN#	**Function**
1	GND
2	RS485-A
3	RS485-B

SW6 is a termination switch to enable termination if necessary.

3.9 FLEXIBLE SPI

FlexSPI with support for XIP (for ME in low-power mode) and parallel read mode of two identical FLASH devices

The FlexSPI module acts as an interface to external serial flash devices. This module contains the following features:

- Flexible sequence engine to support various flash vendor devices
- Single pad/Dual pad/Quad pad mode of operation
- Single Data Rate/Double Data Rate mode of operation
- Parallel Flash mode
- DMA support
- Memory mapped read access to connected flash devices
- Multi master access with priority and flexible and configurable buffer for each master GIC Generic Interrupt Controller the GIC handles all interrupts

3.10 eCSPI KEY features

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

- Full-duplex synchronous serial interface
- Master/slave configurable
- Four chip select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmitting and receiving data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the chip select (SS) and SPI clock (SCLK) are configurable
- Direct Memory Access (DMA)support
- Max operation frequency up to the reference clock frequency

3.11 I2C

I2C-1, 2,3, 4Interface connectivity peripherals provide serial interface for external devices.

The I2C operates primarily in two functional modes: Standard mode and Fast mode.

- In Standard mode, I2C supports the data transfer rates up to 100 kbits/s.
- In Fast mode, data transfer rates up to 400 kbits/s can be achieved. Per block operation, there is no special configuration required for Fast or Standard mode. It is the data transfer rate that distinguishes Standard and Fast mode.

I2C1 Signals: I2C1 Is Reserved for PMIC

I2C2 Signals: Reserved for DSI Display + touchscreen

I2C3Signals: reserved for rtc + expansion port

I2C4 Signals: reserved for audio

3.12 General Purpose I/O

Most of the Nano's IO pins can be used as GPIOs. If you need more GPIO, or need other signals, please contact us to discuss pin muxing options.

3.13 General System Control

3.13.1 Reset

'0' logic will reset Nit8M_Nano

3.14 Reference Clock Out

Nit8M_Nano output clock is controlled by the i.MX8 Nano CCM module. Please refer to the i.MX8 Nano User Manual regarding the configuration option for this clock.

4 Operational Characteristics

4.1 Power Supply

Description	Signal	Description	Typical	Tolerance	Unit
Main Power Supply, DC-IN	5VIN	DC Supply Voltage	5	+/- 5%	V

4.2 Power Consumption

Parameter	Min	Typical	Max	Unit
Main Input Voltage	-	5	-	V
Power Consumption*	-	1300	2700	mW
CPU Clock	-	-	1.5	Ghz

*Reference the NXP Website to get the i.MX8 Nano reference manual for power consumption and CPU clock speed specifications

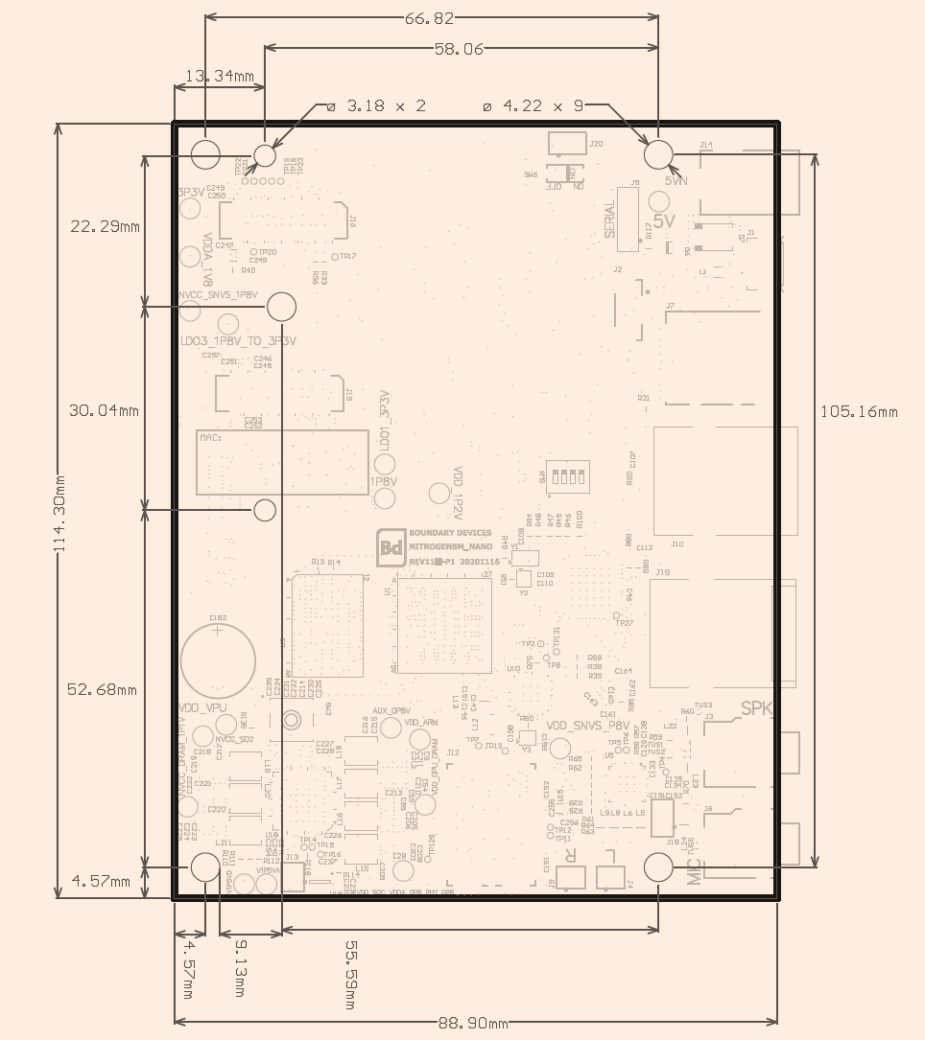
5 Environmental Specifications

Operating Rating	Min. Temperature	Max. Temperature
Commercial Operating Temperature Range	0°C	+70°C
Industrial Operating Temperature Range	-40°C	+85°C

Note: Commercial and Industrial Temperature is based on the operating temperature grade of the SOM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

6 Mechanical Drawing

6.1.1.1 Top View



7 Orderable Part Numbers

SKU	CPU	DDR Memory	eMMC Storage Size	Operating Rating	Operating Temperature Range
Nit8M_Nano_1r16eWB_BRD	i.MX8 Nano Quad	1GB	16GB	Commercial	0° to 70°C
Nit8M_Nano_1r16eWB_i_BRD	i.MX8 Nano	1GB	16GB	Industrial	-40° to 85°C

*Please contact us to discuss other custom options

8 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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