Datasheet

BT740 Enhanced Class 1 Bluetooth v2.1 Module

Version 3.1

Revision History

Version	Date	Notes	Contributor	Approver
1.0	30 July 2013	Initial Release		Jonathan Kaye
1.1	30 Sept 2013	Removed yellow highlights		Jonathan Kaye
1.2	19 Dec 2013	Fixed typo.		Jonathan Kaye
1.3	06 Feb 2014	Updated Bluetooth SIG Qualification section.		Jonathan Kaye
1.4	16 Aug 2016	Changed from *Hardware Integration Guide* to *Datasheet*.		Sue White
1.5	19 Sept 2016	Updated EU Declaration of Conformity		Sue White
1.6	16 June 2017	Updated EU DoC with new RED standards		Tom Smith
1.7	25 Aug 2020	Updated mechanical drawing		Jonathan Kaye
1.8	22 Nov 2020	Updated all regulatory information	Ryan Urness	Jonathan Kaye
2.0	01 Feb 2021	Moved regulatory information into separate document	Sue White	Jonathan Kaye
2.1	13 Mar 2023	Updated BT standard to 2.1 in Specifications	Dave Drogowski	Mark Duncombe
2.2	6 Nov 2024	Updates to Bluetooth SIG Approvals	Dave Drogowski	Jonathan Kaye
3.0	24 Jan 2025	Updated to Ezurio format.	Dave Drogowski	Dave Drogowski
3.1	11 Dec 2025	Updated MSL level to MSL 4.	Dave Drogowski	Jonathan Kaye

© Copyright 2025 Ezurio
All Rights Reserved

Contents

© Copyright 2025 Ezurio
All Rights Reserved

© Copyright 2025 Ezurio
All Rights Reserved

1 Overview and Key Features

Every BT740 series Bluetooth® module from Ezurio is designed to add robust, long-range Bluetooth data connectivity to any device. Based on the market-leading Cambridge Silicon Radio (CSR) BC04 chipset, BT740 modules provide exceptionally low power consumption with outstanding Class 1 range via 18 dBm of transmit power. The modules support the latest Bluetooth Version 2.1 specification, including Secure Simple Pairing (SSP), which improves security and enhances the ease of use for end customers. A broad range of Bluetooth profiles such as Serial Port Profile (SPP) and other vital features make BT740 modules superior to other Bluetooth modules.

With a compact footprint of 15.29 x 28.71 mm, the modules deliver maximum range with a minimum size. To ease integration, the modules are designed to support a separate power supply for I/O. Another integration advantage is the inclusion of a complete Bluetooth protocol stack with support for multi-point connections and numerous Bluetooth profiles, including SPP, Human Interface Device (HID) profile, and Health Device Profile (HDP). BT740 modules fully qualify as a Bluetooth End Products, enabling designers to integrate the modules in devices without the need for further Bluetooth qualification.

An integrated AT command processor interfaces to the host system over a serial port using an extensive range of AT commands. The AT command set abstracts the Bluetooth protocol from the host application, saving many months of programming and integration time. It provides extremely short integration times for data-oriented Bluetooth applications.

Included firmware provides programming support for multi-point applications that use up to seven simultaneous data connections to and from the robust BT740 module. A low-cost developer's kit makes it easy for an OEM to integrate the module and guarantees the fastest route to prototype and then mass production.

Features & Benefits

- Bluetooth v2.1 + EDR
- External or internal antennas
- Comprehensive AT interface for simple programming
- Alternate packet-based interface for complex programming and up to seven simultaneous connections
- Bluetooth EPL
- Compact footprint
- Class 1 output – 18 dBm
- UART interface with GPIO and ADC lines
- Industrial temperature range
- Field proven firmware used on BTM44x series of modules

Application Areas

- Medical devices
- ePOS terminals
- Automotive diagnostic equipment
- Barcode scanners
- Industrial cable replacement

Bluetooth® Profiles Supported

- Serial Port Profile (SPP)
- Human Interface Device (HID) profile host and device supported
- Health Device Profile (HDP): Agent supported
- IEEE Device Specialization 11073-10415 (Weight Scale)
- IEEE Device Specialization 11073 - 10408 (Thermometer)
- IEEE Device Specialization 11073 – 10417 (Glucose)

© Copyright 2025 Ezurio
All Rights Reserved

2 Specifications

2.1 Detailed Specifications

Table 2-1: Detailed Specifications

Categories	Feature	Implementation
Wireless Specification	Bluetooth®	V2.1
	Frequency	2.402 - 2.480 GHz
	Bluetooth Transmitter Class	Class 1 (Basic Rate BT)
	Max Transmit Power	18 dBm into integrated antenna (BT740-SA) 16 dBm into UFL antenna connector (BT740_SC)
	Min Transmit Power	-9 dBm into integrated antenna -9 dBm into UFL antenna connector
	Receive Sensitivity	Better than -87 dBm (at 25° C)
	Range	>1000m (Line of Sight)
	Data Rates	Up to 1.0 Mbps (over the air)
	UART Data Transfer Rate	Circa 350 kbps
Host Interface	UART	One UART TX, RX, DCD, RI, DTR, DSR, CTS, RTS[1] Default 9600, n, 8, 1 From 1,200 to 921,600 bps
	GPIO	8 configurable lines
	ADC	Two ADC channels 8 bit resolution
	PCM	Not Supported in Firmware (One PCM interface)
Profiles	SPP	Serial Port Profile
	HID	Human Interface Device
	HDP	Health Device Profile
Command Interfaces	Operation Modes	AT Command Set Multi-Point API – seven simultaneous connections
	Firmware Upgrade	Firmware Upgrade over UART
Audio	Support SCO Channels PCM Interface	Not Supported in Firmware
Supply Voltage	Supply	3.0 – 5.0 V On-board regulators and brown-out detection. GPIO voltages are 3.3V logic.
Power Consumption	Various Modes – Typical values (see Power Consumption section for test conditions)	Idle mode: 1.25 mA Discoverable: 2.7 mA to 55 mA Inquiry mode: 65 mA Connecting mode: 66 mA

© Copyright 2025 Ezurio
All Rights Reserved

Categories	Feature	Implementation	
		Connected mode (no data transfer)	6 mA
		Connected mode (max data transfer)	35 mA
		Sniff mode	1.8 mA
Antenna Options	Internal	Multilayer ceramic - BT740-SA	
	External	Connection via u.FL - BT740-SC	
Physical	Connections	Surface Mount Pads (1.2mm pitch)	
	Dimensions	15.29 mm x 28.71 mm x 2.5 mm	
	Weight	1.5 g	
Environmental	Operating	-40 °C to +85 °C	
	Storage	-40 °C to +85 °C	
	MSL	4	
Miscellaneous	Lead Free	Lead-free and RoHS compliant	
	Warranty	1-Year Warranty	
Development Tools	Development Kit	Development kit DVK-BT740 and software tools	
Approvals	Bluetooth®	End Product Listing (EPL)	
	FCC/ISED/EU	All BT740 Series	

DSR, DTR, RI and DCD are configurable either as GPIO or as modem control lines.

© Copyright 2025 Ezurio
All Rights Reserved

3 Hardware Specifications

3.1 Hardware Specifications

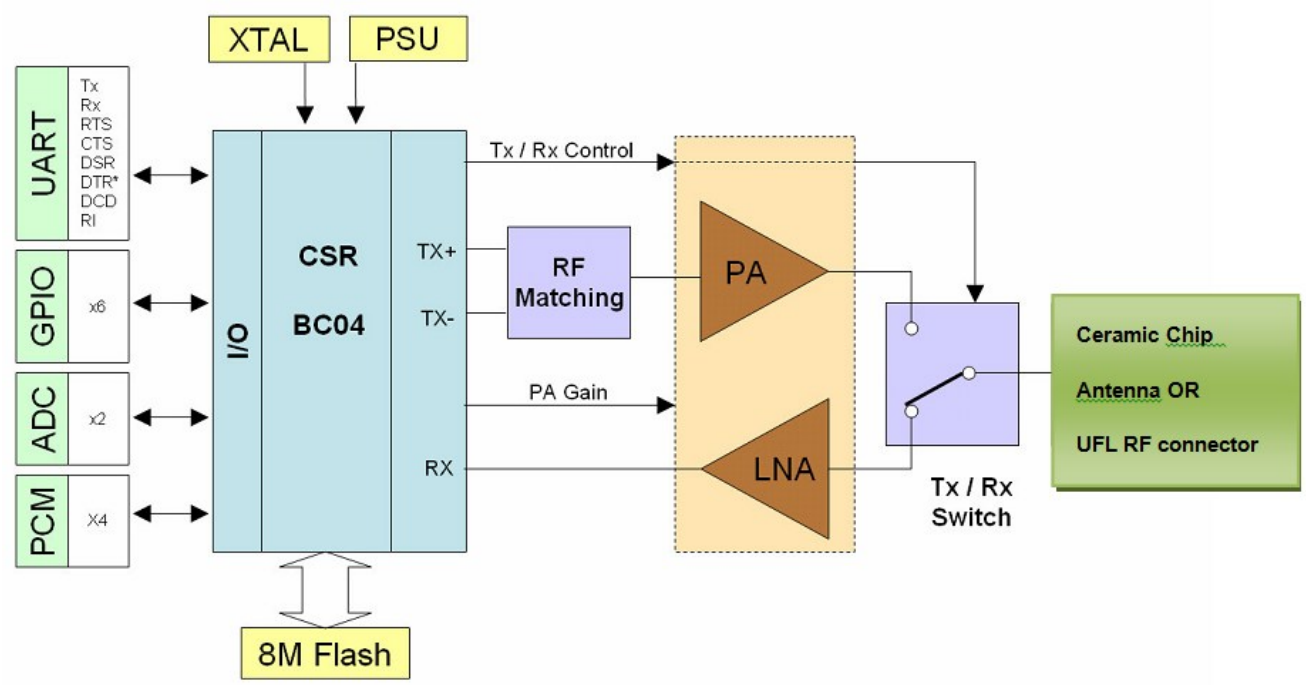


Figure 3-1: Functional Block Diagram

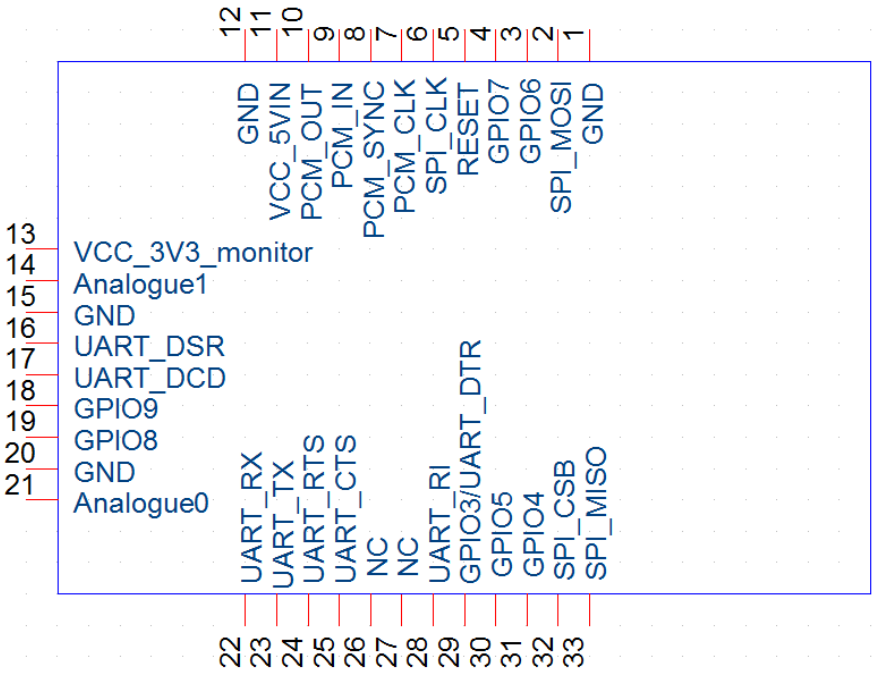


Figure 3-2: BT740-Sx module pin-out (Top View)

© Copyright 2025 Ezurio
All Rights Reserved

3.2 Pin Definitions

Table 3-1: Pin Definitions

Pin	Signal	Description	Comment
1	GND		
2	SPI_MOSI	SPI bus serial I/P	See Note 2
3	GPIO6	I/O for host	
4	GPIO7	I/O for host	
5	nRESET	Module reset I/P	See Note 3
6	SPI_CLK	SPI bus clock I/P	See Note 2
7	NC (PCM_CLK)	PCM clock I/P	See Note 6
8	NC (PCM_SYNC)	PCM sync I/P	See Note 6
9	NC (PCM_IN)	PCM data I/P	See Note 6
10	NC (PCM_OUT)	PCM Data O/P	See Note 6
11	VCC_IN	3.3 V < VCC_IN < 5.0 V	See Note 4
12	GND		
13	VCC_3V3_monitor	3.3 V Monitor (do not connect)	See Note 5
14	Analogue 1	1.8 V max	
15	GND		
16	UART_DSR	UART_DSR I/P	
17	UART_DCD	UART_DCD I/P or O/ P	
18	GPIO_9	I/O for host	
19	GPIO_8	I/O for host	
20	GND		
21	Analogue 0	1.8 V max	
22	UART_RX	Receive data I/P	See Note 7
23	UART_TX	Transmit data O/P	
24	UART_RTS	Request to Send O/P	
25	UART_CTS	Clear to Send I/P	See Note 7
26	NC (Reserved USB_D+)	Not used for AT module variants	
27	NC (Reserved USB_D-)	Not used for AT module variants	
28	UART_RI	Ring Input or Output	
29	GPIO_3/UART_DTR	I/O for host/UART_DTR	
30	GPIO_5	I/O for host	
31	GPIO_4	I/O for host	
32	SPI_CSB	SPI bus chip select I/P	See Note 2
33	SPI_MISO	SPI bus serial O/P	See Note 2

Notes:

1. Unused pins may have internal connections and must not be connected.
2. Pins 2, 6, 32, and 33 (SPI related) are only for Ezurio internal production purposes.

© Copyright 2025 Ezurio
All Rights Reserved

3. Power-on-reset (power cycling and brown out consideration) – The reset circuitry within the BT740 module incorporates a brown-out detector; this may simplify power supply design. The BT430 reset line is an active low input (Input debounced so must be low for more than 5 ms to cause a reset). Upon the application of power, the Power On Reset circuit built into the module ensures that the unit starts correctly. There is no need for an external power reset monitor.
4. Power Supply Consideration – The power supply for the module should be a single voltage source of VCC within the VCC_IN range of 3.3 V to 5.0 V. It must be able to provide sufficient current in a transmit burst. This can rise to 200 mA. To limit dissipation, it is recommended that you use a voltage at the lower end of the range.
5. The module includes regulators to provide internal local 3.3 V. This rail is accessible on pin 13 for monitoring purposes only. Under no circumstances should this pin be used to source current.
6. Pins 7, 8, 9 and 10 (PCM related) are NOT supported in Firmware therefore are NC (No Connect) pins.
7. Add a 10 k pull-up to the host PCB on the UART_RX, otherwise the module will remain in deep sleep if not driven to high. Add a 10 k pull-down to the host PCB on the UART_CTS that if it is not connected (which we do not recommend) then the default state for UART_CTS input will be asserted which means can send data out of UART_TX line.
8. GPIO lines can be configured through software to be either inputs or outputs with weak or strong pull-ups or pull-downs. At reset, all GPIO lines are configured as inputs with weak pull-downs.
9. UART_RX, UART_TX, UART_CTS, UART_RTS, UART_RI, UART_DCD, and UART_DSR are 3.3 V level logic. For example, when RX and TX are idle they sit at 3.3 V. Conversely, for handshaking pins CTS, RTS, RI, DCD, and DSR, a 0 V is treated as an assertion.
10. Pin 28 (UART_RI) is active low. It is normally 3.3 V. When a remote device initiates a connection, this pin goes low. This means that when this pin is converted to RS232 voltage levels it has the correct voltage level for assertion.
11. Pin 17 (UART_DCD) is active low. It is normally 3.3 V. When a connection is live, this pin is low. This means that when this pin is converted to RS232 voltage levels it has the correct voltage level for assertion.
12. Pin 16 (UART_DSR) is an input, with active low logic. It should be connected to the DTR output of the host. When the BTM740 module is in high speed mode (see S Register (in AT mode) in the Firmware User manual), this pin should be asserted by the host to ensure that the connection is maintained. A deassertion means that the connection should be dropped or an online command mode is being requested.
13. Pin 13 (VCC_3V3 monitor) may only be used for monitoring purposes. It must not be used as a current source.
14. The GPIO pins can be accessed using S Registers in AT mode and a special command in MP mode. See the Firmware User manual for S-register required.
15. GPIO3 is also used for DTR output (active low). See the Firmware User manual for S-register required.
16. Analogue 0 and 1 should not exceed 1.8 V and see the Firmware User manual for S-register used to access them.

© Copyright 2025 Ezurio
All Rights Reserved

3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analogue pins of the module are listed below.

WARNING: Exceeding the following values causes permanent damage to the device.

Parameter	Min	Max	Unit
Peak current of power supply	0	200	mA
Voltage at digital pins	-0.4	3.7	V
Voltage at POWER pin	2.9 *	6.0	V

3.3.2 Recommended Operating Parameters

3.3.2.1 Power Supply

Signal Name	Pin No	I/O	Voltage level	Comments
VCC_IN	11	I	3.0 V to 5.0 V * Typ 3.5 V	I_{typ} = 115 mA
GND	1, 12, 15, 20			Four (4) ground terminals to be attached in parallel.
VCC_3V3_monitor	13	O	3.3 V typical	For monitoring only. No current source

Note: VCC_3V3_monitor refers to internal voltage generated by the LDO inside the module which is typically 3.3 V. So to achieve 3.3 V for VCC_3V3_monitor (at Max Tx Power) requires VCC_IN of 3.5 V. IO voltage levels follows VCC_3V3_monitor. At minimum VCC_VIN of 3.3 V, the internal LDO generates 3.3 V but when Radio Tx at max Tx power, VCC_3V3_monitor drops a little (to ~3.15 V).

3.3.2.2 Signal Levels for Interface, GPIO (and SPI)

Signal Type	Signal level	Signal level at 0 mA load
Input	VILmin= -0.4V VILmax=0.8V VIHmin=2.3V VIHmax=3.7V	
Output		VOLmax=0.2V VOHmin=3.1V

3.3.2.3 UART Interface

Signal Name	Pin No	I/O	Comments
UART_TX	23	O	
UART_RX	22	I	
UART_CTS	25	I	
UART_RTS	24	O	
UART_DSR	16	I	
UART_DTR	29	O	Shared with GPIO3
UART_RI	28	I or O	Direction may be programmed.
UART_DCD	17	I or O	Direction may be programmed.

© Copyright 2025 Ezurio
All Rights Reserved

3.3.2.4 SPI Bus

Signal Name	Pin No	I/O	Comments
SPI_MOSI	2	I	INTERNAL USE ONLY - Used to reprogram Flash in Ezurio production.
SPI_MISO	33	O	
SPI_CSB	32	I	
SPI_CLK	6	I	

3.3.2.5 PCM Interface

Signal Name	Pin No	I/O	Comments
PCM_CLK	7	I or O	These pins are NO CONNECT as they are not supported in the Firmware.
PCM_IN	9	I	
PCM_SYNC	8	I or O	
PCM_OUT	10	O	

3.3.2.6 General Purpose I/O and ADC

Signal Name	Pin No	I/O	Signal level	Comments
GPIO_3 - 9	3, 4, 16, 17, 18, 19, 29, 30, 31	I or O	See Recommended Operating Parameters	
Analogue0, Analogue1	14, 21	I	Range 0 – 1.8 V	8 bit

3.3.2.7 nRESET

Signal Name	Pin No	I/O	Signal level	Comments
nRESET	5	I	V_{IL}max=1.0V V_{IH}min=2.3V	Active LOW. The Reset input contains a 10 kΩ pull-up resistor (internal to module).

© Copyright 2025 Ezurio
All Rights Reserved

4 I/O Characteristics

4.1 Power Consumption

The current drain from the VCC power input line is dependent on various factors. The three most significant factors are the voltage level at VCC, UART baud rate, and the operating mode. The hardware specification for the module allows for a voltage range of 3.3 to 5.0 at VCC. The unit includes a linear regulator and tests have shown that there is no significant difference in current draw when VCC changes within the operating limits. Tests have shown that where power dissipation is an issue, it is best to keep VCC at the lower end of the range.

The UART baud rate has a bearing on power dissipation because, as is normal for digital electronics, the power requirements increase linearly with increasing clocking frequencies. Because of this, higher baud rates result in a higher current drain.

The significant operating modes are:

- Idle
- Waiting for a connection
- Inquiring
- Initiating a connection
- Sniff
- Connected

With connected mode, it is also relevant to differentiate between no data being transferred and when data is being transferred at the maximum rate possible. The AT command set document describes how to configure the module for optimal power performance.

4.2 Typical Current Consumption in mA

Table 4-1: Current Consumption

VCC_IN = 3.8 V, Baudrate = 9600 bps Separation Distance = 15 meters (two BT740-SA)	Typical Average Current (mA)
Idle Mode, S512=1	1.25 mA
Wait for Connection Or Discoverable Mode, AT+BTP S508=S510=640, S509=S511=320	55 mA
Wait for Connection Or Discoverable Mode, AT+BTP S508=S510=1000, S509=S511=11	2.7 mA
Inquiry Mode, AT+BTI	65 mA
Connecting Mode (ATDxxx)	66 mA
Connected Mode (No Data Transfer)	6 mA
Connected Mode (Max Data Transfer)	35 mA
Sniff Mode S564=1000, S563=500, S562=50, S561=10	1.8 mA

© Copyright 2025 Ezurio
All Rights Reserved

5 Functional Description

The BT740 Bluetooth module is a self-contained Bluetooth product and requires only power to implement full Bluetooth communication. The integrated, high performance antenna, together with the RF and base-band circuitry provides the Bluetooth link and the UART interface provides a connection to the host system.

The variety of interfaces and the AT command set allow the BT740 module to be used for a wide number of long range wireless applications, from simple cable replacement to complex multipoint applications, where multiple radio links are active at the same time.

The complexity and flexibility of configuration are made simple for the design engineer by the integration of an extremely comprehensive set of AT commands, supplemented with a range of "S" registers which are used for non-volatile storage of system parameters.

To provide the widest scope for integration a range of different physical host interfaces are provided.

5.1 UART Interface

UART_TX, UART_RX, UART_RTS, and UART_CTS form a conventional asynchronous serial data port with handshaking. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signaling levels are nominal 0 V and 3.3 V, and are inverted with respect to the signaling on an RS232 cable. The interface is programmable over a variety of bitrates: no, even, or odd parity; stop bit; and hardware flow control. The default condition on power-up is pre-assigned in the external flash. UART_RTS and UART_CTS implement two-way hardware flow control. UART_RTS is an output and is active low. UART_CTS is an input and is active low.

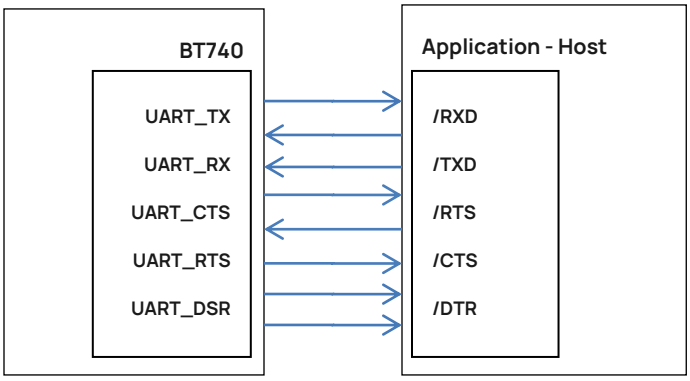
These signals operate according to normal industry convention. UART_RX, UART_TX, UART_CTS, UART_RTS, UART_RI, UART_DCD, and UART_DSR are all 3.3 V level logic. For example, when RX and TX idle, they sit at 3.3 V. Conversely for handshaking pins CTS, RTS, RI, DCD, and DSR, a 0 V is treated as an assertion.

By writing different values to the relevant S register the UART_RI can continuously poll to detect incoming communication. The UART_RI signal serves to indicate incoming calls.

- UART_DSR is an active low input. It should connect to the DTR output of the host. When the module runs in high speed mode (see definition of the required S-register in the Firmware User manual), this pin should assert by the host to ensure a connection maintains. A de-assertion means that the connection should be dropped, or an online command mode is being requested.

The module communicates with the customer application using the following signals:

- Port /TXD of the application sends data to the module's UART_RX signal line
- Port /RXD of the application receives data from the module's UART_TX signal line



Note: The serial module output is at 3.3 V CMOS logic levels. Level conversion must be added to interface with an RS232 level compliant interface.

Some serial applications link CTS and RTS to remove the need for handshaking. Ezurio doesn't recommend linking CTS and RTS other than for testing and prototyping. If these pins link and the host sends data at the point that the BT740 deasserts its RTS signal, there is significant risk that internal receive buffers will overflow and cause an internal processor crash. This also leads to a connection drop and may require a power cycle to reset. Ezurio recommends you follow the correct CTS/RTS handshaking protocol for proper operation.

© Copyright 2025 Ezurio
All Rights Reserved

5.2 SPI Bus

The module is a slave device that uses terminals SPI_MOSI, SPI_MISO, SPI_CLK, and SPI_CSB. This interface is used for program firmware updates ONLY at the factory. Ezurio supplies a PC-based utility to allow a firmware upgrade over the UART port. Ezurio highly recommends that customers use this method for updating firmware.

Note: The designer should be aware that no security protection is built into the hardware or firmware associated with this port, so the terminals should not permanently connect in a PC application.

5.3 PCM Interface

PCM is not supported in Firmware. PCM interface (PCM_OUT, PCM_IN, PCM_CLK, and PCM_SYNC) exists in HW only.

5.4 General Purpose I/O and ADC

5.4.1 GPIO

Seven lines of programmable bi-directional input/outputs (I/O) are provided that can be accessed either via the UART port or Over-the-Air (OTA) from a second Bluetooth unit. These can be used as data inputs or to control external equipment. By using these in OTA mode, a BT740 module can be used for control and data acquisition without the need for any additional host processor. Each of the GPIO[3:9] ports can be independently configured to be either an input or output. A selection of ports can be accessed synchronously.

The ports are powered from internal VCC_3V3. The mode of these lines can be configured and the lines are accessed via S Registers (see the Firmware User manual).

5.4.2 ADC

The BT740 provides access to two 8-bit ADCs (Analogue 0 and 1). These provide an input range of 0 mV to 1,800 mV, which are read using the S registers (see the Firmware User manual).

Suitable external scaling and over-voltage protection should be incorporated in your design. The module provides five samples per second at the UART with a baud rate of 115,200 or above.

1.1 BT740-SA On-board Chip Antenna Characteristics

The BT740-SA on-board chip monopole antenna radiated performance depends on the host PCB layout.

BT740 carrier board was used for BT740-SA development and antenna performance evaluation. To obtain similar performance, follow the guidelines in PCB Layout on Host PCB for BT740-SA to allow the on-board antenna to radiate and reduce proximity effects due to nearby host PCB GND copper or metal covers.

BT740-SA on-board antenna datasheet can be accessed from the following link:

http://www.acxc.com.tw/product/at3216/AT3216-B2R7HAA_071204.pdf

6 Hardware Integration Suggestions

6.1 Circuit

The BT740 series module is easy to integrate requiring no external components on the customer's board apart from those required by customer for development and in customers end application.

Checklist (for the schematic):

- **VCC_IN –** External power source within the operating range specification of BT740-Sx. Add decoupling (or bulk) capacitors for filtering (or reservoir) the external source. Power-on reset circuitry within BT740-Sx series module incorporates brown-out detector, thus simplifying power supply design. Upon application of power, the internal power-on reset ensures module starts correctly.
- **AIN (ADC) and GPIO (or UART) pin IO voltage levels –** BT73-Sx GPIO voltage levels are at 3.3V (see Notes). Electrical Specifications. Ensure input voltage levels into GPIO pins are at 3.3V voltage levels. Ensure ADC pin maximum input voltage (1.8 V) for damage is not violated.
- **UART –** Required. Add connector to allow UART to be interfaced to PC (via UART –RS232 or UART- USB).

© Copyright 2025 Ezurio
All Rights Reserved

- **UART_RX and UART_CTS –** Add a 10 k pull-up to the host PCB on the UART_RX, otherwise the module remains in deep sleep if not driven to high. The pull-up prevents the module from going into deep sleep when UART_RX line is idling.
- Add a 10 k pull-down to the host PCB on the UART_CTS that, if it is not connected (which we do not recommend) then the default state for UART_CTS input will be asserted which means can send data out of UART_TX line.
- **nRESET pin (active low)** – Hardware reset. Wire out to push button or drive by host. If used, the external reset must be exerted for a minimum of 5 mS. By default, the module is out of reset when power is applied to the VCC_IN pin.

6.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate the BT740-SA module close to the edge of PCB (mandatory for BT740-SA for on-board chips antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- Place GND vias as close to module GND pads as possible.
- Unused host PCB area on surface layer can be flooded with copper but place GND vias regularly to connect copper flood to inner GND plane. If GND flood copper underside the module then connect with GND vias to inner GND plane.
- Route traces to avoid noise being picked up on VCC_IN supply, Analogue and GPIO (digital) traces.
- Ensure there is no exposed copper on the underside of the module (refer to land pattern drawing of BT740-Sx).

6.3 PCB Layout on Host PCB for BT740-SA

6.3.1 Antenna keep-out on host PCB

The BT740-SA has an integrated chip antenna and its performance is sensitive to the host PCB. It is critical to locate the BT740-SA on the edge of the host PCB (or corner) to allow the antenna to radiate properly. Refer to guidelines in the section *PCB Land Pattern and Antenna Keep-out area for BT740-SA*. Some of the guidelines are repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the BT740-SA module on the edge of the host PCB, preferably in the corner with the antenna facing the corner. An example shown in Figure 6-1.
- A different host PCB thickness dielectric will have small effect on antenna (the BT740 carrier development board (used for antenna performance evaluation) thickness was 0.78 mm).
- The antenna-keep-out defined in *PCB Land Pattern and Antenna Keep-out area for BT740-SA* applies when the BT740-SA is placed in the corner of the host PCB. When BT740-SA cannot be placed as such, you must place it on the edge of the host PCB and use a modified antenna keep out. This antenna keep-out modification is shown in Figure 6-2 (antenna keep-out is extended by 8 mm on both sides).

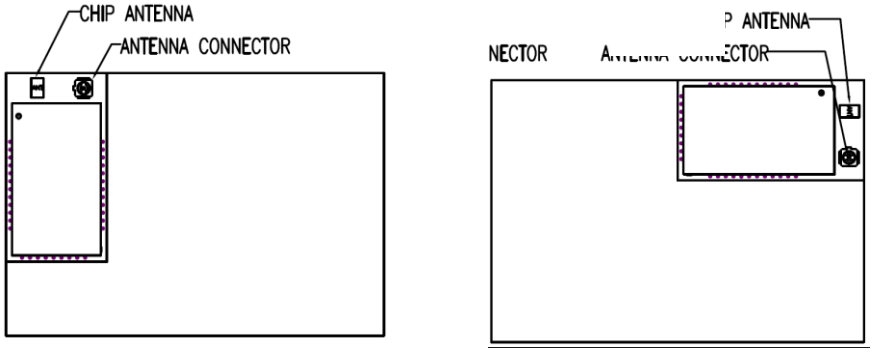


Figure 6-1: BT740-SA placement in the corner of host PCB.

© Copyright 2025 Ezurio
All Rights Reserved

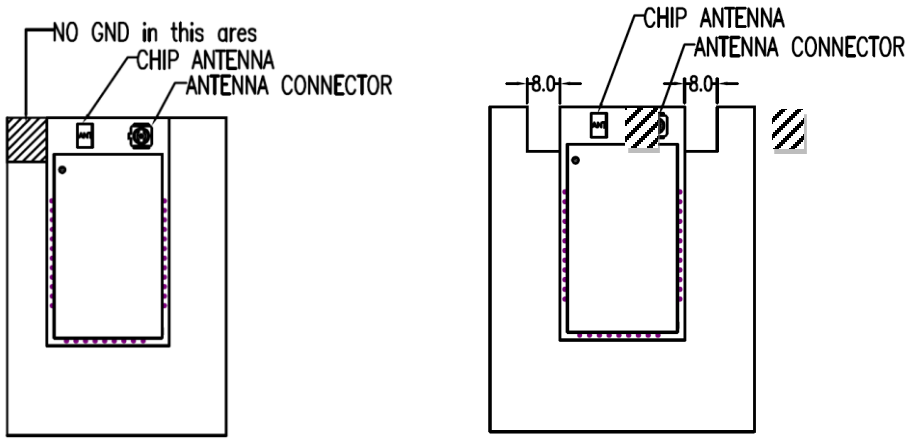


Figure 6-2: BT740-SA placement in the edge (not corner) of host PCB (with modified antenna keep-out).

Note: Copper cut-away on all layers in "antenna keep-out" area under BT740-SA module on host PCB. Refer to "antenna keep-out" defined in *7.4 PCB Land Pattern and Antenna Keep-out for BT740-SA*.

6.3.2 Antenna Keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Figure 12A and 12B shows recommended and not recommended locations for metal with respect to a BT740-SA module on-board antenna.
- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the BT740-SA chip monopole antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of degradation is entirely system dependent which means some testing by customer is required (in their host application).
- Anything metal closer than 20 mm starts to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that the customer tests the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and material, whether metal or plastic).

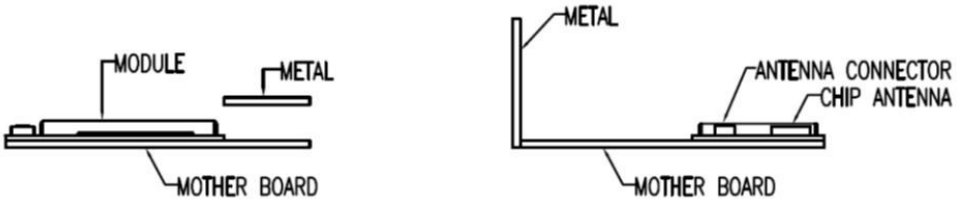


Figure 6-3: Recommended BT740-SA placement on host PCB and proximity to metal cover

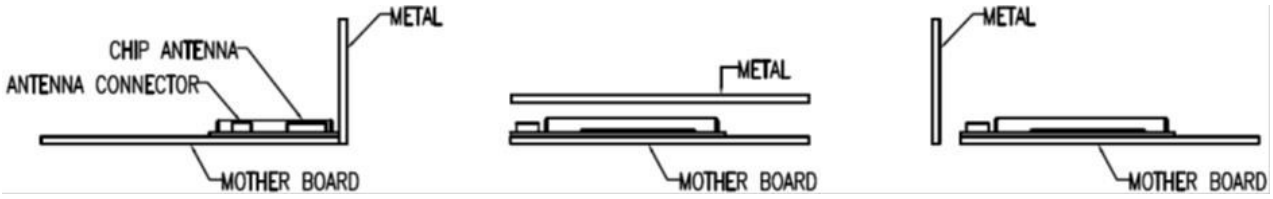


Figure 6-4: Not recommended BT740-SA placement on host PCB and proximity to metal cover

6.4 External Antenna Integration with BT740-SC

Refer to the regulatory sections for FCC, ISED, and the EU for details of use of BT740-SC with external antennas in each regulatory region.

The BT740-SC family has been designed to operate with the antennas listed below with a maximum gain of 2 dBi. The required antenna impedance is 50 ohms. External antennas improve radiation efficiency.

© Copyright 2025 Ezurio
All Rights Reserved

Item	Part Number	Mfg.	Type	Gain (dBi)	Connector Type
1	MAF94045	Ezurio (Laird Connectivity)	Internal	2	UFL
2	WRR2400- IP04-B(MAF94019)	Ezurio (Laird Connectivity)	Dipole	1.5	UFL
3	WTC2450-IP04-K(MAF94006)	Ezurio (Laird Connectivity)	Dipole	2	UFL
4	S181FL-L-RMM-2450S	Nearson (Laird)	Dipole	2	UFL

Note 1: Integral RF co-axial cable with UFL connector. Antenna manufacturer Ezurio contact information:
Email: support@ezurio.com

7 Mechanical Details

7.1 BT740-SC Mechanical Details

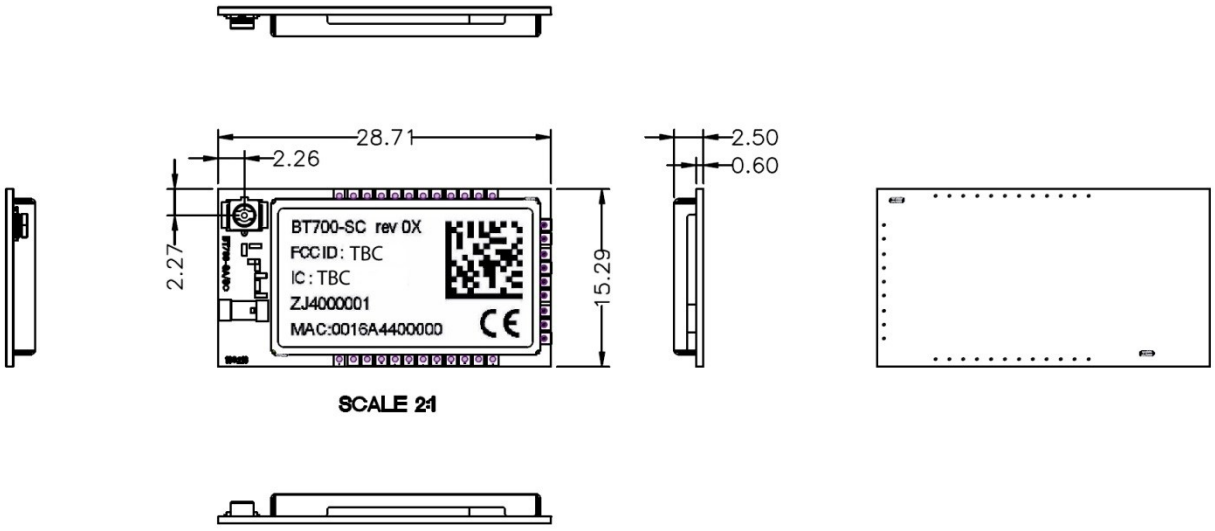


Figure 7-1: BT740-SC mechanical details

© Copyright 2025 Ezurio
All Rights Reserved

7.2 BT740-SA Mechanical Details

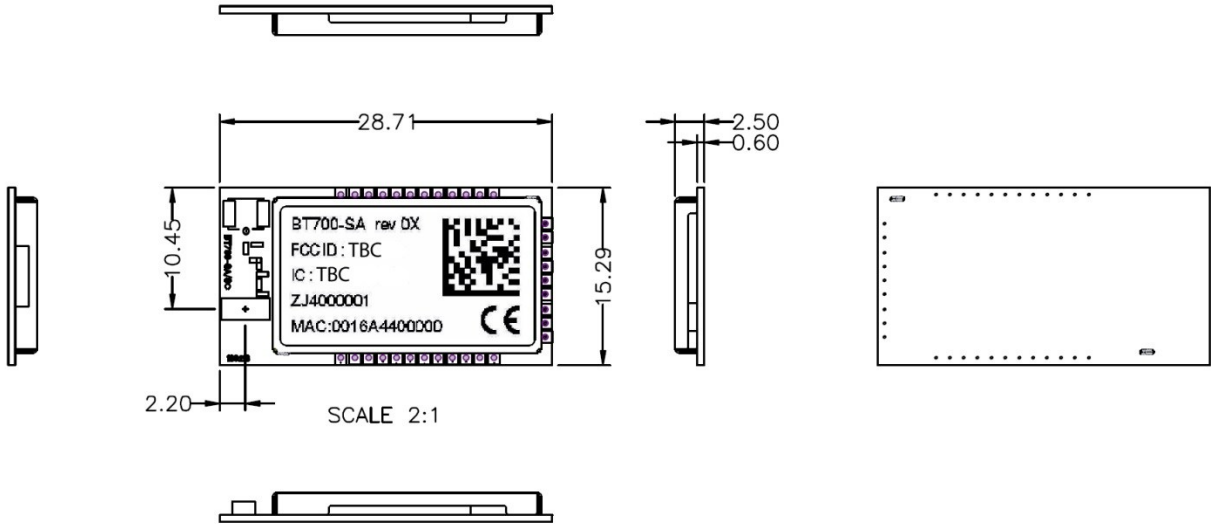
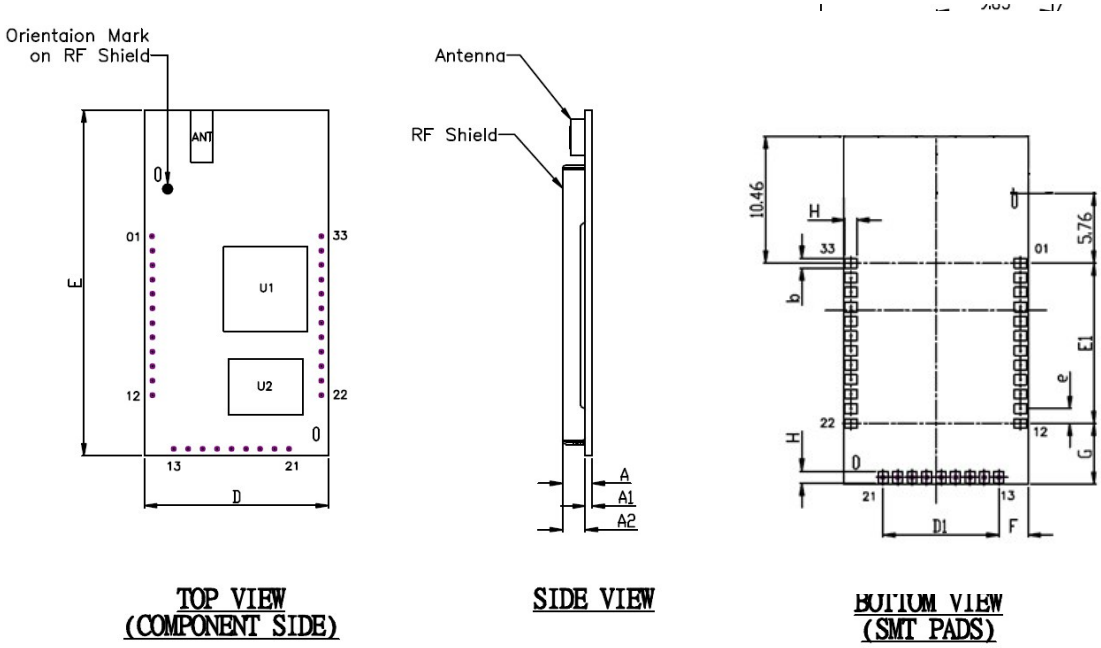


Figure 7-2: BT740-SA mechanical details

© Copyright 2025 Ezurio
All Rights Reserved

7.3 BT740 Pad Definitions – Mechanical Drawing



Description	BT-700			
Size	15.3 x 28.7 x 2.5 mm			
Pitch	1.2 mm			
Demension	Minimum	Typical	Maximum	Notes
A	2.3	2.5	2.7	
A1	0.5	0.6	0.7	PCB Thickness
A2	1.8	1.9	2.0	RF Shield Height
b	0.75	0.80	0.85	Global pad width
D	15.20	15.30	15.40	
E	28.60	28.70	28.80	
e		1.2		Global pitch
D1		9.6		
E1		13.2		
F		2.42		Pad Center to board edge
G		5.05		Pad Center to board edge
H		1.0		Global length of pad to edge of board
Units	mm			

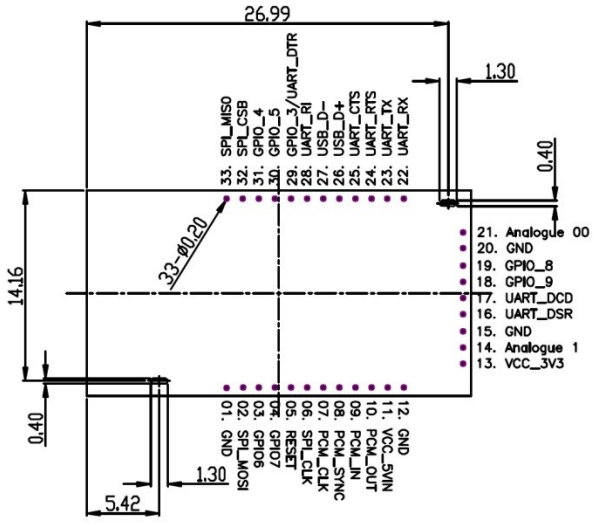


Figure 7-3: BT7xx Mechanical Drawing

© Copyright 2025 Ezurio
All Rights Reserved

7.4 PCB Land Pattern and Antenna Keep-out for BT740-SA

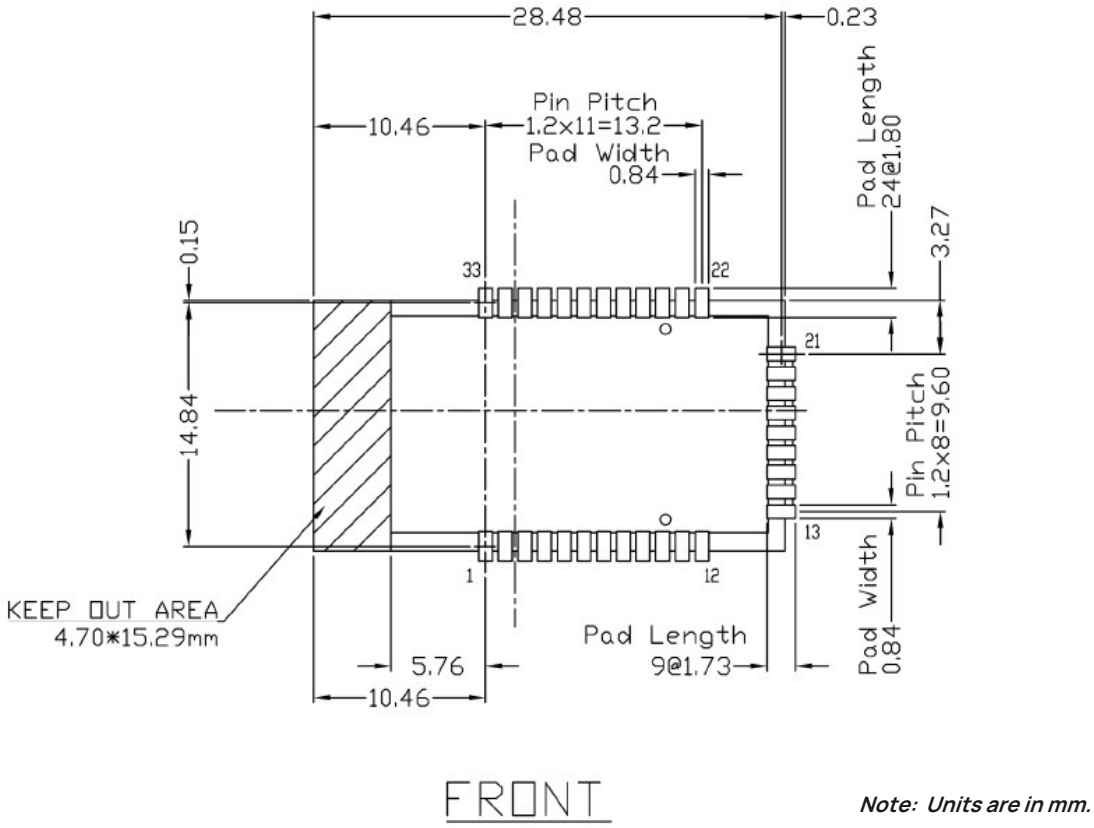


Figure 7-4: PCB Land Pattern and Antenna Keep-out for BT740-SA

APPLICATION NOTES

1. Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear of the area to reduce effects of proximity detuning the antenna and to help antenna radiate properly. Refer to section **6.3.2** for more information.
2. For BT740-SA (with on-board chip antenna) best antenna performance, the module BT740-SA ***must*** be placed on the edge of the host PCB, preferably in the **corner** with the antenna facing the corner (see Figure 6-1). The module is placed in the **corner** of host PCB above the keep-out area. If the BT740-SA is placed on the edge instead, the keep-out area must be modified (see Figure 6-2 in section 6.3.1).
3. Ensure that there is no exposed copper under the module on the host PCB.
4. The user may modify the PCB land pattern dimensions based on their experience and capability.

8 Surface Mount Modules

8.1 Introduction

Ezurio surface mount modules are designed to conform to all major manufacturing guidelines. This section provides additional guidance for mounting the module. This section is considered a living document and is updated as new information is presented.

The modules are designed to meet the needs of a number of commercial and industrial applications. The modules are designed to be easily manufactured and conform to current automated manufacturing processes.

© Copyright 2025 Ezurio
All Rights Reserved

8.2 Shipping

Modules ship in Electrostatic Discharge (ESD)-safe trays that can load into most manufacturers pick and place machines. Layouts of the trays are provided in Figure 8-1.

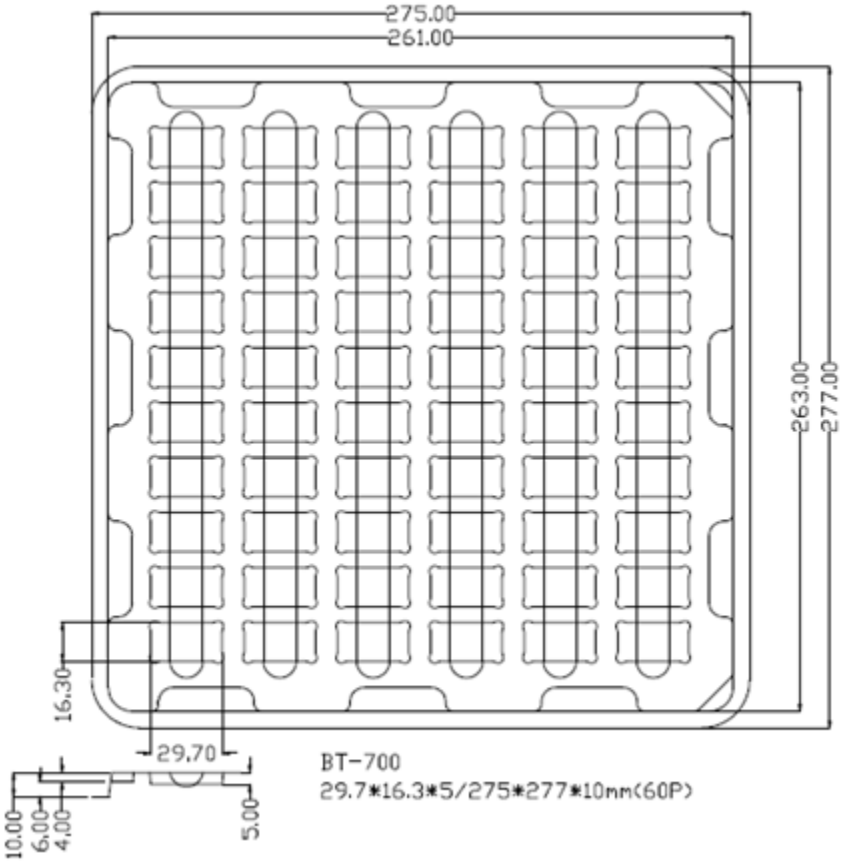


Figure 8-1: BT740 Shipping Tray Details

© Copyright 2025 Ezurio
All Rights Reserved

8.3 Reflow Parameters

Ezurio surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Ezurio's surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

Important: During reflow, modules should not be above 260° and not for more than 30 seconds.

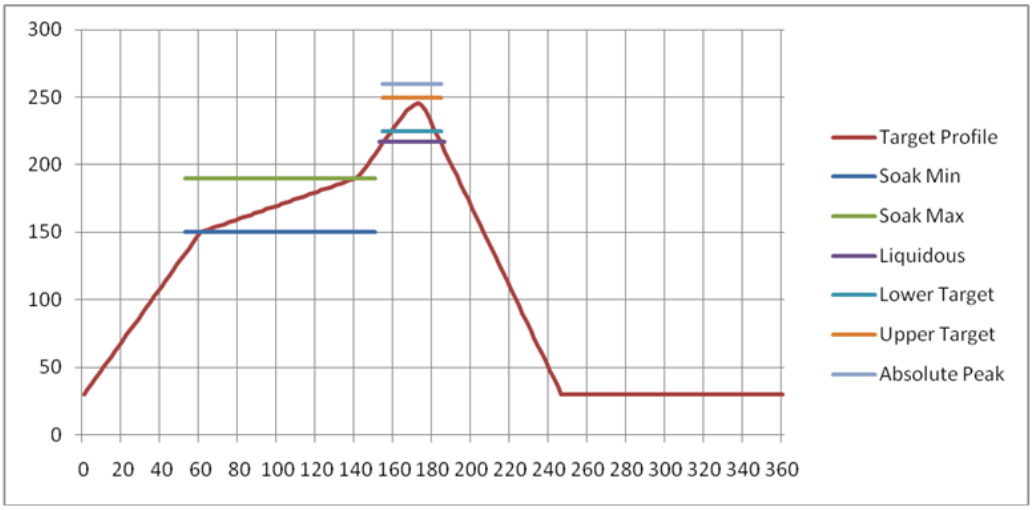


Figure 8-2: Recommended Reflow Temperature

Temperatures should not exceed the minimums or maximums presented in Table 8-1.

Table 8-1: Recommended Maximum and Minimum Temperatures

Specification	Value	Unit
Temperature Inc./Dec. Rate (max)	1~3	°C / Sec
Temperature Decrease rate (goal)	2-4	°C / Sec
Soak Temp Increase rate (goal)	.5 - 1	°C / Sec
Flux Soak Period (Min)	70	Sec
Flux Soak Period (Max)	120	Sec
Flux Soak Temp (Min)	150	°C
Flux Soak Temp (max)	190	°C
Time Above Liquidous (max)	70	Sec
Time Above Liquidous (min)	50	Sec
Time In Target Reflow Range (goal)	30	Sec
Time At Absolute Peak (max)	5	Sec
Liquidous Temperature (SAC305)	218	°C
Lower Target Reflow Temperature	240	°C
Upper Target Reflow Temperature	250	°C
Absolute Peak Temperature	260	°C

© Copyright 2025 Ezurio
All Rights Reserved

9 Regulatory

Note: For complete regulatory information, refer to the BT740 Regulatory Information document which is also available from the BT740 product page.

The BT740-SA/BT740-SC holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQGBT700
EU	N/A
Canada (ISED)	3147A-BT700

© Copyright 2025 Ezurio
All Rights Reserved

10 Bluetooth SIG Approvals

10.1 Overview

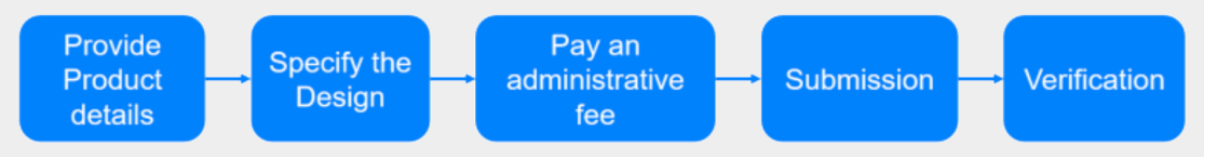
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

17. Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
18. Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

10.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference a single existing design, that has not been modified, (refer to Section 3.2.1 of the Qualification Program Reference Document v3).

This option applies to a Member qualifying a Product that includes an existing Design that has a DN, QDID, or DID and that Design has not been modified (e.g., rebranding a Qualified Product from another Member). The Design identified by the DN, QDID, or DID may only implement Bluetooth Specifications that are active or deprecated at the time of Submission. No modifications may be made to the Design, including changes to the ICS Form.

Changes to the Product outside the Design are allowed, including:

1. Enabling technologies
2. Changes to the industrial design
3. Changes to the communication technology other than Bluetooth
4. Changes to the features that are unrelated to Bluetooth, branding, packaging, colour, shape, Product name, or Model number

Members are responsible for assessing that modifications to the Product outside of the Design do not affect compliance with Bluetooth Specifications or result in a change to the ICS Form.

For the purposes of this document, it is assumed that the member is combining a single unmodified Core-Complete Configuration.

10.3 Qualification Steps When Referencing a single existing design, (unmodified) – Option 1 in the QPRDv3

For this qualification, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process.**
3. Product Details to be entered:
   - Project Name (this can be the product name or the Bluetooth Design name).
   - Product Description
   - Model Number

© Copyright 2025 Ezurio
All Rights Reserved

- Product Publication Date (the product publication date may not be later than 90 days after submission)
- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
- If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the single DN or QDID used in your, (for Option 1 only one DN or QDID can be referenced)
   - Once the DN or QDID is selected it will appear on the left-hand side, indicating the layers covered by the design.
   - Select 'I'm finished entering DN's
   - What do you want to do next? Answer, 'Use this Design without Modification'
   - Save and go to Product Qualification Fee
5. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
6. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
7. Download Product and Design Details:
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

10.4 Example Designs for reference

The following gives an example of a design possible under option 1:

Ezurio End Product design using Nordic Component based design

BT7x0 Series	Ezurio	D049591	147394	https://qualification.bluetooth.com/ListingDetails/104900

10.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.
To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

© Copyright 2025 Ezurio
All Rights Reserved

11 Ordering Information

Part Number	Description
BT740-SA	Enhanced Class 1 Bluetooth V2.1 Module (internal antenna)
BT740-SC	Enhanced Class 1 Bluetooth v2.1 Module (uFL for external antenna)
DVK – BT740-SA	Development board with BT740-SA module soldered in place
DVK – BT740-SC	Development board with BT740-SC module soldered in place

© Copyright 2025 Ezurio
All Rights Reserved

12 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

Note: Information contained in this document is subject to change.

Ezurio's products are subject to standard Terms & Conditions.

© Copyright 2025 Ezurio All Rights Reserved. Any information furnished by Ezurio and its agents is believed to be accurate but cannot be guaranteed. All specifications are subject to change without notice. Responsibility for the use and application of Ezurio materials or products rests with the end user since Ezurio and its agents cannot be aware of all potential uses. Ezurio makes no warranties as to non-infringement nor as to the fitness, merchantability, or sustainability of any Ezurio materials or products for any specific or general uses. Ezurio or any of its affiliates or agents shall not be liable for incidental or consequential damages of any kind. All Ezurio products are sold pursuant to the Ezurio Terms and Conditions of Sale in effect from time to time, a copy of which will be furnished upon request. Nothing herein provides a license under any Ezurio or any third-party intellectual property right. Ezurio and its associated logos are trademarks owned by Ezurio and/or its affiliates.

© Copyright 2025 Ezurio
All Rights Reserved