Datasheet

Lyra S

Version 2.2

Revision History

Version	Date	Notes	Contributors	Approver
1.0	18 Feb 2022	Initial Release	Raj Khatri, Dave Drogowski	Jonathan Kaye
1.1	10 June 2022	Updates to 5 Reference Diagrams and added 5.3 Boot	Greg Leach, Raj Khatri, Dave Drogowski	Jonathan Kaye
1.2	30 Oct 2024	Updated Bluetooth SIG Qualification	Dave Drogowski	Jonathan Kaye
2.0	24 Jan 2025	Ezurio rebranding	Sue White	Dave Drogowski
2.1	10 Dec 2025	Added clarification and further details in section 5.1 "Network Co-Processor (NCP) Application with UART Host" covering the AT Interface application's use of and dependency on the 32.768 kHz (LXFO) crystal.	Florian Baumgartl, Greg Leach	
2.2	22 Dec 2025	Clarified MSL level to MSL 3.	Dave Drogowski	Jonathan Kaye

Contents

1 Introduction

The Lyra S is a module designed and built to meet the performance, security, and reliability requirements of battery powered IoT products running on Bluetooth networks.

Based on the EFR32BG22 SoC, the Lyra S enables Bluetooth® Low Energy connectivity while delivering best-in-class RF range and performance, future-proof capability for feature and OTA firmware updates, enhanced security features, and low energy consumption.

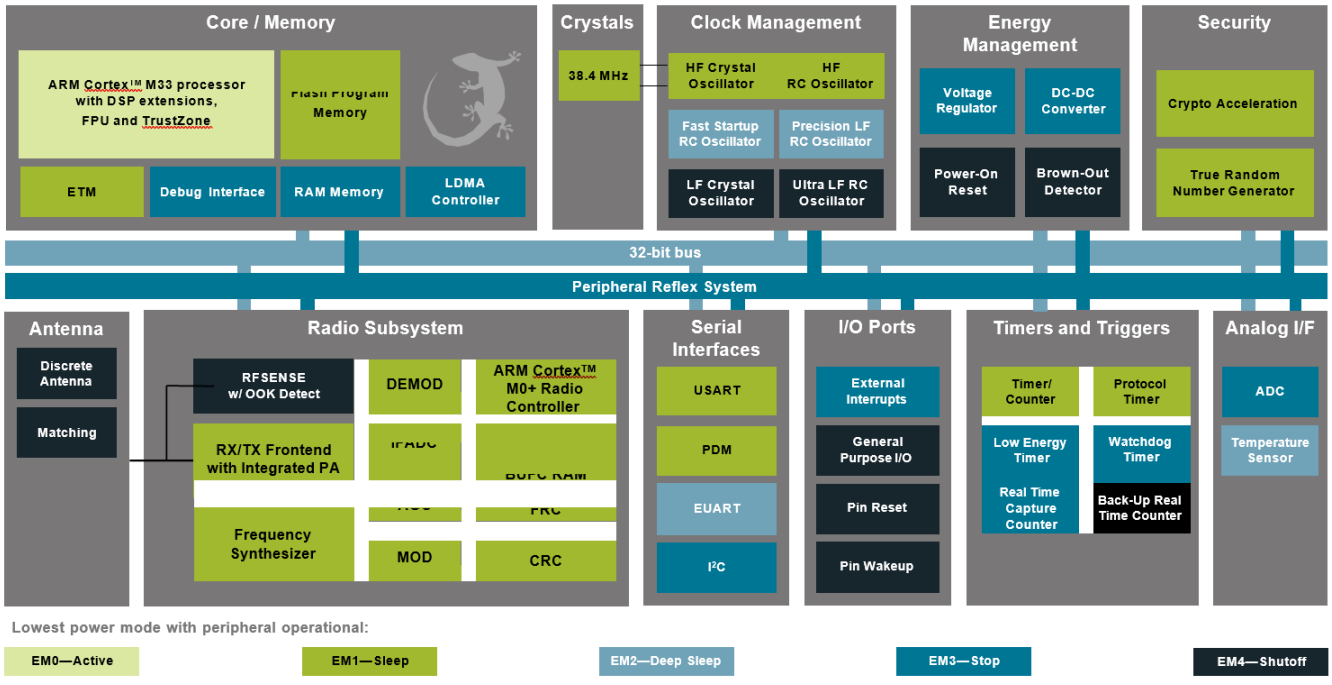
Lyra S modules are a full solution that comes with fully-upgradeable, robust software stacks, world-wide regulatory certifications, advanced development and debugging tools, and support that will minimize and simplify the engineering and development of your end-products helping to accelerate their time-to-market.

The Lyra S is intended for a broad range of applications, including:

- Asset Tags and Beacons
- Portable Medical
- Sports, Fitness, and Wellness devices
- Connected Home
- Industrial and Building Automation
- Bluetooth mesh Low Power Nodes

1.1 Key Features

- Bluetooth 5.3
- Built-in antenna or RF pin
- Up to 6 dBm TX power
- -98.6 dBm BLE RX sensitivity at 1 Mbps
- 32-bit ARM Cortex-M33 core at up to 76.8 MHz
- 512/32 kB of Flash/RAM memory
- Optimal selection of MCU peripherals
- 25 GPIO pins
- 6 mm × 6 mm × 1.1 mm



1.2 Hardware Features

- **Supported Protocols**
  - Bluetooth Low Energy (Bluetooth 5.3)
    - Direction finding
    - 1M, 2M, and LE Coded PHYs
    - Bluetooth Mesh Low Power Node
    - Wireless System-on-Chip
  - 2.4 GHz radio
  - TX power up to 6 dBm
  - High-performance 32-bit ARM Cortex-M33® with DSP instruction and floating-point unit for efficient signal processing
  - Up to 512 kB flash program memory
  - 32 kB RAM data memory
  - Embedded Trace Macrocell (ETM) for advanced debugging
- **High Receiver Performance**
  - -106.4 dBm sensitivity (0.1% BER) at 125 kbps GFSK
  - -102.3 dBm sensitivity (0.1% BER) at 500 kbps GFSK
  - -98.6 dBm sensitivity (0.1% BER) at 1 Mbps GFSK
  - -95.9 dBm sensitivity (0.1% BER) at 2 Mbps GFSK
- **Low-Energy Consumption**
  - 4.2 mA RX current at 1 Mbps GFSK
  - 4.6 mA TX current at 0 dBm output power
  - 26 µA/MHz in Active Mode (EM0)
  - 1.40 µA EM2 Deep Sleep current (RTCC running from LFXO, Full RAM retention)
- **Regulatory Certifications**
  - FCC
  - CE
  - IC/ISED
  - MIC/TELEC
  - KCC
- **Wide Operating Range**
  - 1.8 to 3.8 V
  - -40 to +105 °C
- **Dimensions**
  - 6 mm × 6 mm × 1.1 mm
- **Security Features**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock
- **Wide Selection of MCU Peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - 25 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 4 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 1 × Watchdog Timer
  - 2 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - 1 × Enhanced Universal Asynchronous Receiver/Transmitter (EUART)
  - 2 × I^2C interface with SMBus support
  - Digital microphone interface (PDM)
  - RFSENSE with selective OOK mode

1.3 Firmware Options

The Lyra series supports three different firmware options for software development:

AT Command Set – Fully featured and extensible to suit any developer's needs.

- Proven over 5+ years
- Basic Bluetooth LE cable replacement
- Simplest implementation possible
- Includes all key features of Wireless Xpress and more

Wireless Xpress – Frozen at current release, path for existing Silicon Labs customers

- Basic Bluetooth LE cable replacement
- Secure FOTA capable FW
- Xpress command API for iOS & Android

C Code – Full software development with Silicon Labs SDK and Toolchain

- Native C code development
- Use Simplicity Studio IDE
- Full functionality of Silicon Labs HW / SW

2 Ordering Information

Table 1: Ordering Information

Part	Description
453-00091R	Lyra Series - Bluetooth v5.3 SIP Module with antenna options (Silicon Labs EFR32BG22) - Tape / Reel
453-000091C	Lyra Series - Bluetooth v5.3 SIP Module with antenna options (Silicon Labs EFR32BG22) – Cut / Tape
453-00091-K1	Lyra Series - Development Kit - Bluetooth v5.3 SIP Module with antenna options

3 System Overview

3.1 Introduction

The Lyra S module combines an energy friendly MCU with a highly integrated radio transceiver in a SiP module with a robust, integrated antenna. This section gives a short introduction to the features of the module.

The block diagram for the Lyra S module is shown in the figure below. The wireless module includes the EFR32BG22 wireless System on a Chip (SoC), required decoupling capacitors and inductors, 38.4 MHz crystal, RF matching circuit, and integrated antenna.

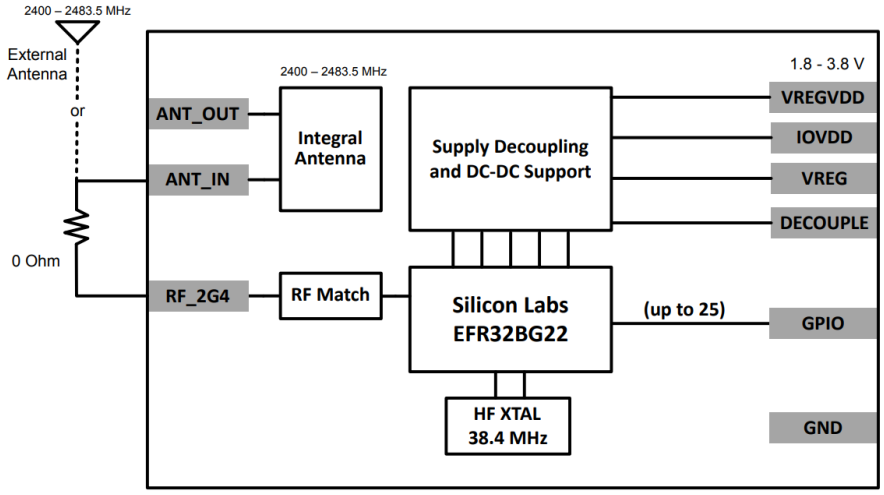


Figure 1: Lyra S

A simplified internal schematic for the Lyra S module is shown in the figure below.

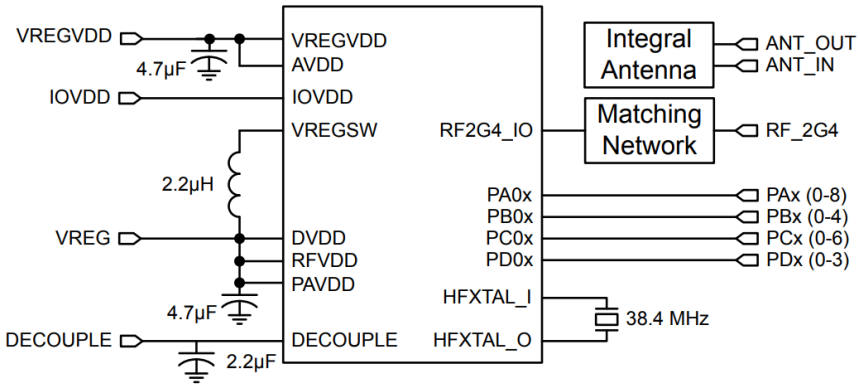


Figure 2: Lyra S Module Schematic

3.2 EFR32BG22 SoC

The EFR32BG22 SoC features a 32-bit ARM Cortex M33 core, a 2.4 GHz high-performance radio, 512 kB of flash memory, a rich set of MCU peripherals, and various clock management and serial interfacing options. Consult the EFR32xG22 Wireless Gecko Reference Manual and the EFR32BG22 Data Sheet for details.

3.3 Internal Antenna

Lyra S module includes an integral antenna on board with the characteristics detailed in the tables below.

Parameter	With optimal layout	Note
Efficiency	-1 to -2 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to Design Guidelines for recommendations to achieve optimal antenna performance.
Peak gain	2.3 dBi	

3.4 External Antenna

Lyra S module can be used with external antennas (certified by Ezurio) and requires a RF 50 Ohm track (Grounded Coplanar Waveguide) to be designed to run from Lyra S module RF_2G4 (pin3) to an RF antenna connector (IPEX MHF 4) on the host PCB. The 50Ohms RF track design and length MUST be copied as defined in section 7.6 Lyra S module 50Ohms RF track design for connecting external antenna.

The list of supported external antennas (certified by Ezurio) are in listed in section 7.7 External Antenna Integration with the Lyra S module.

3.5 Power Supply

The Lyra S requires a single nominal supply level of 3.0 V to operate. All necessary decoupling and filtering components are included in the module, and the supply is fully regulated internally.

4 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and VREGVDD supply at 3.0 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

4.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	+150	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Junction temperature	T_{JMAX}	-G grade	—	—	+105	°C
		-N grade	—	—	+105	°C
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
Input RF level on RF pin RF_2G4	$P_{RFMAX2G4}$		—	—	+10	dBm
Absolute voltage on RF pin RF_2G4	V_{MAX2G4}		-0.3	—	V_{VREG} + 0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

4.2 General Operating Conditions

This table specifies the general operating temperature range and supply voltage range for all supplies. The minimum and maximum values of all other tables are specified over this operating range, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-N temperature grade	-40	—	+105	°C
IOVDDx operating supply voltage (All IOVDD pins)	V_{IOVDDx}		1.71	3.0	3.8	V
VREGVDD operating supply voltage	$V_{VREGVDD}$	DCDC in regulation[1]	2.2	3.0	3.8	V
		DCDC in bypass	1.8	3.0	3.8	V
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	76.8	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2	—	—	50	MHz
		VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
EM01 Group B clock frequency	$f_{EM01GRPBCLK}$	VSCALE2	—	—	76.8	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency[2]	f_{RHCLK}	VSCALE2 or VSCALE1	—	38.4	—	MHz

Note:

1. The supported maximum $V_{VREGVDD}$ in regulation mode is a function of temperature and 10-year lifetime average load current. See more details in DC-DC Operating Limits.
2. The recommended radio crystal frequency is 38.4 MHz. Any crystal frequency other than 38.4 is expressly not supported.

4.2.1 DC-DC Operating Limits

The maximum supported voltage on the VREGVDD supply pin is limited under certain conditions. Maximum input voltage is a function of temperature and the average load current over a 10-year lifetime. Figure 3 shows the safe operating region under specific conditions. Exceeding this safe operating range may impact the reliability and performance of the DC-DC converter.

The average load current for an application can typically be determined by examining the current profile during the time the device is powered. For example, an application that is continuously powered which spends 99% of the time asleep consuming 2 µA and 1% of the time active and consuming 10 mA has an average lifetime load current of about 102 µA.

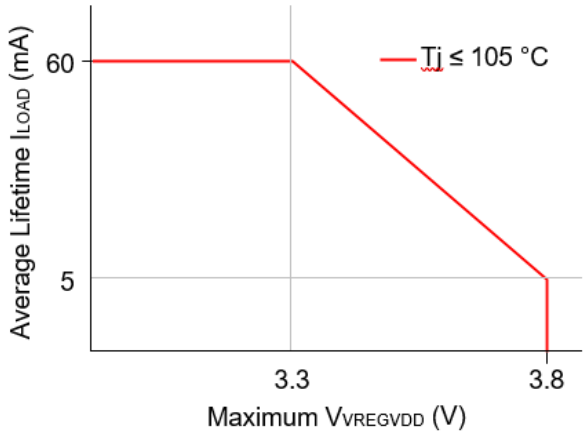


Figure 3: Lifetime average load current limit vs. Maximum input voltage

The minimum input voltage for the DC-DC in EM0/EM1 mode is a function of the maximum load current, and the peak current setting. Figure 4 shows the max load current vs. input voltage for different DC-DC peak inductor current settings.

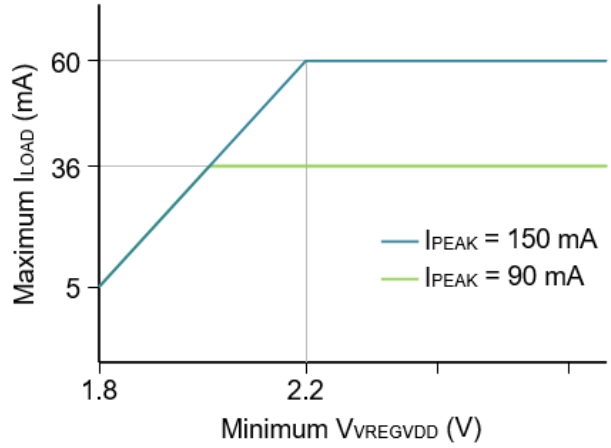


Figure 4: Transient maximum load current vs. Minimum input voltage

4.3 MCU Current Consumption with 3 V Supply

Unless otherwise indicated, typical conditions are: Module supply voltage = 3.0 V. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4: MCU Current Consumption with 3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	27	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	37	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	28	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	26	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	38	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	22	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	28	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	17	—	µA/MHz
		38.4 MHz crystal	—	17	—	µA/MHz
		38 MHz HFRCO	—	13	—	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.40	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.40	—	µA
		Full RAM retention and RTC running from LFRCO in precision mode	—	1.75	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.32	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	1.66	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.21	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.20	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.05	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, No LF Oscillator, DCDC bypassed	—	0.17	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.37	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See for a list of the peripherals in each power domain.

4.4 Radio Current Consumption with 3 V Supply

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 5: Radio Current Consumption with 3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System current consumption in receive mode, active packet reception	IRX_ACTIVE	125 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.8	—	mA
System current consumption in receive mode, listening for packet	IRX_LISTEN	125 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.3	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, Bluetooth stack running	—	4.7	—	mA
System current consumption in transmit mode	ITX	f = 2.4 GHz, CW, 0 dBm output power	—	4.6	—	mA
		f = 2.4 GHz, CW, 6 dBm output power	—	8.8	—	mA

4.5 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 6: RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Maximum TX power	$POUT_{MAX}$	6 dBm output power	—	6.0	—	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-27	—	dBm
Output power variation vs VREGVDD supply voltage variation, frequency = 2450 MHz	$POUT_{VAR\_V}$	6 dBm output power with VREGVDD voltage swept from 1.8 V to 3.0 V	—	0.04	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	$POUT_{VAR\_T}$	6 dBm output power, (-40 to +105 °C)	—	0.2	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	6 dBm output power	—	0.09	—	dB

4.6 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 7: RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

4.7 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 8: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-98.6	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-97.2	—	dBm
		With non-ideal signals[3 1]	—	-96.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	8.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-6.6	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-6.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-40.9	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-39.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-45.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-46.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-23.5	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-40.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-6.6	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-17.1	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -67 dBm.
5. Measured frequency is 2401 MHz ≤ Fc ≤ 2481 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.8 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 9: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-95.9	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-94.3	—	dBm
		With non-ideal signals[3 1]	—	-94.0	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	8.8	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-9.2	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-6.6	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1 5 4 6]	—	-43.3	—	dB
		Interferer is reference signal at -4 MHz offset[1 5 4 6]	—	-44.0	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1 5 4 6]	—	-48.6	—	dB
		Interferer is reference signal at -6 MHz offset[1 5 4 6]	—	-50.7	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-23.8	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1 6]	—	-43.3	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1 6]	—	-9.2	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-18.8	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -64 dBm.
5. Measured frequency is 2401 MHz ≤ Fc ≤ 2481 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.9 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 10: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload2	—	-102.3	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-100.9	—	dBm
		With non-ideal signals[3 1]	—	-99.8	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	2.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-8.0	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-7.9	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-46.5	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-49.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-48.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-53.8	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-48.3	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-49.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-46.5	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -72 dBm.
5. Measured frequency is 2401 MHz ≤ Fc ≤ 2481 MHz.
6. With allowed exceptions.

4.10 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V. RF center frequency 2.45 GHz.

Table 11: RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	SAT	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-106.4	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-106.0	—	dBm
		With non-ideal signals[3 1]	—	-105.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	0.9	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-13.6	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-13.4	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-52.6	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-55.8	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-53.7	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-59.0	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-52.7	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-53.7	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-52.6	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -79 dBm.
5. Measured frequency is 2401 MHz ≤ Fc ≤ 2481 MHz.
6. With allowed exceptions.

4.11 High-Frequency Crystal

Table 12: High-Frequency Crystal

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXTAL}		—	38.4	—	MHz
Initial calibrated accuracy	ACC_{HFXTAL}		-10	+/-5	10	ppm
Temperature drift	$DRIFT_{HFXTAL}$	Across specified temperature range	-20	—	20	ppm

4.12 Low Frequency Crystal Oscillator

Table 13: Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		–	32.768	–	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	–	–	80	kΩ
		GAIN = 1 to 3	–	–	100	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}	GAIN = 0	4	–	6	pF
		GAIN = 1	6	–	10	pF
		GAIN = 2	10	–	12.5	pF
		GAIN = 3 (see note[2])	12.5	–	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kOhm, CL = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	–	357	–	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kOhm, CL = 7 pF, GAIN[3] = 1, AGC[4] = 1	–	63	–	ms
On-chip tuning cap step size	SS_{LFXO}		–	0.26	–	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	–	4	–	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	–	24.5	–	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.13 Precision Low Frequency RC Oscillator (LFRCO)

Table 14: Precision Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		–	32.768	–	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode	-3	–	3	%
		Precision mode[1], across operating temperature range[2]	-500	–	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	–	204	–	µs
		Precision mode[1]	–	11.7	–	ms
Current consumption	I_{LFRCO}	Normal mode	–	175	–	nA
		Precision mode[1], T = stable at 25 °C [3]	–	655	–	nA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ± 40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.14 GPIO Pins

Unless otherwise indicated, typical conditions are: IOVDD = 3.0 V.

Table 15: GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71 V	–	1.9	–	nA
		MODEx = DISABLED, IOVDD = 3.0 V	–	2.5	–	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	–	–	0.3*IOVDD	V
		RESETn	–	–	0.3*DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7*IOVDD	–	–	V
		RESETn	0.7*DVDD	–	–	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05*IOVDD	–	–	V
		RESETn	0.05*DVDD	–	–	V
Output high voltage	V_{OH}	Sourcing 20mA, IOVDD = 3.0 V	0.8*OVDD	–	–	V
		Sourcing 8mA, IOVDD = 1.71 V	0.6*IOVDD	–	–	V
Output low voltage	V_{OL}	Sinking 20mA, IOVDD = 3.0 V	–	–	0.2*IOVDD	V
		Sinking 8mA, IOVDD = 1.71 V	–	–	0.4*IOVDD	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	–	8.4	–	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	–	13	–	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	–	7.1	–	ns
		IOVDD = 1.71 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	–	11.9	–	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	35	44	55	kΩ
		RESETn pin. Pull-up to DVDD	35	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	–	27	–	ns

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.15 Microcontroller Peripherals

The MCU peripherals set available in Lyra S modules includes:

- ADC: 12-bit at 1 Msps, 16-bit at 76.9 ksps
- 16-bit and 32-bit Timers/Counters
- 24-bit Low Energy Timer for waveform generation
- 32-bit Real Time Counter
- USART (UART/SPI/SmartCards/IrDA/I2S)
- EUART (UART/IrDA)
- I^2C peripheral interfaces
- PDM interface
- 12 Channel Peripheral Reflex System

For details on their electrical performance, consult the relevant portions of Section 4 in the SoC datasheet.

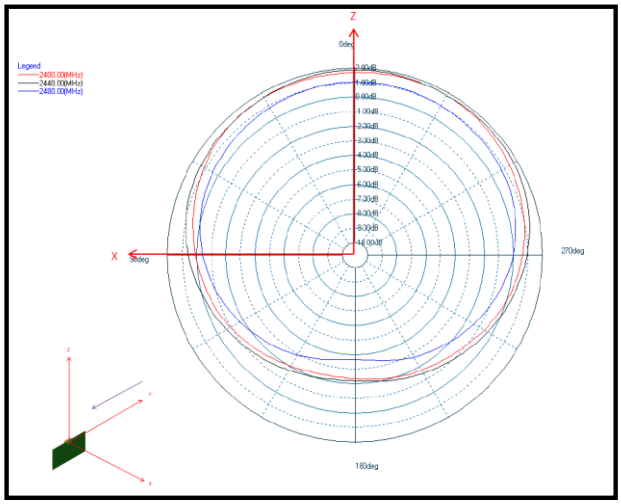
To learn which GPIO ports provide access to every peripheral, consult Analog Peripheral Connectivity and Digital Peripheral Connectivity.

4.16 Typical Performance Curves

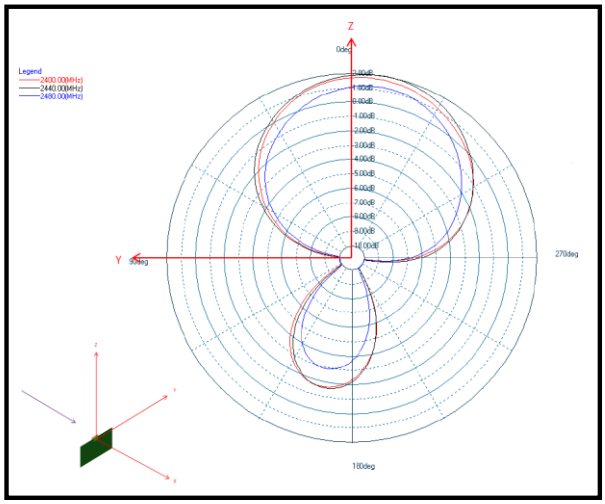
Typical performance curves indicate typical characterized performance under the stated conditions.

4.16.1 Internal Antenna Typical Characteristics

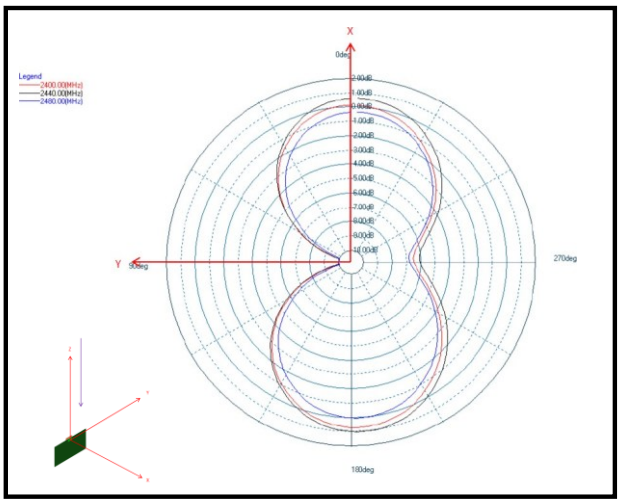
Typical Lyra S radiation patterns for the on-board chip antenna under optimal operating conditions are plotted in the figures that follow. Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna.



Phi 0^o



Phi 90^o



Theta 90°

Figure 5: Lyra S Internal Antenna Typical 2D Antenna Radiation Patterns on 55 mm x 20 mm board

5 Reference Diagrams

5.1 Network Co-Processor (NCP) Application with UART Host

The Lyra S can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug interface, and host interface connections are shown in the figure below. To use the AT Interface app, you must have the UART RTS and CTS pins connected, as the implementation relies on hardware flow control. It also requires a 32.768 kHz crystal to operate. Future GA releases may remove this dependency. On Lyra P, the LXFO is integrated into the module; however, on Lyra S, it is not included due to size constraints and must therefore be provided externally. As a result, our development board incorporates the XTL741-S999-498 (Siward) between PD00 and PD01. If adding a crystal isn't possible in your design, please reach out to your sales or FAE representative to obtain a firmware build that utilizes the LFRCO instead, with the trade-off being a small increase in power consumption.

Note: For boot pin, see section 5.3 Boot.

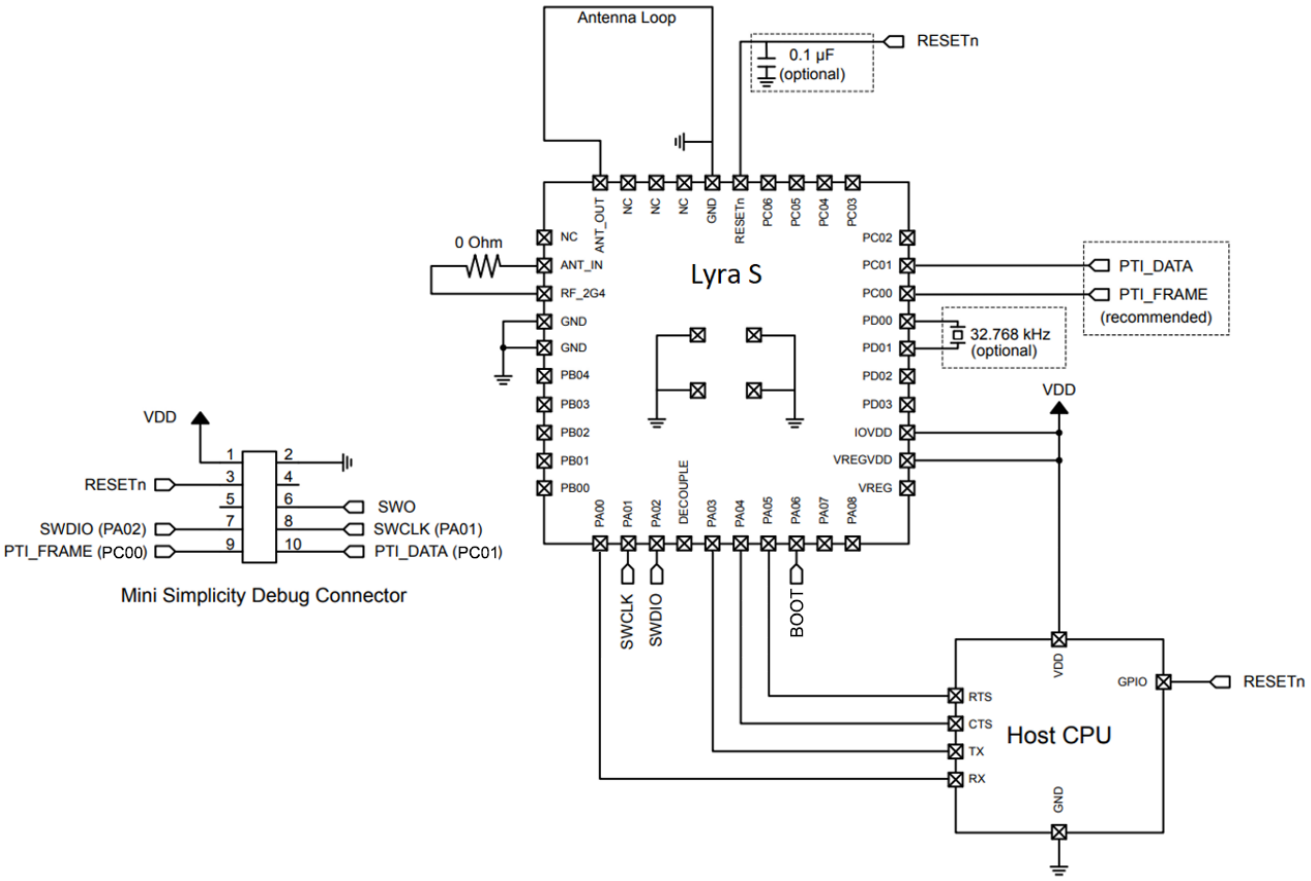


Figure 6: UART NCP Configuration

5.2 SoC Application

The Lyra S can be used in a stand-alone SoC configuration without an external host processor. Typical power supply and programming/debug interface connections are shown in the figure below.

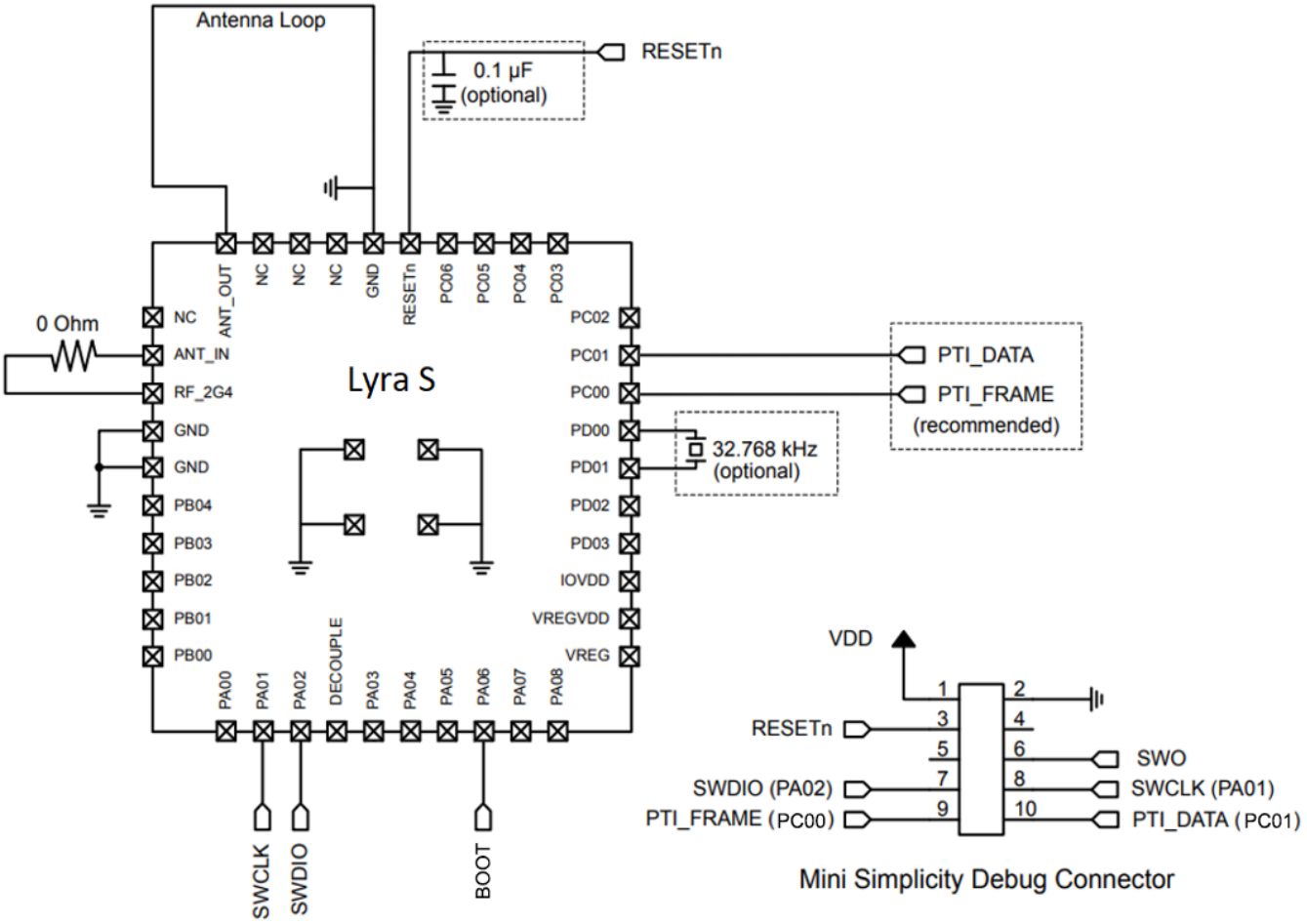


Figure 7: Stand-Alone SoC Configuration

5.3 Boot

The BOOT pin is used to determine when execution of the bootloader is required. Upon reset, execution of the bootloader begins. The state of the BOOT pin is read immediately upon start-up of the bootloader. If LOW, execution of the bootloader continues, facilitating firmware update via the UART. If the BOOT pin is HIGH, the bootloader will stop execution and pass control to the main application firmware.

6 Pin Definitions

6.1 Lyra S 44-Pin SiP Module Device Pinout

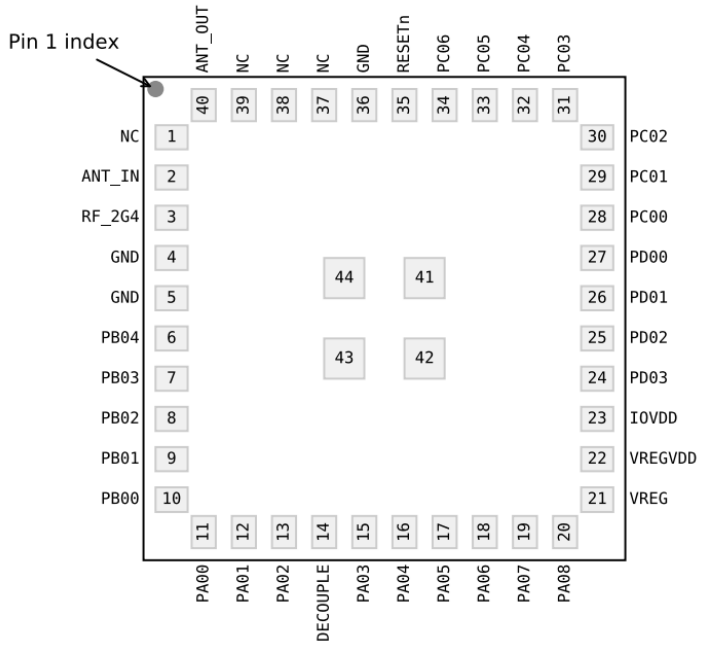


Figure 8: 44-Pin SiP Module Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see Alternate Function Table and Digital Peripheral Connectivity.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
NC	1	Do not connect	ANT_IN	2	Antenna In
RF_2G4	3	2.4 GHz RF input/output	GND	4	Ground
GND	5	Ground	PB04	6	GPIO
PB03	7	GPIO	PB02	8	GPIO
PB01	9	GPIO	PB00	10	GPIO
PA00	11	GPIO	PA01	12	GPIO
PA02	13	GPIO	DECOUPLE	14	Decouple output for on-chip voltage regulator. This pin is internally decoupled, and should be left disconnected.
PA03	15	GPIO	PA04	16	GPIO
PA05	17	GPIO	PA06	18	GPIO
PA07	19	GPIO	PA08	20	GPIO
VREG	21	Regulated supply voltage. This pin is internally connected to the SoC DVDD, RFVDD, and PAVDD supply lines. It is not intended to power external circuitry.	VREGVDD	22	Module input power supply. This pin is internally connected to the SoC AVDD and VREGVDD supply lines.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
IOVDD	23	I/O power supply	PD03	24	GPIO
PD02	25	GPIO	PD01	26	GPIO
PD00	27	GPIO	PC00	28	GPIO
PC01	29	GPIO	PC02	30	GPIO
PC03	31	GPIO	PC04	32	GPIO
PC05	33	GPIO	PC06	34	GPIO
RESETn	35	Reset Pin. The RESETn pin is internally pulled up to VREG (DVDD).	GND	36	Ground
NC	37	Do not connect	NC	38	Do not connect
NC	39	Do not connect	ANT_OUT	40	Antenna Out
GND	41	Ground	GND	42	Ground
GND	43	Ground	GND	44	Ground

6.2 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows what functions are available on each device pin.

GPIO	Alternate Functions	
PB03	GPIO.EM4WU4	
PB01	GPIO.EM4WU3	
PB00		IADC0.VREFN
PA00		IADC0.VREFP
PA01	GPIO.SWCLK	
PA02	GPIO.SWDIO	
PA03	GPIO.SWV GPIO.TDO GPIO.TRACEDATA0	
PA04	GPIO.TDI GPIO.TRACECLK	
PA05	GPIO.EM4WU0	
PD02	GPIO.EM4WU9	
PD01		LFXO.LFXTAL_I LFXO.LF_EXTCLK
PD00		LFXO.LFXTAL_O
PC00	GPIO.EM4WU6 GPIO.THMSW_EN	
PC05	GPIO.EM4WU7	

6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the

ODD pins. When a single ended connection is being used positive input is available on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals.

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port.

Table 16: DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUART0.CTS	Available	Available	Available	Available
EUART0.RTS	Available	Available	Available	Available
EUART0.RX	Available	Available	Available	Available
EUART0.TX	Available	Available	Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PDM.CLK	Available	Available	Available	Available
PDM.DAT0	Available	Available	Available	Available
PDM.DAT1	Available	Available	Available	Available
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		

7 Design Guidelines

7.1 Layout and Placement

For optimal performance of the Lyra S the following guidelines are recommended:

- Place the module 1.50 mm from the edge of the copper "keep-in" area at the middle of the long edge of the application PCB, as illustrated in Figure 9.
- Copy the exact antenna design from Figure 9 with the values for coordinates A to L given in Figure 10.
- Make a cutout in all lower layers aligned with the right edge and the bottom edge of the antenna as indicated by the yellow box in Figure 11.
- Connect all ground pads directly to a solid ground plane in the top layer.
- Connect RF_2G4 to ANT_IN through a 0-ohm resistor (for using Lyra S module Internal Antenna. See section 7.6 Lyra S module 50Ohms RF track design for connecting external antenna for connecting Lyra S to an external antenna).
  - The 0-ohm gives the ability to test conducted and to evaluate the antenna impedance in the design.
- Place ground vias as close to the ground pads of the Lyra S as possible.
- Place ground vias along the antenna loop right and bottom side.
- Place ground vias along the edges of the application board.
- Do not place plastic or any other dielectric material in contact with the Internal antenna.
  - A minimum clearance of 0.5 mm is advised.
  - Solder mask, conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region.

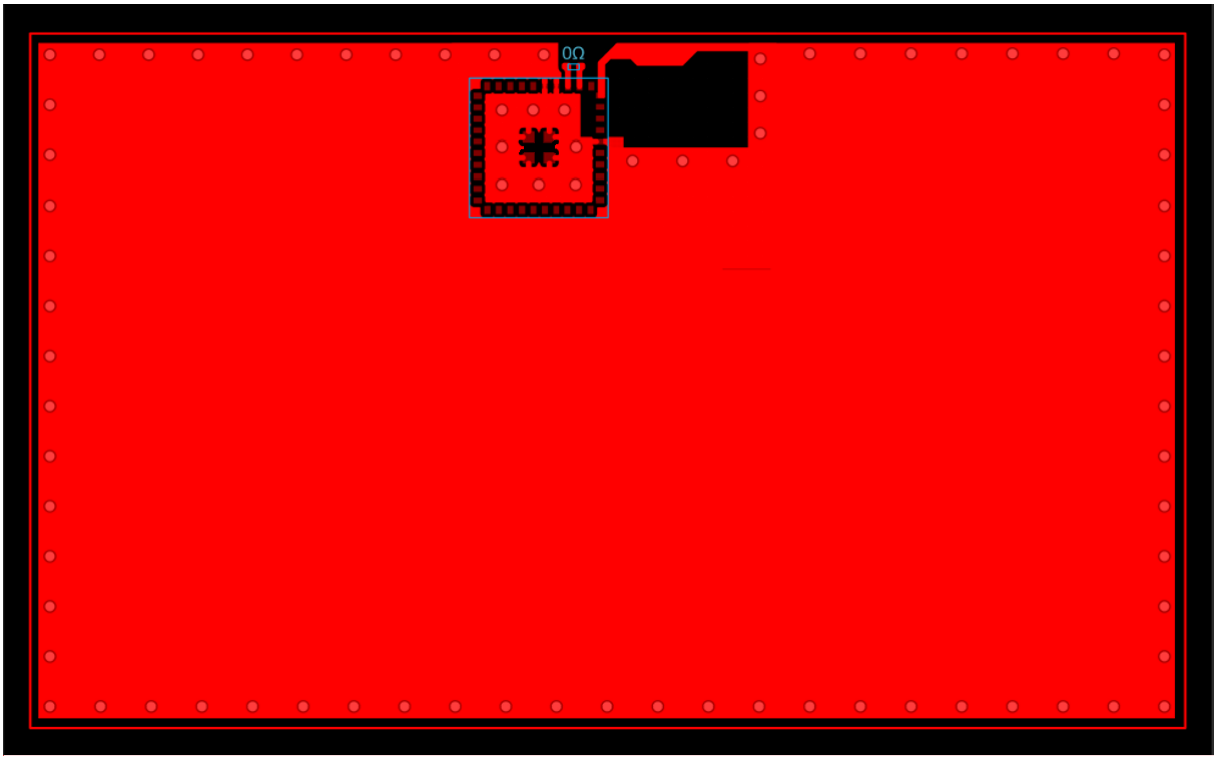


Figure 9: Recommended Layout for Lyra S

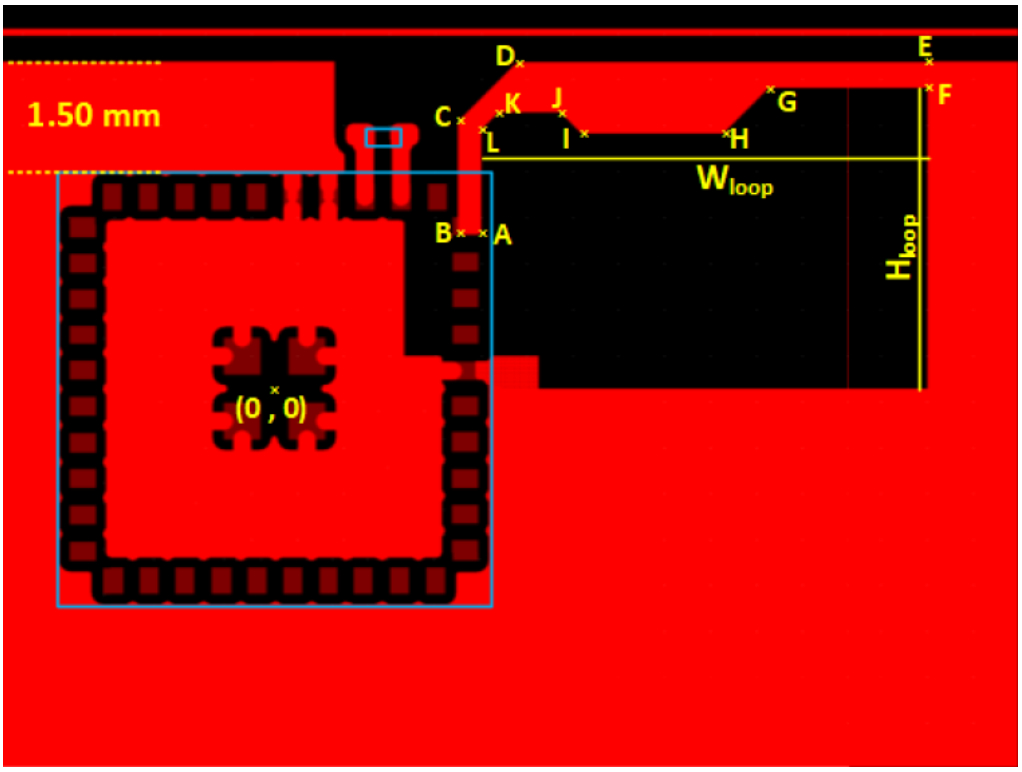


Figure 10: Internal Antenna Layout With Coordinates

Table 17: Antenna Polygon Coordinates, Referenced to Center of Lyra S

Point	Lyra S
A	(2.87, 2.13)
B	(2.54, 2.13)
C	(2.54, 3.69)
D	(3.36, 4.51)
E	(7.75, 4.51)
F	(7.75, 4.15)
G	(6.84, 4.15)
H	(6.21, 3.52)
I	(4.26, 3.52)
J	(3.97, 3.81)
K	(3.10, 3.81)
L	(2.87, 3.58)
W_{loop}	4.88
H_{loop}	4.15

Note:

1. All coordinates and dimensions listed in mm.

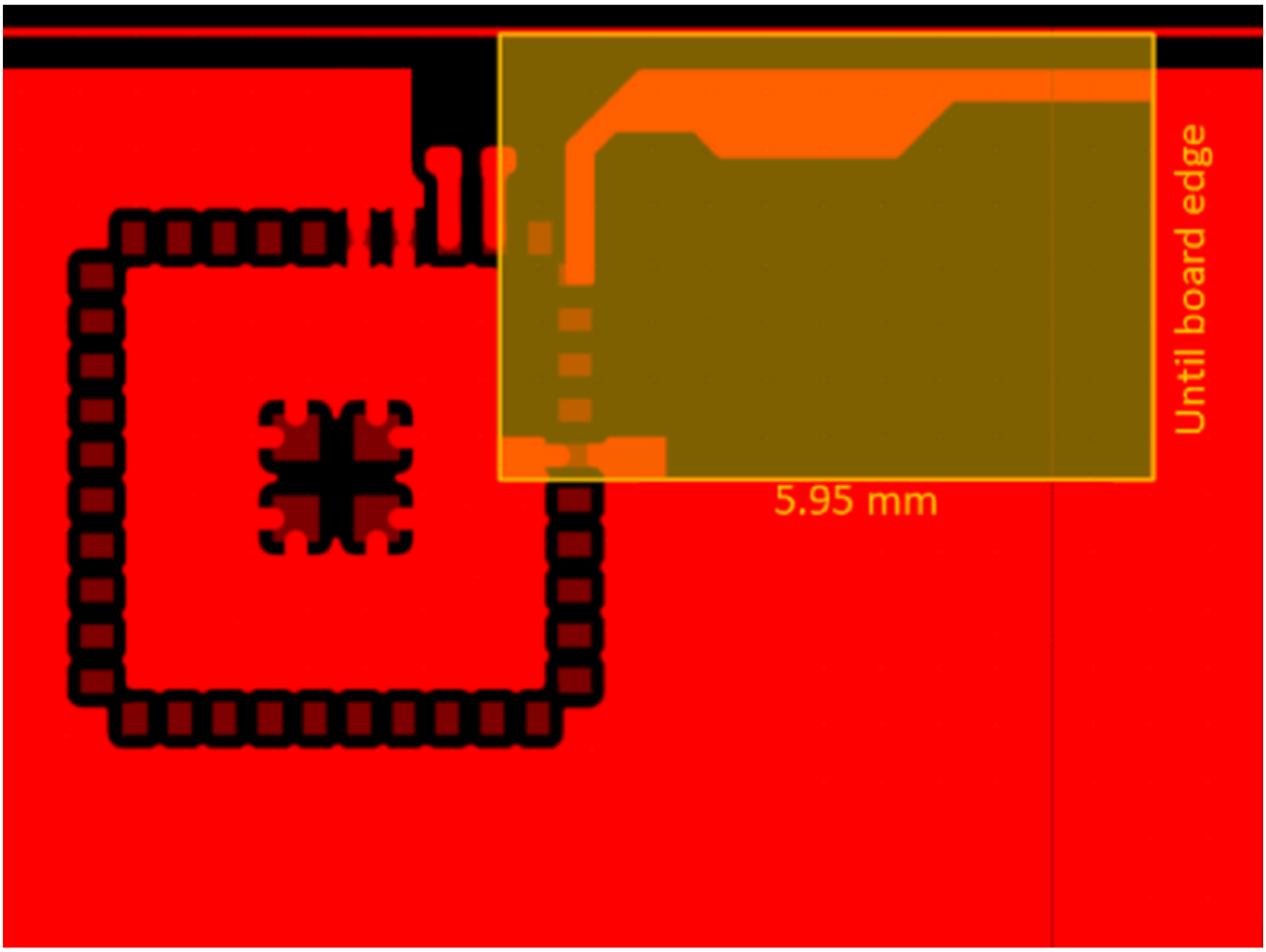


Figure 11: Antenna Clearance in Inner and Bottom Layers

7.2 Best Design Practices

The design of a good RF system relies on thoughtful placement and routing of the RF signals. The following guidelines are recommended:

- Place the Lyra S and antenna close to the center of the longest edge of the application board.
- Do not place any circuitry between the board edge and the antenna.
- Make sure to tie all GND planes in the application board together with as many vias as can be fitted.
- Generally ground planes are recommended in all areas of the application board except in the antenna keep-out area shown in Figure 11.
- Open-ended stubs of copper in the outer layer ground planes must be removed if they are more than 5 mm long to avoid radiation of spurious emissions.
- The width of the GND plane to the sides of the Lyra S will impact the efficiency of the on-board chip antenna.
  - For optimal performance, a GND plane width of 55 mm for Lyra S22A is recommended as seen on Figure 12.
  - See Internal Antenna Typical Characteristics for reference.

Figure 13 illustrates non-optimal layout examples scenarios that will lead to severely degraded RF performance for the application board.

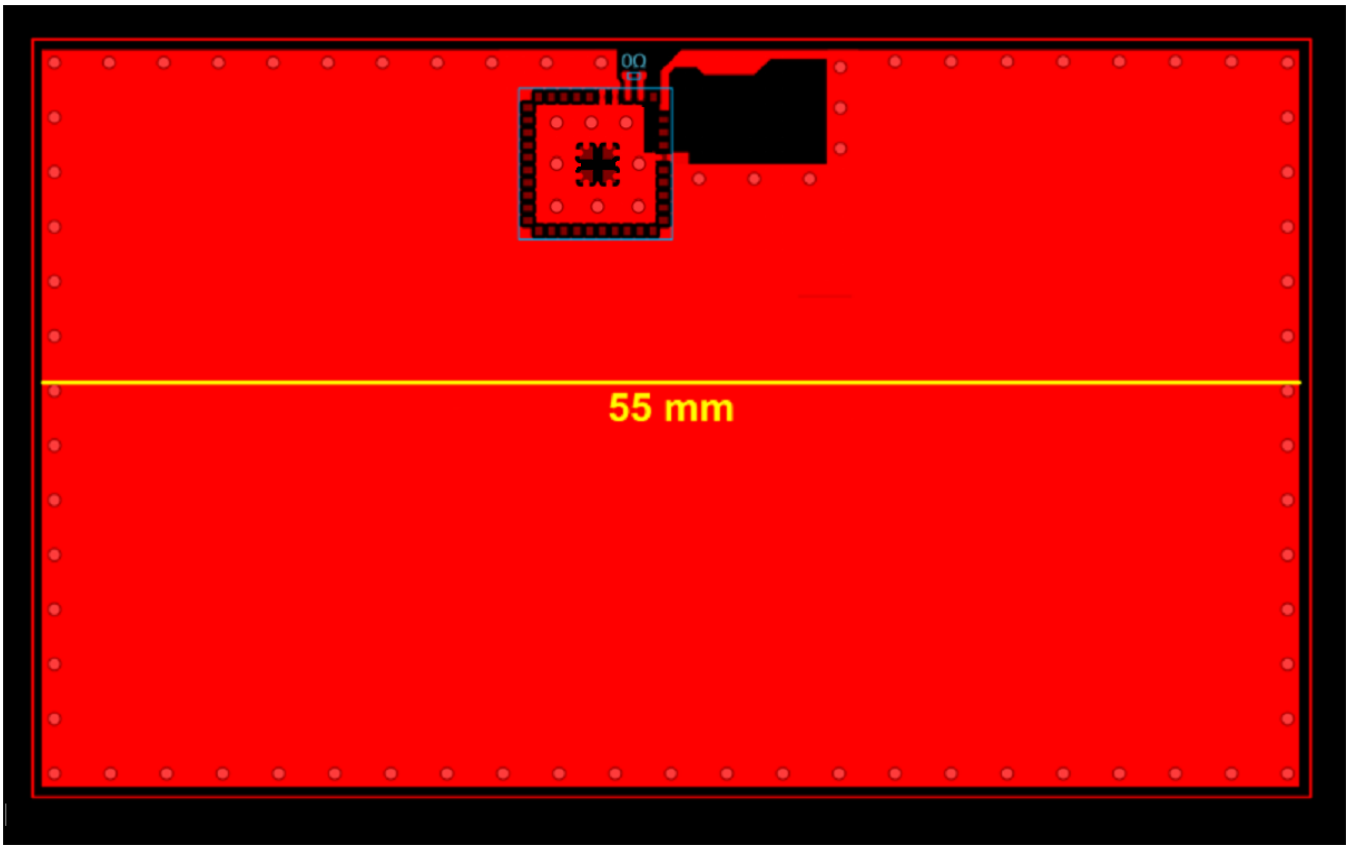


Figure 12: Illustration of Recommended Board Width

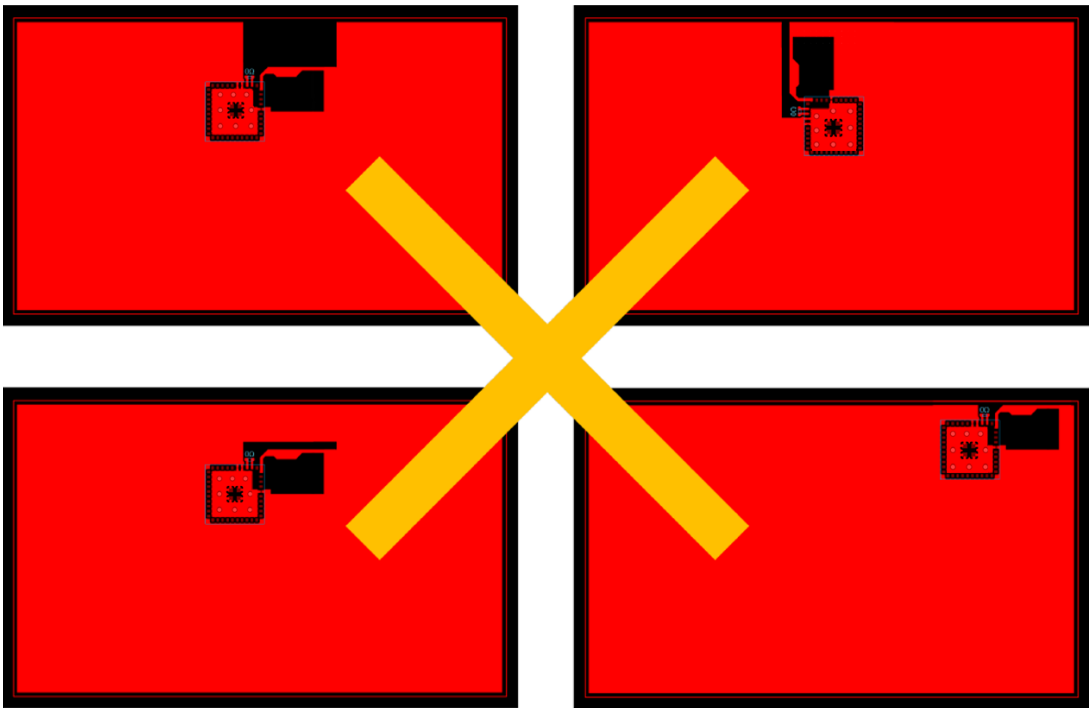


Figure 13: Non-Optimal Layout Examples

7.3 Internal Antenna Radio Performance vs. Carrier Board Size

For many applications, the carrier board size is determined by the overall form factor or size of the additional circuitry. The recommended carrier board width 55 mm for the Lyra S is thus not always possible in the end-application. If another form factor is required, the antenna performance of the integrated antenna will be compromised but it may still be sufficiently good for providing the required link quality and range of the end-application. Figure 14 shows the total efficiency of the integrated antenna for different carrier board sizes. As can be seen the best performance is achieved for the carrier board size of 55 mm x 25 mm for the Lyra S, with relatively constant performance for larger boards and rapidly declining performance for smaller boards.

The performance of all the sizes tested will be adequate for more than 15 m line-of-sight range and all of the sizes are thus usable.

WARNING: Any antenna tuning or change of the loop dimensions will void the modular certification of modules with modular certification. In that case, a Permissive Change to the modular approval is required.

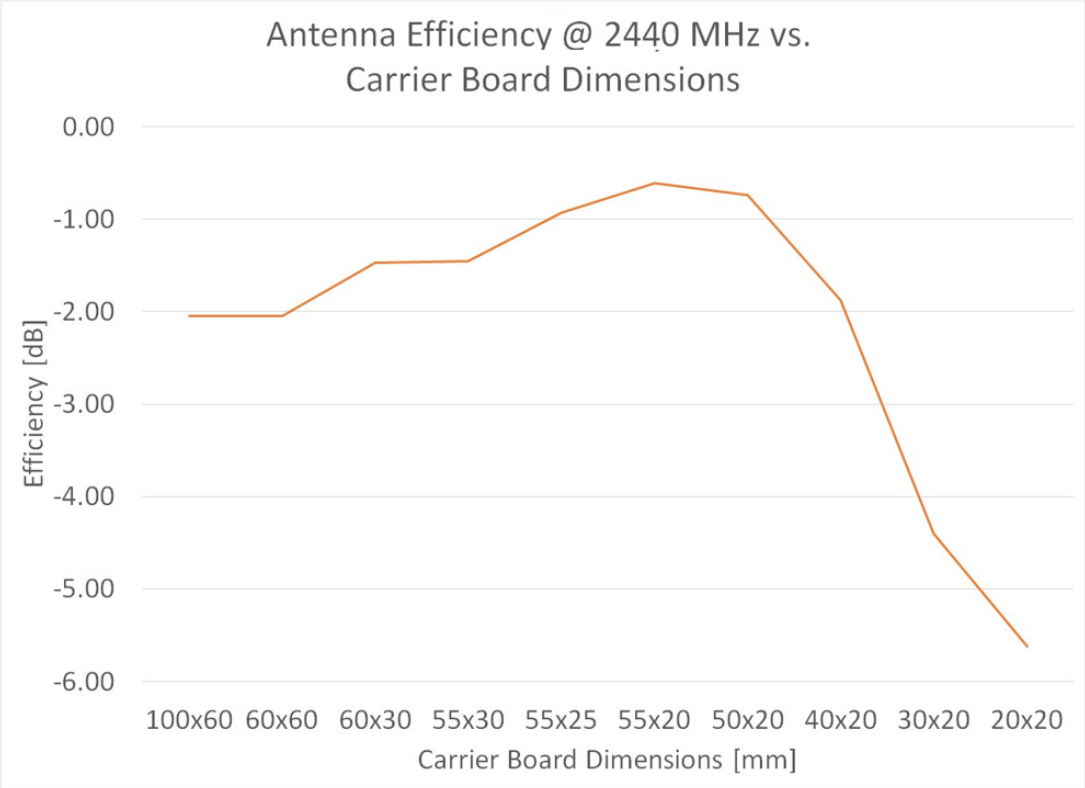


Figure 14: Efficiency of the Integrated Antenna as Function of the Carrier Board Size for Lyra S

7.4 Proximity to Other Materials

Placing plastic or any other dielectric material directly in contact with the antenna may cause performance degradation. A clearance of minimum 0.5 mm is recommended to avoid excessive detuning of the antenna. Solder mask, conformal coating, and other thin dielectric layers are acceptable directly on top of the antenna region. Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

7.5 Proximity to Human Body

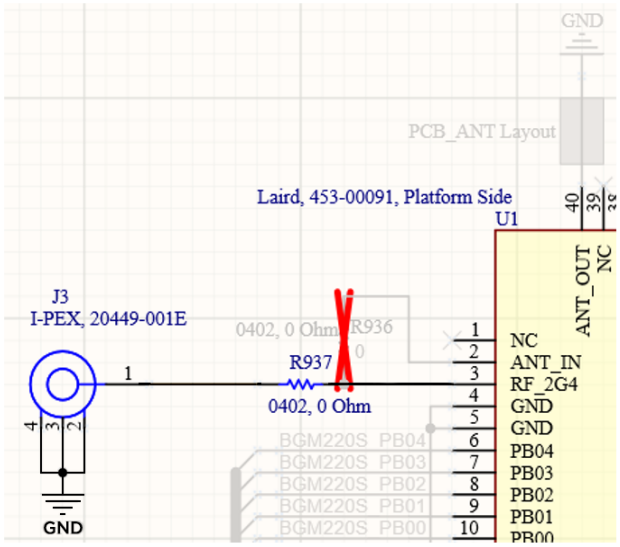
Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range. Furthermore, additional certification may be required if the module is used in a wearable device.

7.6 Lyra S module 50Ohms RF track design for connecting external antenna

Lyra S module can be used with external antennas (certified by Ezurio), and requires a 50 Ohm RF trace (GCPW, that Grounded Coplanar Waveguide) to be designed to run from Lyra S module RF_2G4 (pin3) to a RF antenna connector (IPEX MHF4) on host PCB. The 50 Ohms RF track design and length MUST be copied (as specified in this section). On the RF path, 0R series resistor connects Lyra S module RF_2G4 (pin3) to RF track. Lyra S module GND pin4 and GND pin5 used to support GCPW 50Ohm RF trace.

Checklist for SCH

Lyra S External antenna connection	Lyra S Internal antenna connection
1. Fit IPEX MHF4 RF connector (20449-001E) 2. Fit 0R resistor (position R937 in below SCH) between Lyra S module pin3 (RF_2G4) and IPEX MHF4 RF connector (20449-001E). 3. Leave Lyra S module pin2 (ANT_IN) open circuited.	1. Fit 0R resistor (position R936 in below SCH) between Lyra S module pin3 (RF_2G4) and pin2 (ANT_IN). 2. Do not Fit R937 and J3 (positions in below SCH). 3. Lyra S pin40 (ANT_OUT) internal antenna PCB layout MUST be followed.



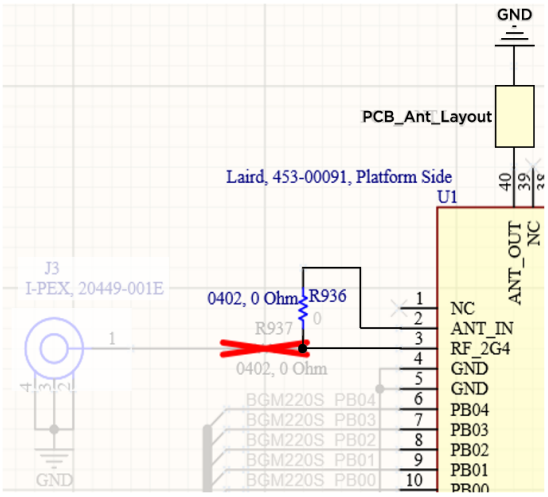
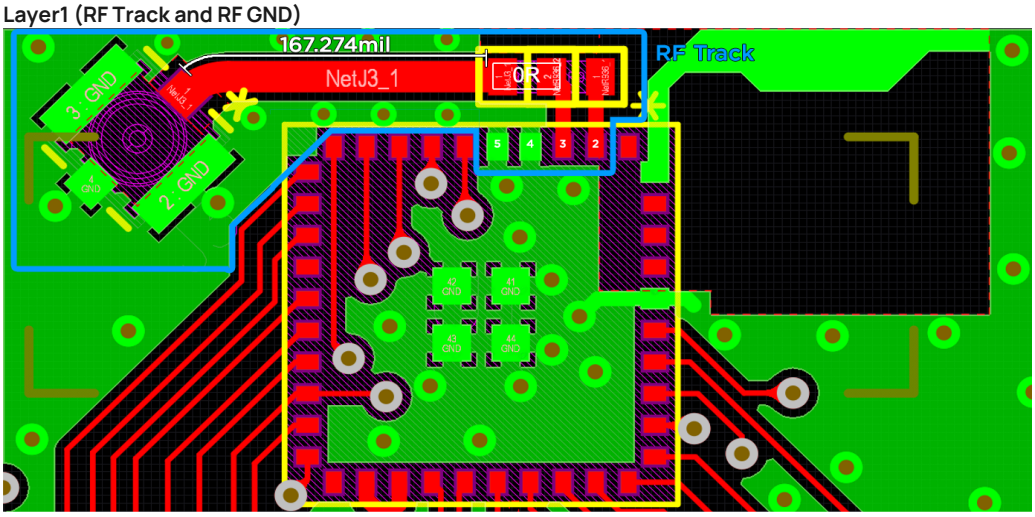


Figure 15: Lyra S for External antenna connection host PCB 50-Ohm RF trace schematic (0R resistor and RF connector)

Layer1 (RF Track and RF GND)



Layer2 (RF GND)

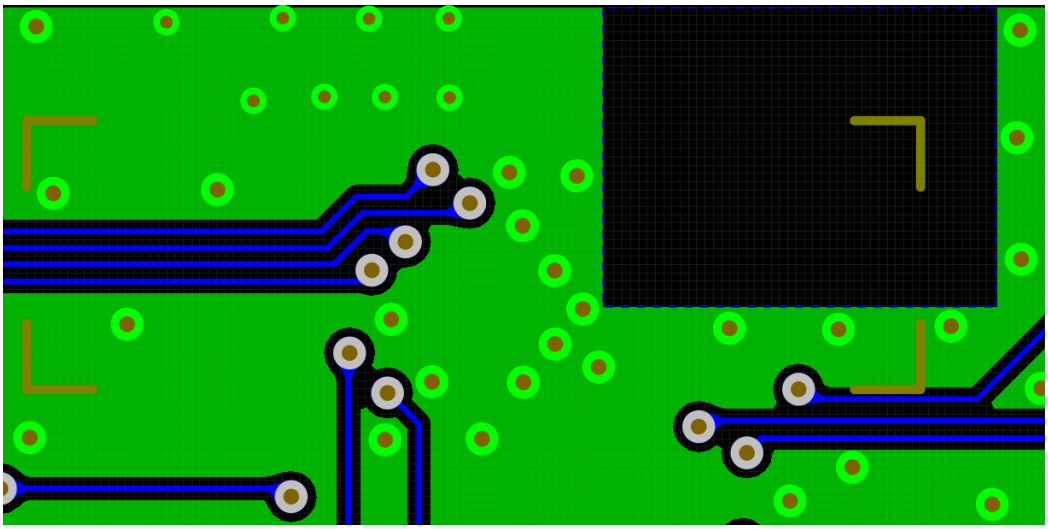
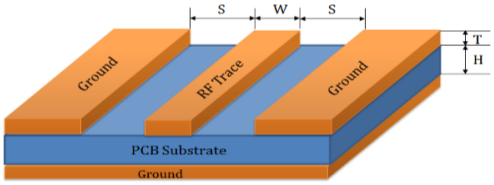


Figure 16: 50-Ohm RF trace design (Layer1 and Layer2) on DVK-Lyra S development board 453-00091-K1 (or host PCB) for use with Lyra S (453-00091) module

Checklist for PCB:

▪ MUST use a 50-Ohm RF trace (GCPW, that is Grounded Coplanar Waveguide) from RF_2G4 pad (pin3) of the Lyra S module (453-00091) to RF antenna connector (IPEX MHF4 Receptable (MPN: 20449-001E)) on host PCB.

▪ To ensure regulatory compliance, MUST follow exactly the following considerations for 50-Ohms RF trace design and test verification:



	Thickness mil	Dielectric Constant Er	
Solder Mask	1.18	3.5	Stack up for 50Ohms GCPW RF track.
Layer1 Copper 1oz+plating	1.3		
Core 0.6mm	59.06	4.2	
Layer2 Copper 1oz+plating	1.3		
Solder Mask	1.18	3.5	

Figure 17: Lyra S development board PCB stack-up and 50-Ohms Grounded CPW RF trace design using GND on L1 and L2

Note 1: The plating (ENIG) above base 1ounce copper is not listed, but plating expected to be ENIG.

- The 50-Ohms RF trace design MUST be Grounded Coplanar Waveguide (GCPW) with
  - Layer1 RF track width (W) of 20 mil and
  - Layer1 gap (S) to GND of 4.5 mil and where the
  - Layer1 to Layer 2 dielectric thickness (H) MUST be 59.06 mil (dielectric constant Er 4.2).
  - Further the Layer1 base copper must be 1-ounce base copper (that is 1.3 mil) plus the plating and
  - Layer1 MUST be covered by solder mask of 1.18 mil thickness (dielectric constant Er 3.5).
- The 50-Ohms RF trace design MUST follow the PCB stack-up shown in Figure 17. (Layer1 to Layer2 thickness MUST be identical to the Lyra S development board).
- The 50-Ohms RF track should be a controlled-impedance trace e.g., ±10%.
- The 50-Ohms RF trace length MUST be identical (as seen in Figure 16) (167.274mil) to that on the Lyra S development board from Lyra S module RF_2G4 RF pad (pin3) to the RF connector IPEX MHF4 Receptable (MPN: 20449-001E).
- Place GND vias regularly spaced either side of 50-Ohms RF trace to form GCPW (Grounded coplanar waveguide) transmission line as shown in Figure 16 and use Lyra S module GND pin4 and GND pin5.
- Use spectrum analyzer to confirm the radiated (and conducted) signal is within the certification limit.

7.7 External Antenna Integration with the Lyra S module

Please refer to the Lyra S Regulatory Information Guide for details on using Lyra S module with external antennas in each regulatory region.

The Lyra S has been designed to operate with the below external antennas (with a maximum gain of 2.0 dBi). The required antenna impedance is 50 ohms. See Table 18. External antennas improve radiation efficiency.

Table 18: External antennas for the Lyra S

Manufacturer	Model	Ezurio Part Number	Type	Connector	Peak Gain	
					2400-2500 MHz	2400-2480 MHz
Ezurio (Laird Connectivity)	NanoBlue	EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2 dBi	-
Ezurio (Laird Connectivity)	FlexPIFA	001-0022	PIFA	IPEX MHF4	-	2 dBi
Mag.Layers	EDA-8709-2G4C1-B27-CY	0600-00057	Dipole	IPEX MHF4	2 dBi	-
Ezurio (Laird Connectivity)	mFlexPIFA	EFA2400A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi

8 Mechanical Specifications

8.1 Package Dimensions

The package dimensions are shown in Figure 18.

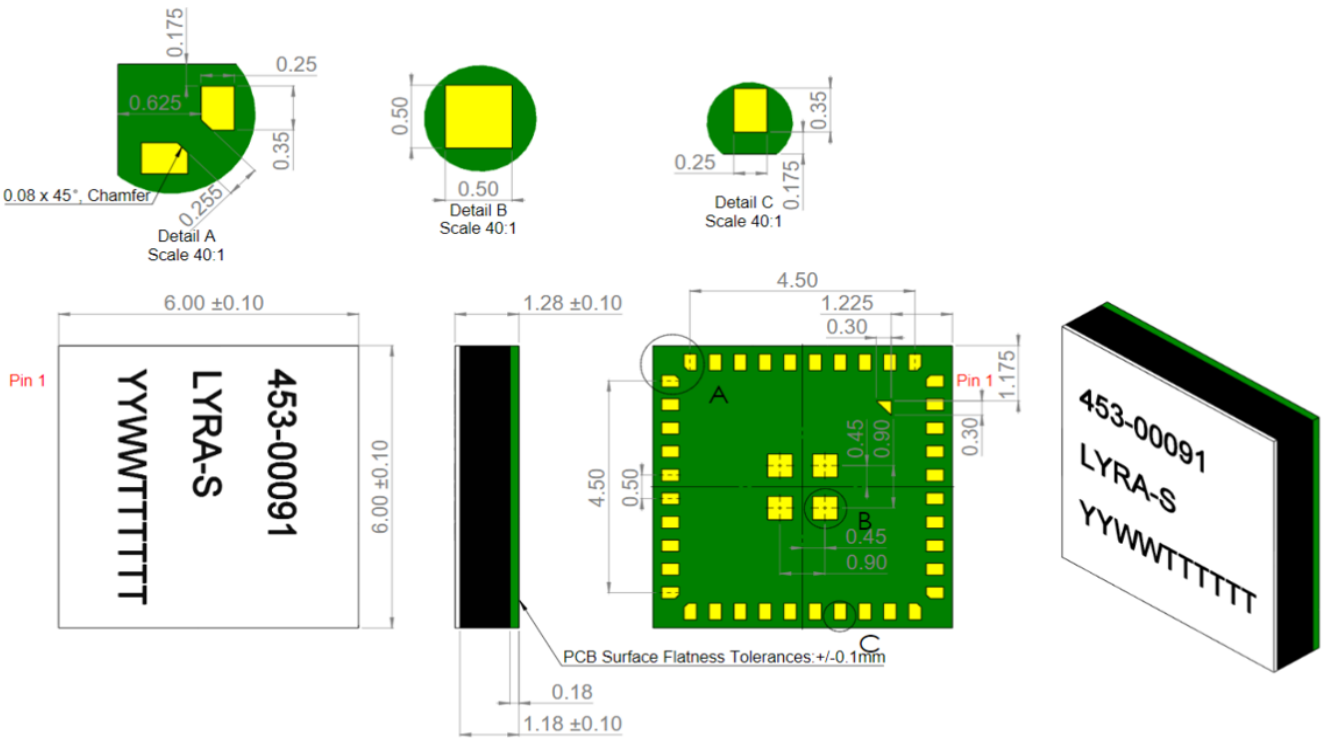


Figure 18: Mechanical Dimensions – Full

8.2 Recommended PCB Land Pattern

The recommended PCB Land Pattern is shown in Figure 19.

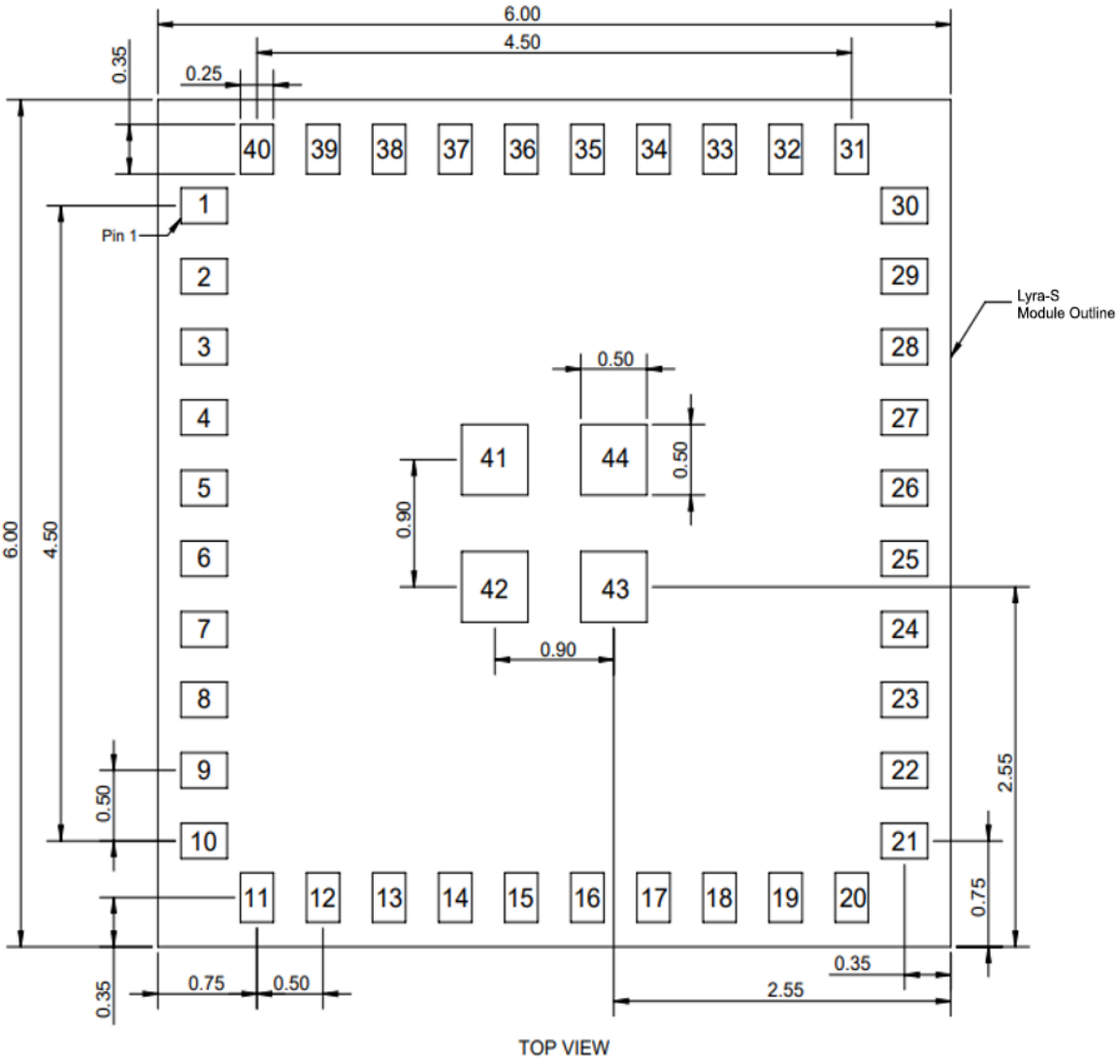


Figure 19: Module Land Pattern

Notes:

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05mm is assumed.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.100 mm (4 mils).
5. The stencil aperture to land pad size recommendation is 80% paste coverage.

Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

8.3 Lyra S Top Marking

Figure 20: Lyra S Top Marking

Table 19: Top Marking Definition

Part Number	Line 1 Marking	Line 2 Marking	Line 3 Marking
453-00091	453-00091	Lyra-S	See note below

Note: YY = Year. WW = Work Week, TTTTTTT = Trace Code

9 Soldering Recommendations

9.1 Reflow for lead Free Solder Paste

- Optimal solder reflow profile depends on solder paste properties and should be optimized as part of an overall process development.
- It is important to provide a solder reflow profile that matches the solder paste supplier'srecommendations.
- Temperature ranges beyond that of the solder paste supplier's recommendation could result in poorsolderability.
- All solder paste suppliers recommend an ideal reflow profile to give the best solderability.

9.2 Recommended Reflow Profile for lead Free Solder Paste

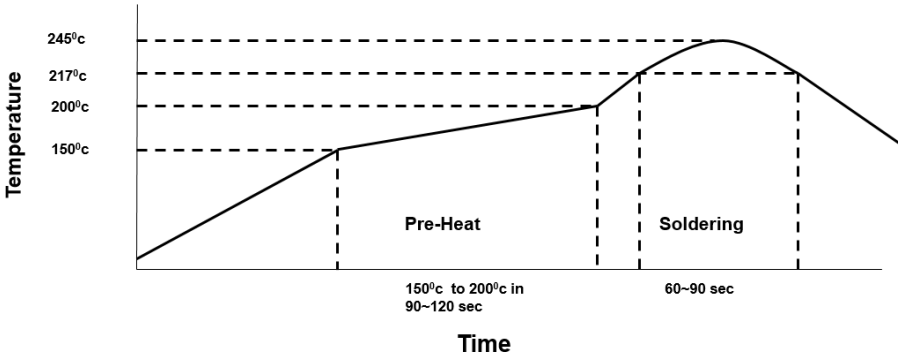


Figure 21: Recommended Reflow Profile

10 Miscellaneous

10.1 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently

10.2 Rework

The Lyra S module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions terminate warranty coverage.

10.3 Handling and Storage

10.3.1 Handling

The Lyra S modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently

10.3.2 Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 3 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

10.3.3 Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX. Do not store in direct sunlight.

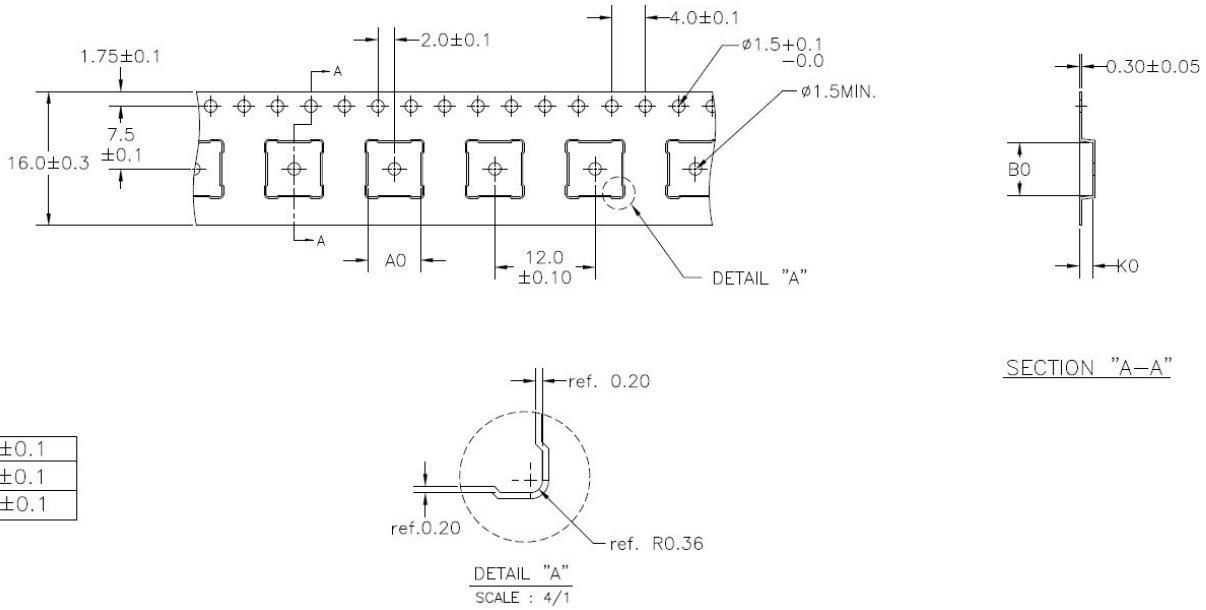
The product should not be subject to excessive mechanical shock.

10.3.4 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

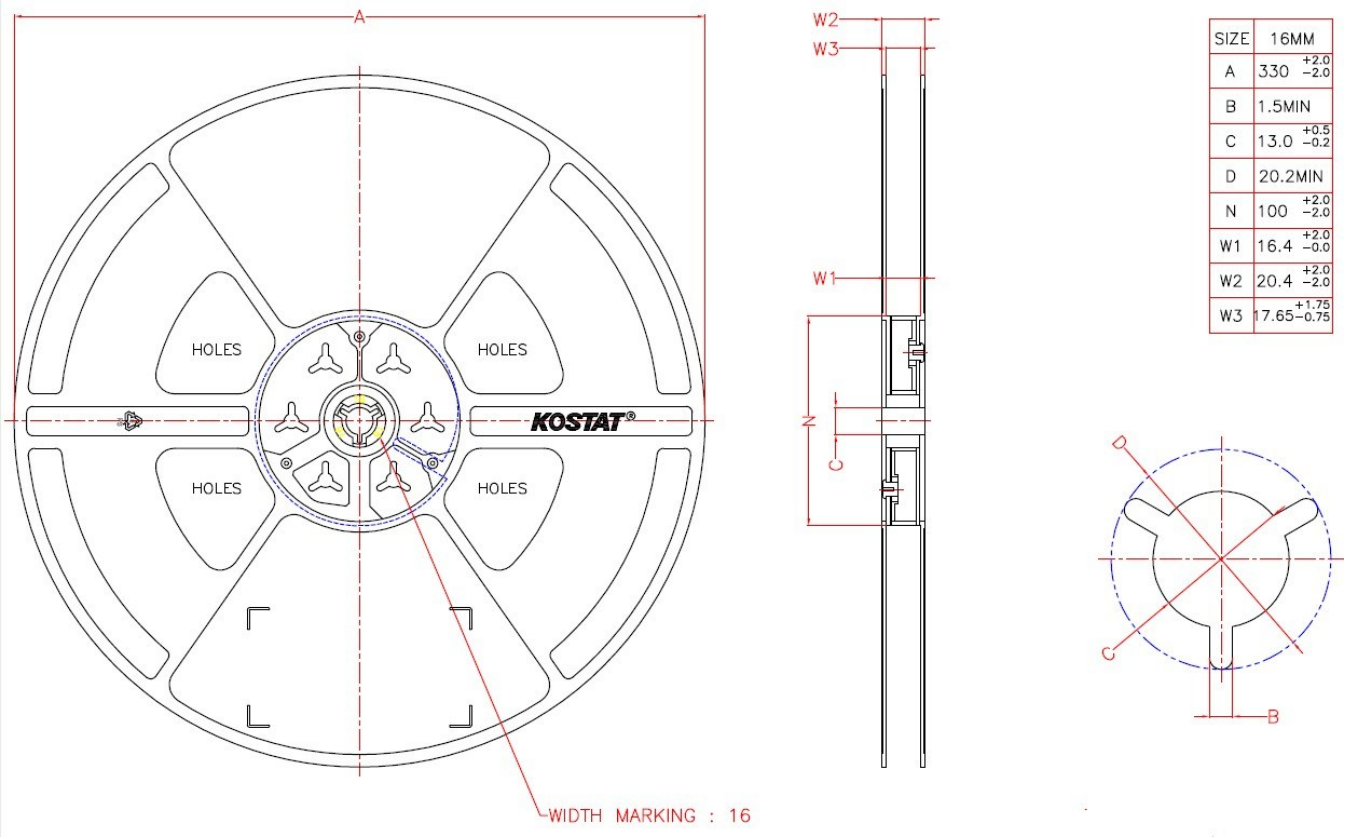
11 Tape and Reel

Lyra S modules are delivered to the customer in Cut Tape (600 pcs) or reel (2500 pcs / reel) packaging with the dimensions below. All dimensions are given in mm unless otherwise indicated.



A0	6.30mm±0.1
B0	6.30mm±0.1
K0	1.60mm±0.1

Figure 22: Carrier Tape Dimensions



SIZE	16MM
A	330 +2.0 −2.0
B	1.5MIN
C	13.0 +0.5 −0.2
D	20.2MIN
N	100 +2.0 −2.0
W1	16.4 +2.0 −0.0
W2	20.4 +2.0 −2.0
W3	17.65 +1.75 −0.75

Figure 23: Reel Dimensions

12 Regulatory

Note: For complete regulatory information, refer to the Lyra S Regulatory Information document which is also available from the Lyra Series product page.

The Lyra S holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-LyraS
Canada (ISED)	3147A-LyraS
UK (UKCA)	N/A
EU	N/A
Japan (MIC)	209-J00457
Korea (KC)	R-C-L7C-LyraS

13 Bluetooth SIG Qualification

13.1 Overview

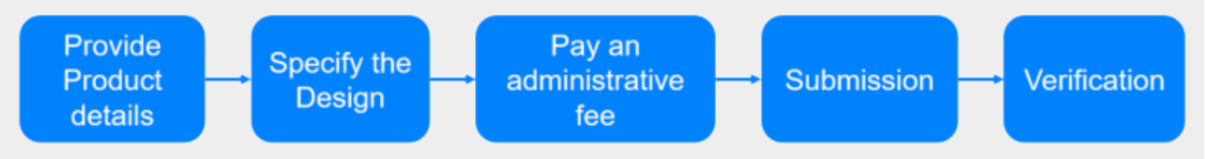
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

13.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference a single existing design, that has not been modified, (refer to Section 3.2.1 of the Qualification Program Reference Document v3).

This option applies to a Member qualifying a Product that includes an existing Design that has a DN, QDID, or DID and that Design has not been modified (e.g., rebranding a Qualified Product from another Member). The Design identified by the DN, QDID, or DID may only implement Bluetooth Specifications that are active or deprecated at the time of Submission. No modifications may be made to the Design, including changes to the ICS Form.

Changes to the Product outside the Design are allowed, including:

- Enabling technologies
- Changes to the industrial design
- Changes to the communication technology other than Bluetooth
- Changes to the features that are unrelated to Bluetooth, branding, packaging, colour, shape, Product name, or Model number

Members are responsible for assessing that modifications to the Product outside of the Design do not affect compliance with Bluetooth Specifications or result in a change to the ICS Form.

For the purposes of this document, it is assumed that the member is combining a single unmodified Core-Complete Configuration.

13.3 Qualification Steps When Referencing a single existing design, (unmodified) – Option 1 in the QPRDv3

For this qualification, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number

- Product Publication Date (the product publication date may not be later than 90 days after submission)
- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
- If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the single DN or QDID used in your, (for Option 1 only one DN or QDID can be referenced)
   - Once the DN or QDID is selected it will appear on the left-hand side, indicating the layers covered by the design.
   - Select 'I'm finished entering DN's
   - What do you want to do next? Answer, 'Use this Design without Modification'
   - Save and go to Product Qualification Fee
5. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
6. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
7. Download Product and Design Details:
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

13.4 Example Designs for reference

The following gives an example of a design possible under option 1:

Ezurio End Product design using Silicon Labs Component based design

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
Lyra S	Ezurio	D057227	182889	https://qualification.bluetooth.com/ListingDetails/147725

13.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

14 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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http://www.ezurio.com