Datasheet

Sera NX040

Version 2.1

Revision History

Version	Date	Notes	Contributor(s)	Approver
0.1	11/7/2023	Preliminary release	Dave Neperud	Jonathan Kaye
0.2	11/29/2023	Updated Table 9 – ranging accuracy	Dave Neperud	Jonathan Kaye
1.0	15 Dec 2023	Initial Release	Dave Neperud	Jonathan Kaye
1.1	25 Mar 2024	Revised for latest SW options (Canvas, Python, AT Command set)	Erik Lins	Jonathan Kaye
1.2	30 Oct 2024	Updated Bluetooth Qualification process	Dave Drogowski	Jonathan Kaye
2.0	24 Feb 2024	Ezurio rebranding	Sue White	Dave Drogowski
2.1	1 Dec 2025	Updated RAM values in Host MCU Current Consumption	Dave Drogowski	Dave Neperud

Contents

1 Overview

The Sera NX040 series modules are an integration of wireless silicon from NXP and Nordic Semiconductor to produce a small form factor UWB/BLE module that is optimized for indoor positioning and location applications. The integration of all UWB and Bluetooth LE functionality in a single package provides value added hardware and software capabilities to the development of UWB/BLE applications.

The Sera NX040 series device supports IEEE 802.15.4/4z HPR UWB operations with a fully embedded FiRa compliant MAC and PHY. The device supports both initiator and responder modes for Two-Way Ranging sessions as well as Blink mode operation in Time Difference of Arrival system. The device includes a dedicated Bluetooth 5.4 radio for provisioning, setup, and control of the UWB ranging sessions.

The Sera NX040 is a complete hardware solution incorporating all the required circuitry for a UWB/BLE application. The inclusion of an additional 8Mb of flash on the module provides the user room to grow through additional value-added software capability as well as an easier application development experience. In addition, each device is pre-calibrated for regulatory compliance as well as for optimal ranging performance over temperature and UWB antenna implementation. The Sera NX040 series wireless modules include two product SKUs which have different RF antenna implementations to fit every application. Please contact Ezurio Sales/FAE for further information.

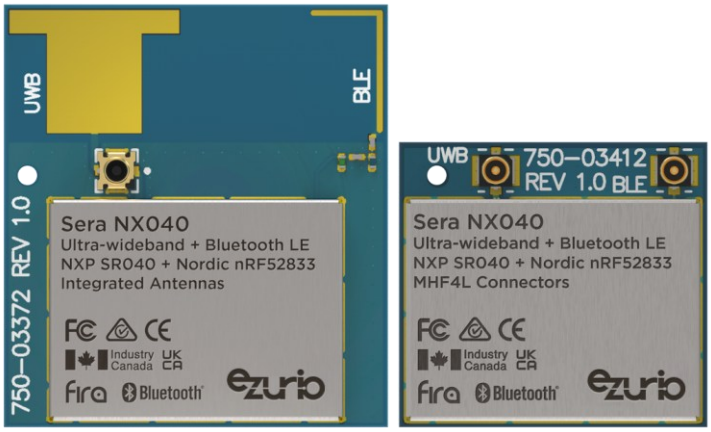


Figure 1: Sera NX040 module variants

2 Ordering Information

Table 1: Ordering Information

Part Number	Product Description
453-00174R	Module, Sera NX040, MHF4L, Tape and Reel
453-00174C	Module, Sera NX040, MHF4L, Cut Tape
453-00175R	Module, Sera NX040, Trace Antenna, Tape and Reel
453-00175C	Module, Sera NX040, Trace Antenna, Cut Tape
453-00174-K1	Development Kit, Module, Sera NX040, MHF4L
453-00175-K1	Development Kit, Module, Sera NX040, Trace Antenna

3 Sera NX040 Features Summary

Table 2: NX040 features summary

Feature	Description
Variants	• Integrated UWB and BLE antennas on module (453-00175) • MHF4L connectors for external cabled antennas (453-00174)
Ultra-Wideband (UWB)	• NXP – Trimension™ SR040HN/B02CY chipset • Supports Two Way Ranging (TWR) and Time Difference of Arrival (TDoA) technologies. • Ranging accuracy < ±10cm. • IEEE 802.15.4/4z HRP UWB PHY compliant • FiRa ready MAC and PHY (FiRa certified chipset) • 128 MHz PRF (HPRF) support • Channels 5 (6489.6 MHz) & 9 (7987.2 MHz) supported. • -92 dBm typical receiver sensitivity (6.8 Mbps, 62.4 MHz PRF) • Antenna delay factory calibrated
Bluetooth®	• Nordic Semiconductor – nRF52833-CJAA • Bluetooth (LE) v5.4 • CODED PHY and 2M PHY support • +8 dBm maximum transmit output power (conducted), configurable to -40 dBm. • -96 dBm typical receive sensitivity (BLE @ 1Mbps)
Microcontroller (MCU)	• 64 MHz ARM® Cortex®-M4 Core with FPU • 512KB on chip flash • 128KB on chip RAM • 1MB on module SPI flash to ease integration and customer software development • SWD/JTAG programming interfaces • Over-the-air (OTA) firmware updates via BLE • On module 32.768kHz crystal for low power operation and timing accuracy
Peripherals	• Full Speed 12 Mbps USB 2.0 • UART, SPI, I2C interfaces • 8 Dedicated GPIO • General Timer and PWM interfaces • ADC • NFC – supported by external antenna (part # 0600-00061)
Programmability	• Rapid design applications. Canvas™ Software Suite • On-module Python Scripting Engine • AT command set for hosted designs
Supply Voltage	• Main module power supply 1.8 - 3.6 V • Nordic nRF52833 uses Internal DCDC converter or LDO for BLE/MCU power domains. • NXP SR040 supply domains integrated on module.
Dimensions	• Integrated Antenna variant: 20.3 x 22.3 x 2.15 mm • External MHF4 connector variant: 15 x 16.3 x 2.15 mm
Warranty	• One Year Warranty
Approvals	• FCC/ISED/EU/UKCA • RCM/MIC/KCC pending. • Full Bluetooth SIG Declaration ID • FiRa Consortium - TBD

4 Block Diagram

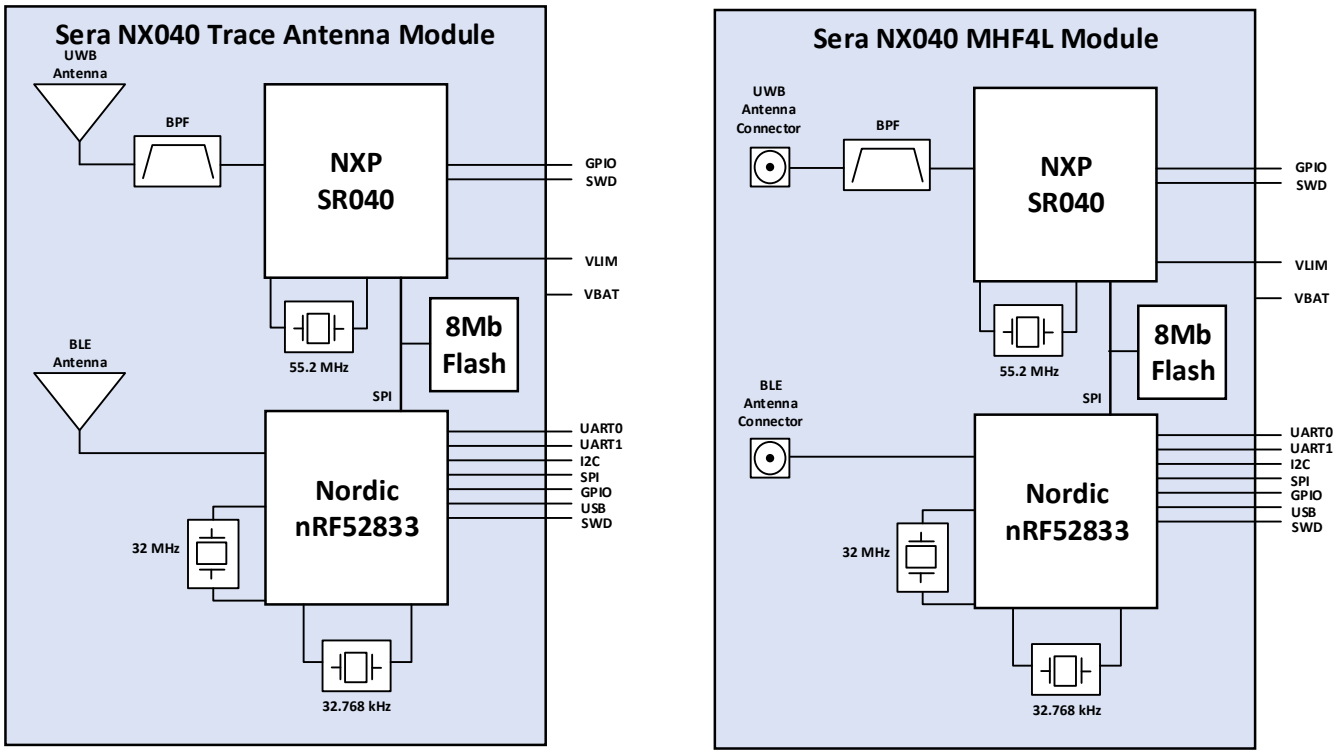


Figure 2: NX040 block diagrams

5 Symbol/Pin Definitions/Footprint

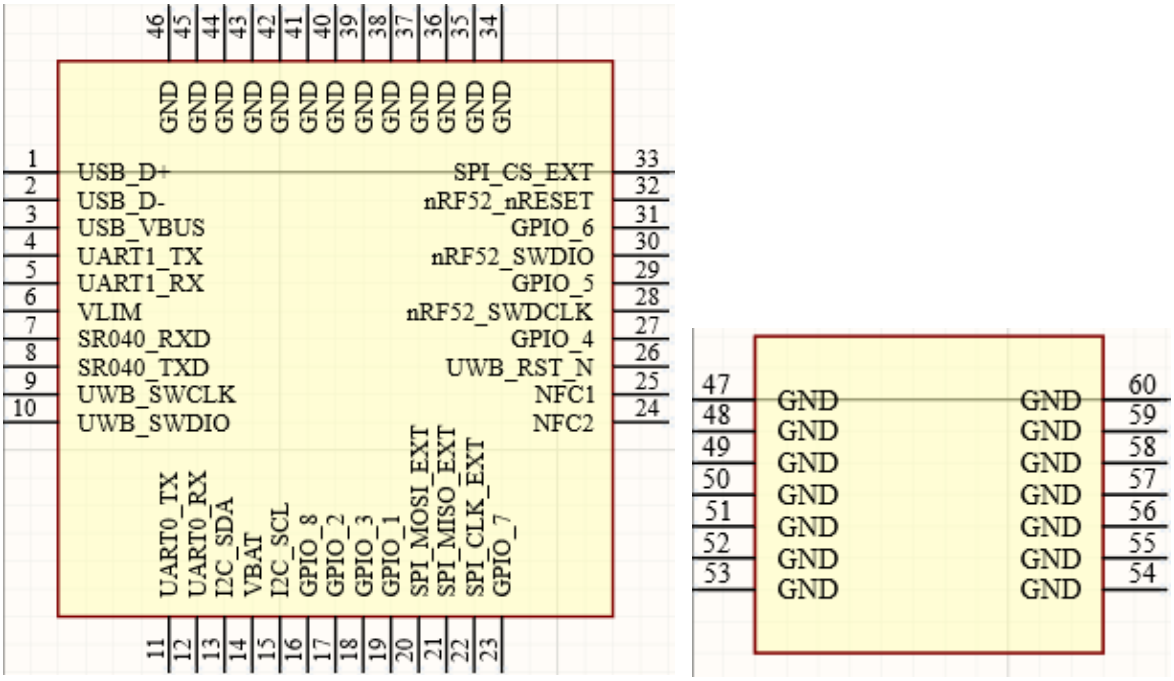


Figure 3: NX040 modules schematic symbol

5.1 Pin Definitions

Table 3: NX040 series module Pin definitions (Note 1)

Pin #	Pin Name	Type	nRF52833 WLCSP Pin	nRF52833 Name	SR040 Pin	SR040 Name	Description
1	USB_D+	USB	J7	D+	-	-	USB D+
2	USB_D-	USB	H7	D-	-	-	USB D-
3	USB_VBUS	Pin	H8	VBUS	-	-	5V input for USB regulator
4	UART1_TX	O	J5	P0.17	-	-	-
5	UART1_RX	I	G8	P0.11	-	-	-
6	VLIM	Pin	-	-	9	VDD_BUF	Connected to programmable current limiter output. Supply for UWB LDO and PA
7	SR040_RXD	-	-	-	13	P11	Not available[2]
8	SR040_TXD	-	-	-	14	P12	Not available[2]
9	UWB_SWCLK	-	-	-	17	SWCLK	SR040 Serial Wire debug (SWD) Clock[2]
10	UWB_SWDIO	-	-	-	18	SWDIO	SR040 Serial Wire debug (SWD) Data[2]
11	UART0_TX	O	E9	P0.06	-	-	-
12	UART0_RX	I	E8	P0.07	-	-	-
13	I2C_SDA	I/O	C9	P0.26	-	-	-
14	VBAT	Pin	G9,H9,A9,B3,J1,J4	VDD,VDDH	26	VBAT_IO	Main Power Supply Input
15	I2C_SCL	I/O	C8	P0.27	-	-	-
16	GPIO_8	I/O	B6	P0.31/AIN7	-	-	GPIO[3]
17	GPIO_2	I/O	A5	P0.29/AIN5	-	-	GPIO[3]
18	GPIO_3	I/O	B5	P0.30/AIN6	-	-	GPIO[3]

Pin #	Pin Name	Type	nRF52833 WLCSP Pin	nRF52833 Name	SR040 Pin	SR040 Name	Description
19	GPIO_1	I/O	A4	P0.03/AIN1	-	-	GPIO[3]
20	SPI_MOSI_EXT	O	F9	P1.08	-	-	-
21	SPI_MISO_EXT	I	G4	P0.21	-	-	-
22	SPI_CLK_EXT	O	F8	P1.09	-	-	-
23	GPIO_7	I/O	B4	P1.03	-	-	GPIO[3]
24	NFC_2	I/O	E2	P0.10/NFC2	-	-	NFC antenna /GPIO[3]
25	NFC_1	I/O	F2	P0.09/NFC1	-	-	NFC antenna /GPIO[3]
26	UWB_RST_N	-	G1	P1.07	31	RST_N	SR040 reset input (active low)[4]
27	GPIO_4	I/O	H1	P1.02	-	-	GPIO[3]
28	NRF52_SWDCLK	-	H2	SWDCLK	-	-	Serial wire debug clock input for programming and debug
29	GPIO_5	I/O	H3	P1.00	-	-	GPIO
30	NRF52_SWDIO	-	J2	SWDIO	-	-	Serial wire debug I/O for programming and debug
31	GPIO_6	I/O	J3	P0.22	-	-	GPIO
32	NRF52_NRESET	I	H4	P0.18/RESET	-	-	Reset pin[5]
33	SPI_CS_EXT	I/O	G5	P0.20	-	-	SPI_CS or GPIO
34	GND	GND	-	-	-	-	-
35	GND	GND	-	-	-	-	-
36	GND	GND	-	-	-	-	-
37	GND	GND	-	-	-	-	-
38	GND	GND	-	-	-	-	-
39	GND	GND	-	-	-	-	-
40	GND	GND	-	-	-	-	-
41	GND	GND	-	-	-	-	-
42	GND	GND	-	-	-	-	-
43	GND	GND	-	-	-	-	-
44	GND	GND	-	-	-	-	-
45	GND	GND	-	-	-	-	-
46	GND	GND	-	-	-	-	-
47	GND	GND	-	-	-	-	-
48	GND	GND	-	-	-	-	-
49	GND	GND	-	-	-	-	-
50	GND	GND	-	-	-	-	-
51	GND	GND	-	-	-	-	-
52	GND	GND	-	-	-	-	-
53	GND	GND	-	-	-	-	-
54	GND	GND	-	-	-	-	-
55	GND	GND	-	-	-	-	-
56	GND	GND	-	-	-	-	-
57	GND	GND	-	-	-	-	-
58	GND	GND	-	-	-	-	-
59	GND	GND	-	-	-	-	-
60	GND	GND	-	-	-	-	-

Pin #	Pin Name	Type	nRF52833 WLCSP Pin	nRF52833 Name	SR040 Pin	SR040 Name	Description

Pin Definition Notes:

Note 1	GPIO voltage levels track VBAT. AIN = Analog Input.
Note 2	Not currently supported, leave pins as no connect or bring to test pads
Note 3	Standard Drive, low frequency I/O only. Low frequency I/O is a signal with a frequency up to 10kHz.
Note 4	Controlled on-module. Leave as no connect or bring to test pad.
Note 5	HW reset. Pull nRESET pin low for >100msec to reset the nRF52833.
Note 6	Connect all module GND pins to host PCB ground.

5.2 Module Footprints

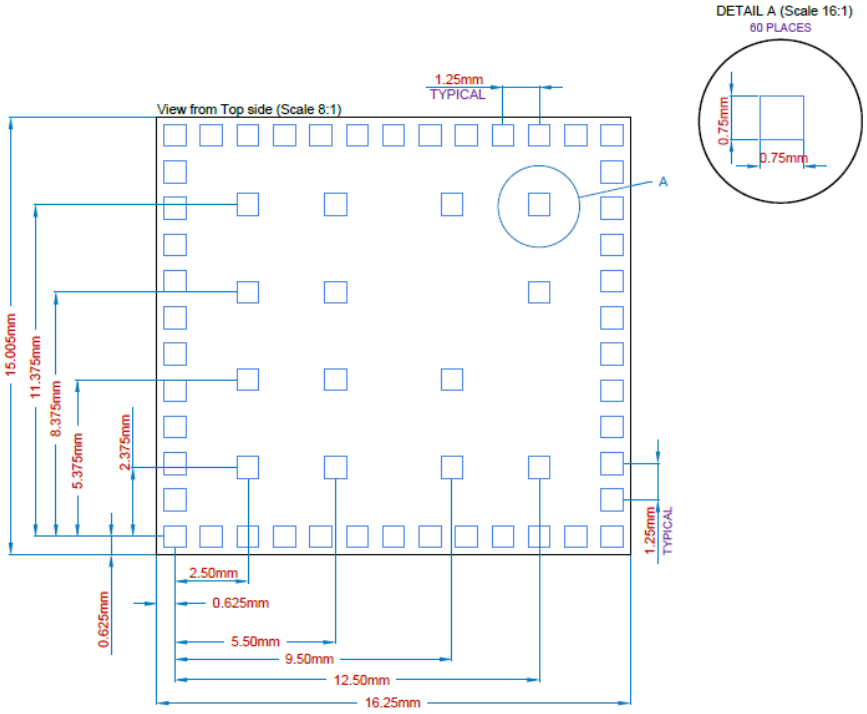


Figure 4: Land pattern for MHF4 connector variant (453-00174)

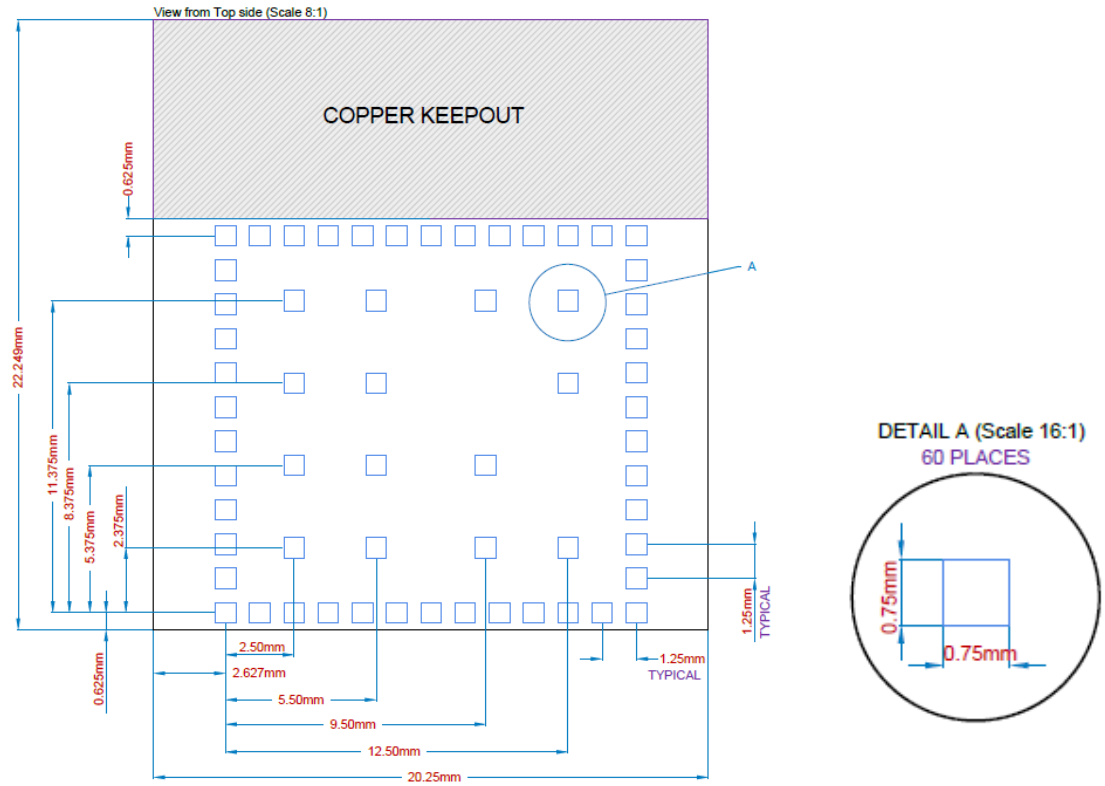


Figure 5: Land pattern and Keep-out for PCB antenna variant (453-00175)

6 UWB Functional Description

The Sera NX040 module is designed with the NXP SR040 Ultra-Wideband Transceiver. The SR040 is a fully integrated single chip Impulse Radio Ultra-Wideband low energy IC compliant to IEEE 802.15.4/4z UWB PHY. The Sera NX040 performs Time of Flight (ToF) distance measurements between NX040 devices via Two-Way Ranging (TWR). The Sera NX040 is also capable of operating as an initiator in Time Difference of Arrival (TDoA) based one way ranging to synchronized anchor devices.

Table 4: UWB Functional Description

Feature	Description
UWB Configurations	• The NX040 supports SS/DS-TWR (Single/Double Sided – Two Way Ranging) between NX040 devices. • Module can function in either initiator or responder TWR role. • Supports blink localization mode (TDoA) for use with an Anchor device.
UWB Functionality	• HRP UWB PHY • Fully embedded MAC and PHY compliant to FiRa consortium specification. • Integrated Baseband subsystem implements algorithms for data transfer and time of arrival (ToA) measurements. • UWB CPU subsystem. 32-bit ARM® Cortex®-M33 processor. • 256kB Non-volatile memory for calibration and UWB MAC operations. • Integrated TX/RX switch for a single UWB RF port • On-module 55.2MHz system clock source.
UWB Security	• Dedicated hardware block for secured Crypto subsystem. • IEEE 802.15.4z UWB PHY enhancements implemented. • Scrambled Timestamp Sequence (STS) supported compliant to NIST SP 800-90A..
UWB Channel	• HRP UWB channels 5 and 9. • 499.2 MHz channel bandwidth. • 6.81Mbps and 7.80Mbps Data rates available • 62.4MHz (BPRF mode) and 124.8MHz (HPRF mode) Pulse Repetition Frequencies (PRF) • On module crystal thermistor with stored LUTs to maintain center frequency accuracy over temperature.
UWB Calibrations	• Transmit power individually calibrated on each module to meet regulatory limits. • Crystal frequency offset calibrated to maintain ranging accuracy. • Antennas calibrated for most accurate ranging.
UWB Power	• Module has configurable current limiter for battery powered applications. • Operation in Initiator mode (TWR) and blink mode (TDoA) can be battery powered. • Device operating in Responder mode must be powered with a regulated external supply.

7 BLE Functional Description

The Sera NX040 series modules are designed with the Nordic Semiconductor nRF52833 chipset. The nRF52833 is a fully qualified Bluetooth SoC supporting Bluetooth Low Energy.

Table 5: BLE Functional Description

Feature	Description
BLE Features	• Bluetooth (LE) Core Specification version 5.4 • CODED PHY support • 2M PHY support
BLE Functionality	• Beaconing • Advertising • Provisioning • OOB Pairing • OTA Firmware updates. • Setup and control of UWB ranging sessions. • Backhaul channels.

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Absolute maximum ratings for supply voltage and voltages on digital and analog pins of the module are listed in the following table; exceeding these values causes permanent damage.

Table 6: Maximum ratings

Parameter	Min	Max	Unit
Voltage at VBAT pin	-0.3	+3.6	V
Voltage at VLIM pin	-0.3	+3.6	V
Voltage at USB_VBUS pin	-0.3	+5.8	V
Voltage at GND pin		0	V
Voltage at SIO pin	-0.3	VBAT +0.3	V
NFC antenna pin current (NFC1/2)	-	80	mA
Radio RF input level (BLE or UWB)	-	+10	dBm
Environmental			
Storage temperature	-40	+85	°C
MSL (Moisture Sensitivity Level)	-	4	-
Electrostatic Discharge Voltage			
Human Body Model (HBM)[1], 1500 Ω, 100pF		2	kV
Charged Device Model (CDM)[2], all IO except RF		500	V
Maximum Rating Notes:			
Note 1 ANSI/ESDA/JEDEC JS-001			
Note 2 ANSI/ESDA/JEDEC JS-002			

8.2 Recommended Operating Parameters

The recommended operating conditions for the Sera NX040 series wireless module are listed in the following tables. Operation at conditions outside those listed is not recommended.

Table 7: Recommended operating parameters

Parameter	Min	Typ	Max	Unit
VBAT	1.8	3.3	3.6	V
VLIM[1]		VBAT	VBAT	V
$VBAT_{POR}$ voltage	1.75	-	-	V
VBAT maximum ripple or noise[2]	-	-	10	mV
VBAT supply rise time (0V to 1.8V)[3]	-	-	60	msec
USB_VBUS supply range	4.35	5	5.5	V
Operating temperature range	-40	+25	+85	°C
Recommended Operating Parameters Notes:				
Note 1 VLIM is either tied directly to VBAT, left unconnected, or connected to additional storage capacitance.				
Note 2 This is the maximum supply ripple or noise that does not disturb the radio performance.				
Note 3 For proper power-on reset functionality				

8.3 Electrical Specifications

Table 8: Signal levels for interface, SIO

Parameter	Min	Typ	Max	Unit
V_{IH} Input high voltage	0.7 VBAT		VBAT	V
V_{IL} Input low voltage	VSS		0.3 x VBAT	V
V_{OH} Output high voltage				
(std. drive, 0.5mA) (Note 1)	VBAT - 0.4		VBAT	V
(high-drive, 3mA) (Note 1)	VBAT - 0.4		VBAT	V
(high-drive, 5mA) (Note 2)	VBAT - 0.4		VBAT	
V_{OL} Output low voltage				
(std. drive, 0.5mA) (Note 1)	VSS		VSS+0.4	V
(high-drive, 3mA) (Note 1)	VSS		VSS+0.4	V
(high-drive, 5mA) (Note 2)	VSS		VSS+0.4	
V_{OL} Current at VSS+0.4V, Output set low				
(std. drive, 0.5mA) (Note 1)	1	2	4	mA
(high-drive, 3mA) (Note 1)	3	-	-	mA
(high-drive, 5mA) (Note 2)	6	10	15	mA
V_{OL} Current at VBAT - 0.4, Output set low				
(std. drive, 0.5mA) (Note 1)	1	2	4	mA
(high-drive, 3mA) (Note 1)	3	-	-	mA
(high-drive, 5mA) (Note 2)	6	9	14	mA
Pull up resistance	11	13	16	kΩ
Pull down resistance	11	13	16	kΩ
Pad capacitance		3		pF
Pad capacitance at NFC pads		4		pF

Signal Levels Notes:

Note 1 For VBAT≥1.8V. The firmware supports high drive (3 mA, as well as standard drive). See Table 3 for NX040 pin assignments of GPIO supporting standard drive only.

Note 2 For VBAT≥2.7V. The firmware supports high drive (5 mA (since VBAT≥2.7V), as well as standard drive).
The GPIO (SIO) high voltage level always equals the voltage supplied to the **VBAT** pin. See Table 3 for NX040 pin assignments of GPIO supporting standard drive only.

9 RF Characteristics

9.1 UWB Radio RF Characteristics

Table 9: UWB RF Characteristics

Item	Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range		Channel 5 and 9	6.24	-	8.24	GHz
Channel Bandwidth			-	500	-	MHz
Carrier Frequency Offset		-40˚C ~ +85˚C	-15	-	+15	ppm
TX Output Power Spectral Density (EIRP)	Channel 5	See Note 1	-	-41.3	-	dBm/MHz
	Channel 9		-	-41.3	-	
Data Rate			-	6.8	7.8	Mbps
Rx Sensitivity	6.8Mbps, 62.4MHz PRF	SP0 packet format	-	-92		dBm
	6.8Mbps, 62.4MHz PRF	SP3 packet format	-	-96		dBm
Pulse Repetition Rate			-	62.4	124.8	MHz
Symbol Modulation Accuracy			-	97	-	%
Maximum RF Input Level		UWB signal, functional	-20	-	-	dBm
Ranging ToF accuracy[2]	95% confidence level	STS used	-10	-	+10	cm

UWB RF Notes:

Note 1: Each module is calibrated at production for < -41.3 dBm/MHz transmit output EIRP on both channels. Tx Adaptive power control **must** be enabled to apply transmit power calibration values and meet regulatory requirements.

Note 2: On Sera NX040 DVK at 3m separation, 1.5m height.

9.2 BLE Radio RF Characteristics

Table 10: BLE RF Characteristics

Item	Conditions	Min	Typ	Max	Unit
Frequency Range	-	2402	-	2480	MHz
RX Sensitivity	1Mbps, 30.8% PER	-	-96	-	dBm
	2Mbps, 30.8% PER	-	-92	-	dBm
	500kbps, 30.8% PER	-	-99	-	dBm
	125kbps, 30.8% PER	-	-103	-	dBm
TX Power Setting		-40	0	+8	dBm
Maximum EIRP[1]		-	-	10	dBm

BLE RF Notes:

Note 1: BLE RF transmit EIRP cannot exceed 10dBm for CE compliance and operation. In these countries the BLE TX power setting CANNOT be set higher than +5dBm for operation.

10 Power Consumption

Data at VBAT of 3.3 V and 25°C unless otherwise noted.

10.1 Radio Power Consumption

Table 11: NX040 UWB Power consumption

Parameter	Min	Typ	Max	Unit
Active state 'peak' current (Note 1)				
UWB Tx only peak current		115		mA
UWB Rx only peak current	-	131	-	mA
Hard Power Down Mode (HPD) (Note 2)	-	500	-	nA
SR040 powered down				
Deep Power Down Mode (DPD) (Note 3)				
Retention mode		550		µA
Without state retention		5		µA
Active State current				
SR040 Wake		4.0		mA
SR040 CPU running		5.1		mA

UWB Power Consumption Notes:

Note 1 UWB Ranging Session. This is for Peak UWB Radio Current only, there is additional current due to the MCU.

Note 2 Firmware activated. The SR040 can be activated by a chip reset.

Note 3 In Deep Power Down retention mode, the memory is powered, and the wake-up timer is running.

- In no retention state wake up is possible through external interrupt or chip reset.

Table 12: NX040 BLE Power consumption: VBAT = 3.3V with nRF52833 DCDC(REG1) or LDO(REG1) at 25 °C

Parameter	Min	Typ	Max	Unit
Active mode 'peak' current (Note 1)		With DCDC [with LDO]		
(Advertising or Connection)				
Tx only run peak current @ Txpwr = +8 dBm		14.2 [30.4]		mA
Tx only run peak current @ Txpwr = +4 dBm		9.6 [20.7]		mA
Tx only run peak current @ Txpwr = 0 dBm		4.9 [10.3]		
Tx only run peak current @ Txpwr = -4 dBm		3.8 [8.0]		
Tx only run peak current @ Txpwr = -8 dBm		3.4 [7.1]		
Tx only run peak current @ Txpwr = -12 dBm		3.1 [6.4]		
Tx only run peak current @ Txpwr = -16 dBm		2.9 [5.9]		
Tx only run peak current @ Txpwr = -20 dBm		2.7 [5.5]		
Tx only run peak current @ Txpwr = -40 dBm		2.3 [4.5]		
Active Mode				
Rx only 'peak' current, BLE 1Mbps (Note 1)		4.6 [9.6]		mA
Rx only 'peak' current, BLE 2Mbps (Note 2)		5.2 [10.7]		mA

Active Mode Average current (Note)		
Advertising Average Current draw		
Max, with advertising interval (min) 20 mS	Note 2	uA
Min, with advertising interval (max) 10240 mS	Note 2	uA
Connection Average Current draw		
Max, with connection interval (min) 7.5 mS		
Min, with connection interval (max) 4000 mS	Note 2	uA
	Note 2	uA

Power Consumption Notes:

Note 1 This is for BLE Radio Current only, there is additional current due to the MCU. The internal DCDC convertor (REG1) or LDO (REG1) is decided by the underlying BLE stack.

Note 2 Average current consumption depends on several factors (including Tx power, VCC, accuracy of 32MHz and 32.768 kHz). With these factors fixed, the largest variable is the advertising or connection interval set.

Advertising Interval range:

- 20 milliseconds to 10240 mS in multiples of 0.625 milliseconds.

For an advertising event:

- The minimum average current consumption is when the advertising interval is large 10240 mS.
- The maximum average current consumption is when the advertising interval is small 20 mS.
- Other factors that are also related to average current consumption include the advertising payload bytes in each advertising packet and whether it's continuously advertising or periodically advertising.

Connection Interval range (for a peripheral):

- 7.5 milliseconds to 4000 milliseconds in multiples of 1.25 milliseconds.

For a connection event (for a peripheral device):

- The minimum average current consumption is when the connection interval is large 4000 milliseconds.
- The maximum average current consumption is with the shortest connection interval of 7.5 ms, no slave latency.

Other factors that are also related to average current consumption include:

- Number packets per connection interval with each packet payload size

Connection Interval range (for a central device):

- 2.5 milliseconds to 40959375 milliseconds in multiples of 1.25 milliseconds.

10.2 Host MCU Current Consumption

Table 13: NX040 Host Power consumption: VBAT = 3.3V with nRF52833 DCDC(REG1) or LDO(REG1) at 25 ˚C

Parameter	Min	Typ	Max	Unit
CPU running (Note 1)		With DCDC [with LDO]		
CPU running @64MHz from flash		3.3 [5.6]		mA
CPU running @64MHz from RAM		2.4 [4.7]		mA
Ultra-Low Power Mode 1 (Note 2) Standby Doze, 128k RAM retention		2.7		uA
Ultra-Low Power Mode 2 (Note 3) Deep Sleep (no RAM retention)		0.6		uA
8Mb SPI Flash				
Standby Current		5		uA
Deep Power Down		7		nA
Read		2.2		mA

Host Power Consumption Notes:

Note 1: Typical scenario based on CoreMark® benchmark.

Note 2: Standby Doze of 2.7 uA typical is for the Nordic nRF52833 section only.

Note 3: In Deep Sleep, everything is disabled, and the only wake-up sources are reset and changes on SIO or NFC pins on which sense is enabled.

10.3 Peripheral Block Current Consumption

The values below are provided for a typical operating voltage of 3V.

Table 14: UART power consumption

Parameter	Min	Typ		Max	Unit
		WITH DCDC(REG1)	WITH LDO(REG1)		
UART Run current @ 115200 bps	-	450	721	-	uA
UART Run current @ 1200 bps	-	450	721	-	uA
Idle current for UART (no activity)	-	2.9	2.9	-	uA

Table 15: SPI power consumption

Parameter	Min	Typ		Max	Unit
		WITH DCDC(REG1)	WITH LDO(REG1)		
SPI Master Run current @ 2 Mbps	-	536	803	-	uA
SPI Master Run current @ 8 Mbps	-	536	803	-	uA
Idle current for SPI (no activity)	-	<1	<1	-	uA

Table 16: I2C power consumption

Parameter	Min	Typ		Max	Unit
		WITH DCDC(REG1)	WITH LDO(REG1)		
I2C Run current @ 100 kbps	-	734	994	-	uA
I2C Run current @ 400 kbps	-	734	994	-	uA
Idle current for I2C (no activity)	-	2.5	2.5	-	uA

Table 17: ADC power consumption

Parameter	Min	Typ		Max	Unit
		WITH DCDC(REG1)	WITH LDO(REG1)		
ADC current during conversion	-	1900	1350	-	uA
Idle current	-	0	0	-	uA

The above current consumption is for the given peripheral including the internal blocks that are needed for that peripheral for both the case when DCDC(REG1) is on and LDO (REG1) is on. The peripheral Idle current is when the peripheral is enabled but not running (not sending data or being used). In all cases radio is not turned on.

11 Host Implementation

To provide the widest scope for integration, a variety of physical host interfaces are provided. The major NX040 series module functional blocks supported are described below.

Please refer to the Nordic Semiconductor nRF52833 product specification for further details on the requirements, implementation, and use of these peripherals. https://infocenter.nordicsemi.com/topic/ps_nrf52833/keyfeatures_html5.html

11.1 Canvas™ Firmware Pin Mapping

Default NX040 pin mapping for the NX040 development kit and Ezurio Canvas™ firmware. When referring to a hardware pin from within a Python script, use the name in the Canvas™ Pin Name column.

Table 18: Pin Mapping

Pin #	NX040 Pin Name	NX040 DVK Default Function	nRF52833 Pin Name	Canvas™ Pin Name
4	UART1_TX	UART1_TX	P0.17	
5	UART1_RX	UART1_RX	P0.11	
11	UART0_TX	UART0_TX	P0.06	
12	UART0_RX	UART0_RX	P0.07	
13	I2C_SDA	MikroE_SDA	P0.26	SDA
15	I2C_SCL	MikroE_SCL	P0.27	SCL
16	GPIO_8	MikroE_RESET	P0.31/AIN7	GPIO8
17	GPIO_2	MikroE_INT	P0.29/AIN5	GPIO2
18	GPIO_3	MikroE_PWM	P0.30/AIN6	GPIO3
19	GPIO_1	MikroE_AN	P0.03/AIN1	GPIO1
20	SPI_MOSI_EXT	MikroE_MOSI	P1.08	SPI_MOSI
21	SPI_MISO_EXT	MikroE_MISO	P0.21	SPI_MISO
22	SPI_CLK_EXT	mikroE_SPI_CLK	P1.09	SPI_CLK
23	GPIO_7	USER BUTTON	P1.03	GPIO7
24	NFC_2	NFC	P0.10/NFC2	NFC2
25	NFC_1	NFC	P0.09/NFC1	NFC1
27	GPIO_4	GPIO	P1.02	GPIO4
28	NRF52_SWDCLK	SWDCLK	SWDCLK	
29	GPIO_5	GPIO	P1.00	GPIO5
30	NRF52_SWDIO	SWDIO	SWDIO	
31	GPIO_6	RGB LED DIN	P0.22	GPIO6
32	NRF52_NRESET	nRESET	P0.18/RESET	
33	SPI_CS_EXT	mikroE_SPI_CS	P0.20	SPI_CS

11.2 Power Management

Power management features:

- System Standby Doze and Deep Sleep modes
- Open/Close peripherals (UART, SPI, I2C, SIO's, ADC, NFC). Peripherals consume current when open; each peripheral can be individually closed to save power consumption.
- Use of the internal DCDC (REG1) convertor or LDO (REG1) is decided by the underlying BLE stack.
- Pin wake-up system from deep sleep (including from NFC pins)

Power supply features:

- Supervisor hardware to manage power during reset, brownout, or power fail.
- 1.8V to 3.6V supply range for normal power supply (VBAT pin) using internal DCDC convertor (REG1) or LDO(REG1) decided by the underlying BLE stack.
- Integrated UWB radio current limiter for battery option.

11.3 NX040 Power Supply Options

The main power supply input to the NX040 is the VBAT module pin. It functions as the power supply for all digital I/Os and as the power supply input for the UWB chip current limiter.

11.3.1 External Regulated Supply

The NX040 series modules can be supplied by a regulated external supply, however the supply must have the capability to handle the >150mA current spikes during operation of the UWB radio. In this configuration, the regulated supply is connected to both the VBAT and VLIM supply inputs of the module. The current limiter operation available on the SR040 UWB radio is bypassed with this supply option.

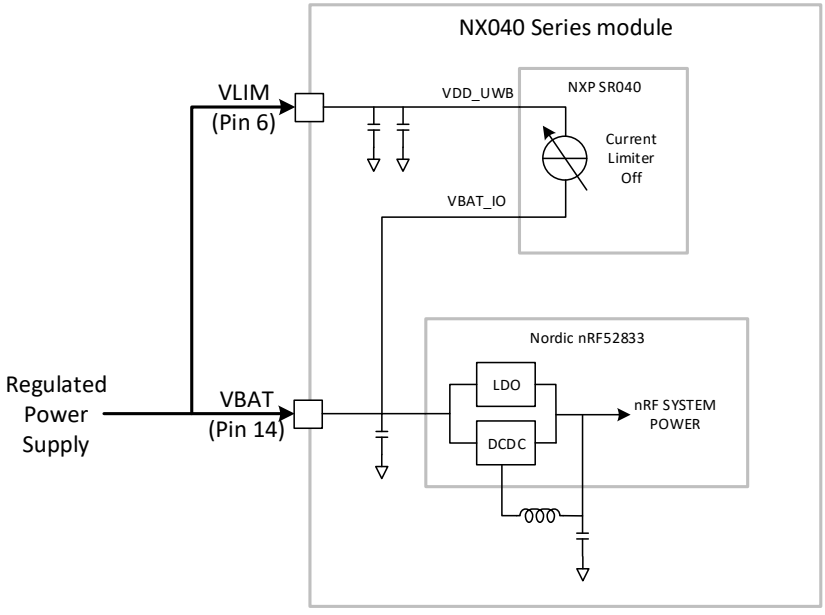


Figure 6: NX040 power supply block diagram with external regulated supply

Note: A NX040 module configured as a responder in a TWR configuration MUST use a regulated power supply or a power supply capable of handling current spikes of >150mA.

11.3.2 Battery Supply – Limited Peak Current Capability

In the case of the NX040 is supplied by a battery with limited peak current capability, the integrated current limiter must be enabled. The current limiter is connected between VBAT (pin) and VLIM (pin). With a battery, the battery is connected only to the VBAT supply pin of the NX040. The VLIM pin is left unconnected to separate the battery from the current peaks through the current limiter. Optionally, a bulk capacitor (>47uF) can be connected to the pin to provide additional surge current support of the UWB TX and RX limited duration spikes.

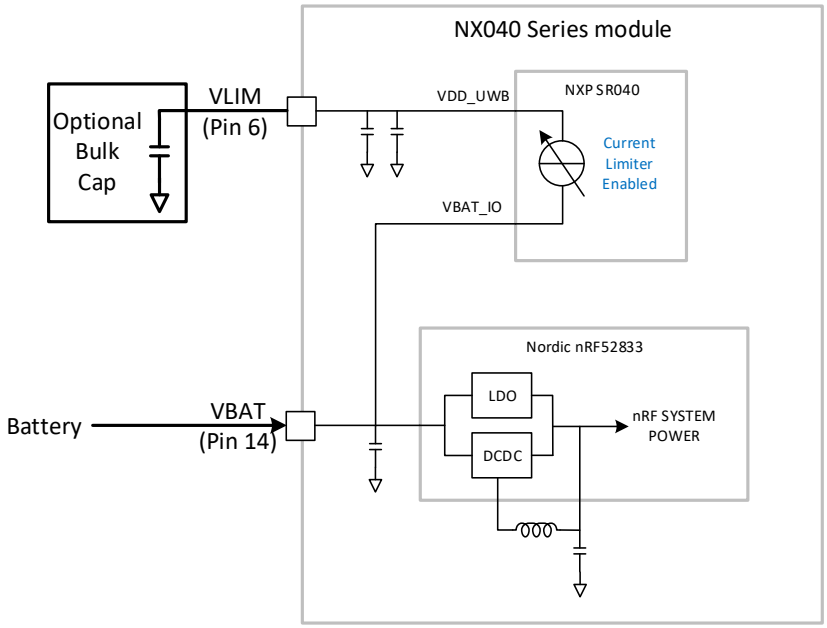


Figure 7: NX040 power supply block diagram with battery

11.3.3 Current Limiter Configuration

Use of the current limiter is intended for applications with a coin cell battery supply. The limit will maximize the battery lifetime by minimizing the peak current pulses drawn from the battery. The current limit is configurable in software.

- Configurable current limit from 5mA to 20mA, in steps of 1mA.
- The nRF52833 and all GPIO remain supplied by VBAT.
- When enabled, the current into VBAT_IO of the NXP SR040 is limited to the configured maximum.

The current limiter is connected between the module VBAT and VLIM pins. The VBAT current limit is configurable by software to between 5mA and 20mA, in steps of 1mA. A higher current setting will lead to a faster recharge of the buffer capacitors, enabling a shorter time between UWB ranging sequences.

The capacitance on the current limiter output (VLIM pin) is a critical component of the operation as the ranging energy is temporarily stored here. The NX040 includes 200uF of capacitance on the module. If additional surge current support is needed, additional external capacitance can be added externally on the VLIM pin. However, any additional capacitance will require a longer time to recharge, increasing the time needed between ranging sequences.

The user will need to perform measurements with different battery profiles to determine the best balance of additional buffer capacitance, slot time, current limiter values to achieve the use-case/battery lifetime desired.

11.4 System Clocks

The NX040 has integrated high accuracy 32 MHz (±10 ppm) crystal oscillator for use with radio operation and serving as the source for the 64 MHz HFXO system clock.

The NX040 also includes an integrated 32.768 kHz crystal to enable use of the LFXO crystal oscillator. This provides higher accuracy and lower power consumption in the StandByDoze and Deep Sleep modes of the MCU than with the on-chip 32.768 kHz LFRC oscillator.

11.5 UART Interface

Note: The NX040 has two UARTs.

The Universal Asynchronous Receiver/Transmitter (UART) on the NX040 provides:

- Baud Rates up to 1Mbps
- Full-duplex operation
- Automatic flow control
- Parity checking and generation for the 9th data bit.

Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and UART_CTS is an input and can be assigned to a module GPIO pin if used. Both are active low.

These signals operate according to normal industry convention. UART_RX, UART_TX, UART_CTS, UART_RTS are all 3.3 V level logic (tracks VBAT).

The module communicates with an external device using the following signaling format:

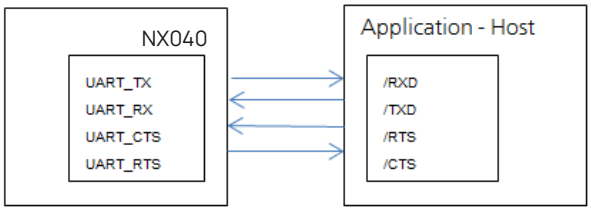


Figure 8: UART signals

Table 19: UART interfaces (default)

Signal Name	Pin No.	I/O
P0.06 / UART0_TX	11	O
P0.07 / UART0_RX	12	I
P0.16 / UART1_TX	4	O
P0.11/ UART1_RX	5	I

11.6 USB Interface

The NX040 has USB 2.0 FS (Full Speed, 12 Mbps) hardware capability. There is a CDC driver/Virtual UART as well as other USB drivers.

Table 20: USB interface

Signal Name	Pin No	I/O	Comments
USB_D+	1	I/O	
USB_D-	2	I/O	
USB_VBUS	3		When using the NX040 USB interface, connecting VBUS to the USB_VBUS pin is mandatory. **Note**: This does not power the NX040 module. You MUST power the rest of NX040 module circuitry through the VBAT (1.8 – 3.6V) pin.

11.7 SPI Bus

The NX040 series modules utilize a dedicated 6-wire SPI interface for operation and control of the SR040 UWB chipset. These nRF52833 pin assignments are fixed and MUST NOT be changed or re-purposed. These lines are embedded on the NX040 modules and not accessible.

Table 21: Dedicated UWB SPI interface assignments

nRF52833 Port	Function
P0.04	UWB_SPI_CLK
P0.05	UWB_SPI_MOSI
P0.17	UWB_SPI_MISO
P0.14	UWB_SPI_CS
P0.12	UWB_RDY_N
P0.15	UWB_INT_N

The NX040 modules provide a second dedicated 4-wire SPI Bus interface that is accessible through the module pins.

Table 22: External SPI interface (default)

Signal Name	Pin No	Comments
P1.08/SPI_MOSI_EXT	20	NX040 is the master device.
P0.21/SPI_MISO_EXT	21	
P1.09/SPI_CLK_EXT	22	
P0.20/SPI_CS_EXT	33	Implementation for the Ezurio Development board. SPI_CS can be implemented using any spare GPIO digital output pins to allow for multi-dropping.
P0.25	Not available	SPI_CS for the on module 8Mb flash. DO NOT change or re-purpose.

The 8Mb module flash shares this SPI bus and these nRF52833 pin assignments are fixed and MUST NOT be changed or re-purposed.

11.8 I2C Interface

The two-wire I2C interface can interface a bi-directional wired-OR bus with two lines (SCL, SDA) and has master /slave topology. The interface is capable of clock stretching. Data rates of 100 kbps and 400 kbps are supported.

IMPORTANT: It is essential to remember that pull-up resistors on both SCL and SDA lines are not provided in the module and MUST be provided external to the module.

Table 23: I2C interface (default)

Signal Name	Pin No
P0.26/I2C_SDA	13
P0.27/I2C_SCL	15

11.9 General Purpose I/O, ADC, PWM, and FREQ

11.9.1 GPIO

The 8 GPIO pins are configurable. They can be accessed individually. Each has the following user configured features:

- Input/output direction
- Output drive strength (standard drive 0.5 mA or high drive 5mA)
- Internal pull-up and pull-down resistors (13 K Ohms typical) or no pull-up/down or input buffer disconnect.
- Wake-up from high or low-level triggers on all pins including NFC pins.

11.9.2 ADC

The ADC is an alternate function on 4 of the available GPIO pins, configurable by software.

The NX040 provides access to 8-channel 8/10/12-bit successive approximation ADC in one-shot mode. This enables sampling up to 8 external signals through a front-end MUX. The ADC has configurable input and reference pre-scaling and sample resolution (8, 10, and 12 bit).

Table 24: NX040 available Analog interface pins

Signal Name	Pin No
P0.31/AIN7 – GPIO_8	16
P0.29/AIN5 – GPIO_2	17
P0.30/AIN6 – GPIO_3	18
P0.03/AIN1 – GPIO_1	19

11.9.3 PWM Signal Output on Up to 8 GPIO Pins

The PWM output is an alternate function on ALL (GPIO) pins, all of which are software configurable.

The **PWM output** signal has a frequency and duty cycle property. Frequency is adjustable (up to 1 MHz), and the duty cycle can be set over a range from 0% to 100%.

PWM output signal has a frequency and duty cycle property. PWM output is generated using dedicated hardware in the chipset.

11.9.4 FREQ Signal Output on Up to 8 GPIO Pins

The FREQ output is an alternate function on the 8 GPIO pins, all of which are software configurable.

Note: The frequency driving each of the 8 GPIO pins is the same, but the duty cycle can be independently set for each pin.

FREQ output signal frequency can be set over a range of 0Hz to 4 MHz (with 50% mark-space ratio).

11.10 nRESET Pin

Table 25: nRESET pin

Signal Name	Pin No	I/O	Comments
nRF52_nRESET	32	I	NX040 HW reset (active low). Pull the nRF52_nRESET pin low for minimum 100 mS for the NX040 to reset.

11.11 Two-Wire Interface SWD (JTAG)

Table 26: SWD Interface

Signal Name	Pin No	I/O	Comments
nRF52_SWDIO	30	I/O	Internal pull-up resistor
nRF52_SWDCLK	28	I	Internal pull-down resistor

The Ezurio development board incorporates an on-board SWD (JTAG) DAPLink programmer for this purpose.

The SWD (JTAG) connector MPN is as follows:

Reference	Part	Description and MPN (Manufacturers Part Number)
J15	FTSH-105	Header, 1.27mm, SMD, 10-way, FTSH-105-01-L-DV Samtech

Note: Reference on the NX040 development board schematic (Figure 9) shows the DVK development schematic wiring only for the SWD (JTAG) connector and the NX040 module JTAG pins.

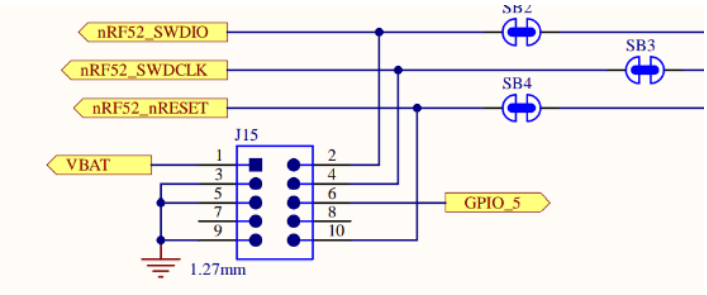


Figure 9: NX040 development board SWD schematic

A SWD (JTAG) is required to load firmware on the module. It is strongly recommended to bring the SWD (JTAG) interface to a header or test pads on your host design so you can update module firmware. You can wire out the JTAG (2-wire SWD interface) on your host design (see Figure 9, where the following four lines should be wired out – SWDIO, SWDCLK, GND, and VBAT).

11.12 NFC Interface

The Sera NX040 series modules and the nRF52833 offer an NFC peripheral:

- Based on the NFC forum specification
  - 13.56 MHz
  - Date rate 106 kbps
  - NFC Type2 and Type4 tag emulation
- Modes of operation:
  - Disable
  - Sense
  - Activated

11.12.1 Use Cases

- Touch-to Pair with NFC
- Launch a smartphone app (on Android)
- NFC enabled Out-of-Band Pairing
- System Wake-On-Field function (SENSE)
  - Proximity Detection

Table 27: NFC interface

Signal Name	Pin No	I/O	Comments
NFC_1	25	I/O	The NFC pins are by default NFC pins and an alternate function on each pin is GPIO.
NFC_2	24	I/O	

11.12.2 NFC Antenna Coil Tuning Capacitors

From Nordic's *nRF52833 Product Specification v1.5*: infocenter.nordicsemi.com/pdf/nRF52833_PS_v1.5.pdf

The NFC antenna coil must be the connected differential between the NFC_1 and NFC_2 pins of the NX040. Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz (Figure 10).

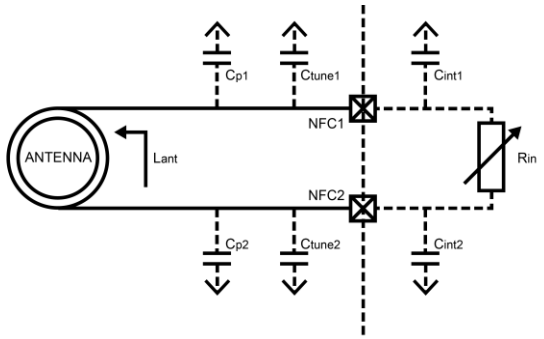


Figure 10: NFC antenna coil tuning capacitors

The required external tuning capacitor value is given by the following equation:

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56\ MHz)^2 \cdot \mathrm{L}_{ant}} - C_p - C_{int}$$

An antenna inductance of Lant = 0.72 uH provides tuning capacitors in the range of 300 pF on each pin. The total capacitance on NFC1 and NFC2 must be matched. Cint and Cp are small usually (Cint is 4pF), so can be omitted from calculation.

Battery Protection Note: If the NFC coil antenna is exposed to a strong NFC field, the supply current may flow in the opposite direction due to parasitic diodes and ESD structures. If the used battery does not tolerate a return current, a series diode must be placed between the battery and the NX040 to protect the battery.

11.13 Unavailable nRF52833 pins

The NX040 series modules do not have the following Nordic nRF52833 chipset pins brought out and these ports are not accessible or available for use.

Table 28: Unavailable nRF52833 pins

nRF52833-CJAA Chipset Pin Name
P0.02/AIN0
P0.08
P0.13 (See Note 1)
P0.19
P0.23
P0.24
P0.28/AIN4
P1.01
P1.04 (See Note 1)
P1.05
P1.06

Pin Notes:

Note 1	P0.13 and P1.04 are reserved for GPIO connections to UWB chipset on the module.

12 Hardware Integration Guidance

12.1 On-board PCB Antenna Characteristics

The **453-00175** module contains separate on-board PCB trace monopole antennas for the UWB (6.25 – 8.25 GHz) and the BLE (2.4 – 2.48 GHz) radios. The radiated performance of these antennas depends on the host PCB layout.

The NX040 development board was used for the 453-00175 PCB antenna performance evaluation. To obtain similar performance, follow the guidelines in section *PCB Layout on Host PCB for the 453-00175* to allow the on-board PCB antenna to radiate and reduce proximity effects due to nearby host PCB GND copper or metal covers.

12.1.1 UWB PCB Planar Monopole Antenna performance

Table 29: UWB PCB Antenna Performance

453-00175 PCB trace UWB antenna	Peak Gain	Avg. Gain	Efficiency
Channel 5 = 6489.6 MHz	2.69 dBi	-1.12 dBi	77.3%
Channel 9 = 7987.2 MHz	3.44 dBi	-1.21 dBi	75.7%

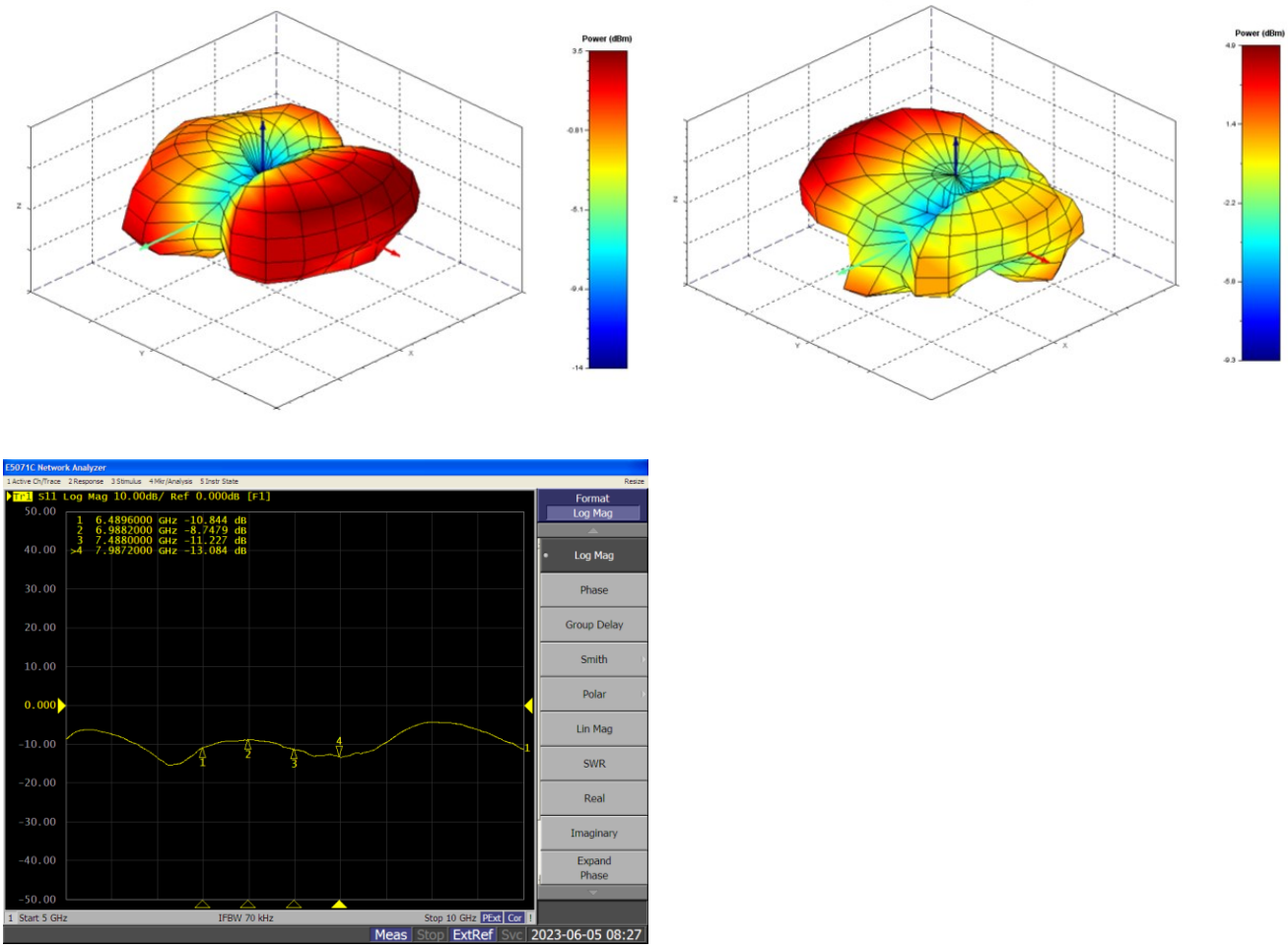


Figure 11: 453-00175 on-board PCB UWB antenna performance (Antenna Gain and S11 – whilst 453-00175 module sitting on Devboard 453-00175-K1)

12.1.2 BLE PCB Trace Antenna performance

Table 30: BLE PCB Antenna Performance

453-00175 PCB trace BLE antenna	Peak Gain	Avg. Gain	Efficiency
2402 MHz	-0.38 dBi	-5.60 dBi	27.5%
2440 MHz	0.73 dBi	-4.61 dBi	34.6%
2480 MHz	0.55 dBi	-4.60 dBi	34.7%

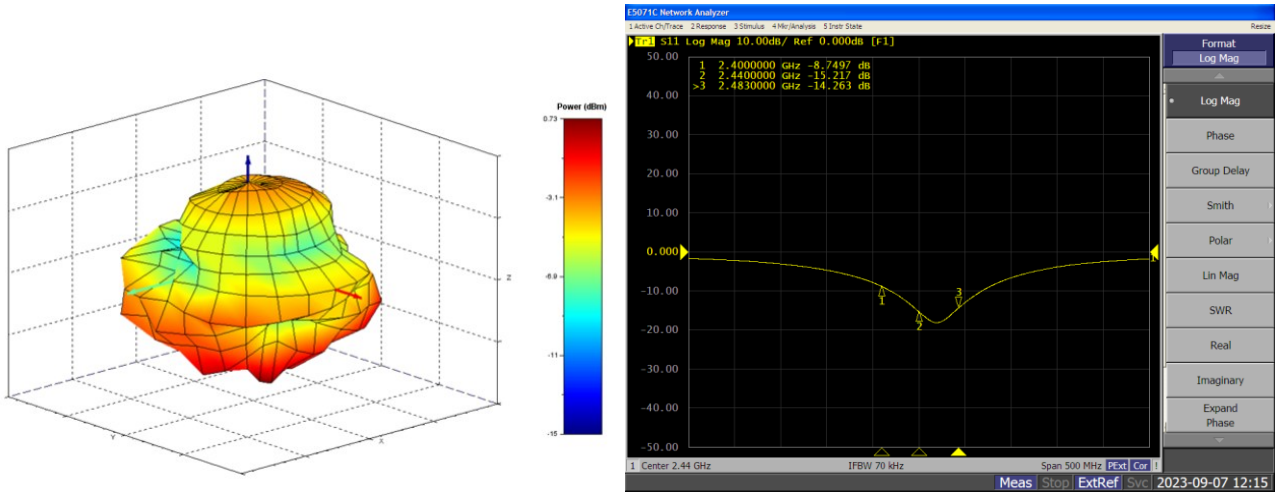


Figure 12: 453-00175 on-board PCB BLE antenna performance (Antenna Gain @ 2440MHz and S11 – whilst 453-00175 module sitting on Devboard 453-00175-K1)

12.2 Circuit Recommendations

The NX040 is easy to integrate, requiring no external components on your board apart from those which you require for development and in your end application.

The following are suggestions for your design for the best performance and functionality.

Checklist (for Schematic):

- **NX040 power supply options:**

  Option 1 – External regulated supply. Connect external supply within 1.8V to 3.6V range to NX040 VBAT and VLIM pins.

  OR

  Option 2 – Battery supply. Connect battery supply to NX040 VBAT pin. NX040 VLIM pin is left unconnected or additional bulk capacitance is added as described in Battery Supply – Limited Peak Current Capability.

  For either option, if you use the USB interface then the NX040 VBUS pin must be connected to external supply within the range 4.35V to 5.5V.

  Note: A NX040 module configured as a responder in a Two-Way Ranging application MUST use an external regulated supply (Option 1).

  The external power source should be within the operating range, rise time and noise/ripple specification of the NX040. Add decoupling capacitors for filtering the external source. The Power-on reset circuitry within NX040 series module incorporates brown-out detector, thus simplifying the power supply design. Upon application of power, the internal power-on reset ensures that the module starts correctly.

- **AIN (ADC) and SIO pin IO voltage levels**

  NX040 SIO voltage levels are at VBAT. Ensure input voltage levels into SIO pins are at VBAT also (particularly if the supply source is a battery whose voltage will drop). Ensure ADC pin maximum input voltage for damage is not violated.

- **JTAG (SWD)**

  This is REQUIRED for loading flash images which can only be loaded using the SWD (JTAG) interface.

Recommend that you place JTAG (2-wire interface) to provide additional capability to handle future NX040 module firmware upgrades. Recommend placing the JTAG (2-wire interface) on your host design (see Figure 9 where four lines should be wired out, namely SWDIO, SWDCLK, GND and VBAT). Firmware upgrades can also be performed over the NX040 UART interface.

- **UART**

  A connector can be added to allow interfacing with UART via PC (UART–RS232 or UART-USB).

- **I2C**

  It is essential to remember that pull-up resistors on both I2C_SCL and I2C_SDA lines are not provided in the NX040 module and MUST be provided external to the module as per I2C standard.

- **SPI**

  Implement SPI chip select using any unused GPIO pin within your application then SPI_CS is controlled from the software application allowing multi-dropping.

- **NFC antenna connector**

  To make use of the Ezurio flexi-PCB NFC antenna, fit connector:

  - Description – FFC/FPC Connector, Right Angle, SMD/90d, Dual Contact,1.2 mm Mated Height
  - Manufacturer – Molex
  - Manufacturers Part number – 512810598

  Add tuning capacitors of 300 pF on NFC1 pin to GND and 300 pF on NFC2 pins to GND if the PCB track length is similar as development board.

- **nRESET pin (active low)**

  Hardware reset. Wire out to push button or drive by host.
  By default module is out of reset when power applied to VBAT pin.

12.3 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate NX040 module close to the edge of PCB (mandatory for the 453-00175 for on-board PCB trace antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect the copper flood to the inner GND plane. If GND flood copper is on the bottom of the module, then connect it with GND vias to the inner GND plane.
- Route traces to avoid noise being picked up on VBAT, VLIM, VBUS supply and AIN (analog) and SIO (digital) traces.
- Ensure no exposed copper is on the underside of the module (refer to land pattern of NX040 development board).

12.4 PCB Layout on Host PCB for the 453-00175

12.4.1 Antenna Keep-Out on Host PCB

The 453-00175 has integrated PCB trace antennas and their performance is sensitive to host PCB. It is critical to locate the 453-00175 on the edge of the host PCB to allow the antennas to radiate properly. Refer to guidelines in section ***PCB land pattern and antenna keep-out area for the 453-00175***. Some of those guidelines repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the 453-00175 module on the edge of the host PCB, preferably in the edge center.
- The NX040 development board has the 453-00175 module on the edge of the board (not in the corner). The antenna keep-out area is defined by the NX040 development board which was used for module development and antenna performance evaluation is shown in Figure 13, where the antenna keep-out area is 10.5 mm high, 53.5 mm wide; with PCB dielectric (no copper) height 1.6 mm sitting under the 453-00175 PCB trace antenna.
- The 453-00175 module on-board PCB trace antennas are tuned when the 453-00175 is sitting on development board (host PCB) with size of 85.6 mm x 53.5 mm x 1.6 mm. The development board PCB extends 3.1 mm beyond the edge of the 453-00175 module. This PCB extension is not required, and removal will have a small effect on the antenna.
- A different host PCB thickness dielectric will have small effect on antenna.

- Further antenna-keep-out is defined in the Host PCB Land Pattern and Antenna Keep-out for the 453-00175 section.

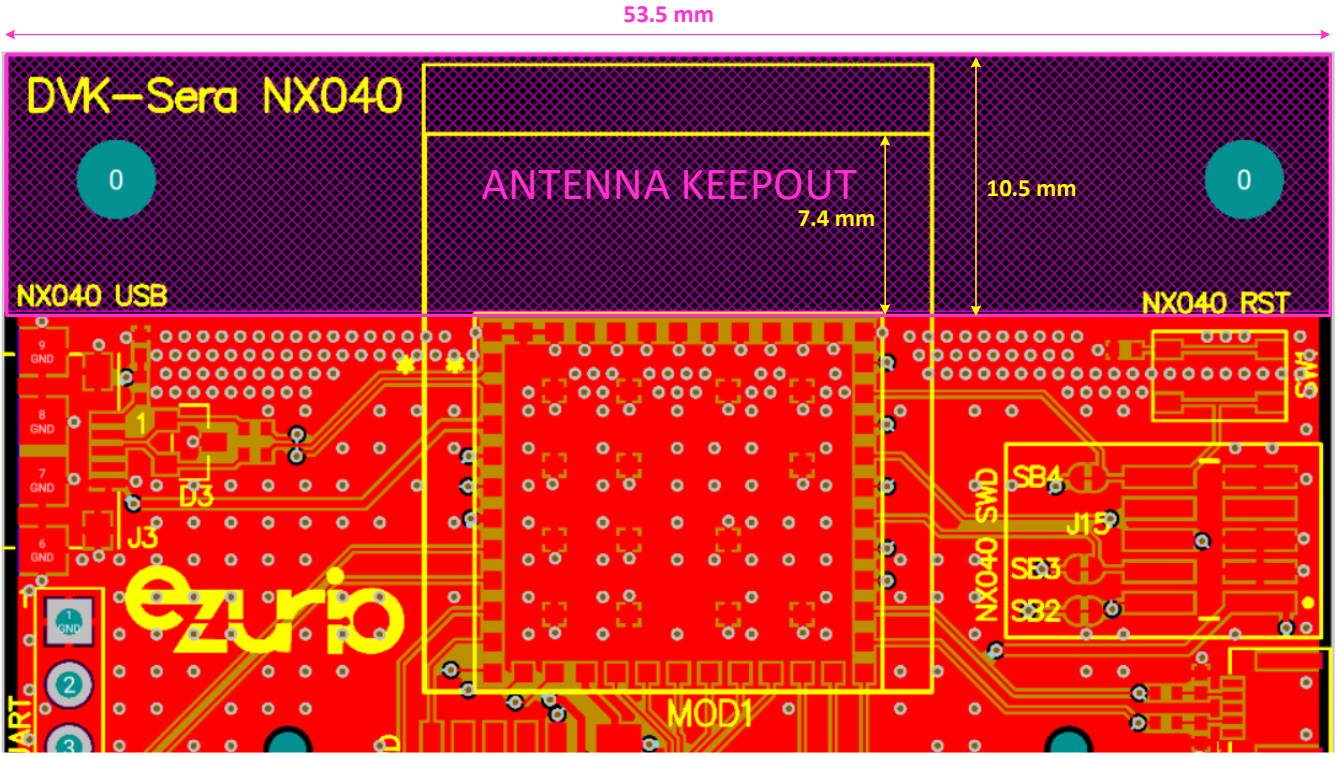


Figure 13: PCB trace Antenna keep-out area (cross-hatched), top edge of the NX040 development board for the 453-00175 module.

12.4.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00175

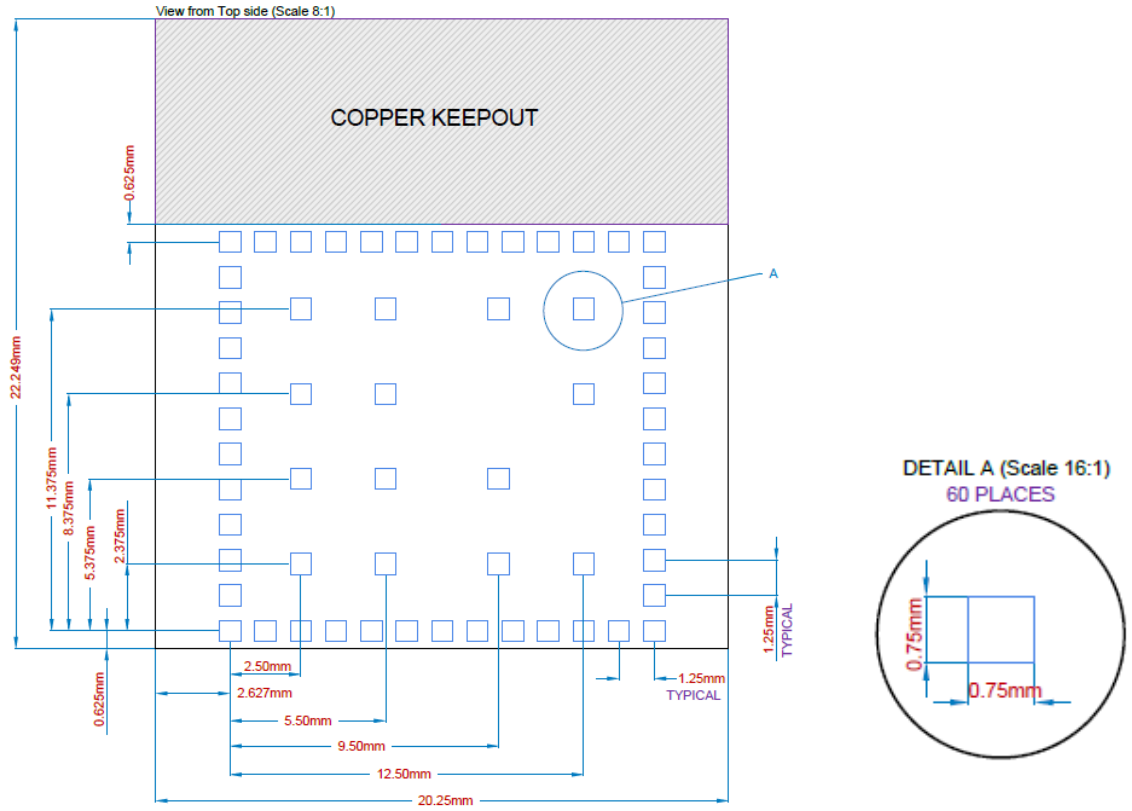


Figure 14: Land pattern and Keep-out for the 453-00175

Host PCB Land Pattern and Antenna Keep-out for the 453-00175 Notes:	
Note 1	Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear of the area (Refer to Antenna Keep-Out and Proximity to Metal or Plastic) to reduce effects of proximity detuning the antenna and to help antenna radiate properly.
Note 2	For the best on-board antenna performance, the module 453-00175 MUST be placed on the edge of the host PCB and preferably in the edge center of the host PCB, with the antenna "Keep Out Area" is extended on the host PCB as in Figure 13.
Note 3	Ensure that there is no exposed copper under the module on the host PCB.
Note 4	You may modify the PCB land pattern dimensions based on their experience and/or process capability.

12.4.3 Antenna Keep-Out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the 453-00175 PCB trace antennas (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of that degradation is entirely system dependent, meaning you will need to perform some testing with your host application.
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic).

12.5 External Antenna Integration with 453-00174

Please refer to the regulatory sections for FCC, ISED, EU, RCM, KC, and Japan for details of use of NX040-with external antennas in each regulatory region.

Note: In countries where EU/CE compliance is applicable, the BLE RX transmit power CANNOT be set higher than +5 dBm during operation to meet the BLE RF transmit EIRP requirement of +10dBm.

The NX040 family has been designed to operate with the below external antennas. The required antenna impedance is 50 ohms. External antennas improve radiation efficiency.

Table 31: External antennas for the NX040

Model	Type	Connector	Frequencies / Peak Gain (dBi)
Ezurio NanoBlue EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2400 – 2500 MHz / 2 dBi
Ezurio FlexPIFA 001-0022	PIFA	IPEX MHF4	2400 – 2480 MHz / 2 dBi
Mag Layers EDA-8709-2G4C1-B27 0600-00057	Dipole	IPEX MHF4	2400 – 2480 MHz / 2 dBi
Ezurio mFlexPIFA EFA2400A3S-10MH4L	PIFA	IPEX MHF4	2400 – 2480 MHz / 2 dBi
Ezurio EFG2400A3S-10MH4L	PIFA	IPEX MHF4L	2400 – 2500 MHz / 3.1 dBi
Ezurio NanoUWB EUB5850A3S-10MHL4	PCB Monopole	IPEX MHF4L	5850 – 8250 MHz / 3.5 dBi
Ezurio NFC 0600-00061	NFC spiral	N/A	-

Warning: The NX040 453-00174 module has been calibrated for use with the Ezurio NanoUWB external antenna exclusively. If a different external UWB antenna is used, the reported ranging distances will be incorrect. Please contact Ezurio for guidance on module re-calibration.

13 Mechanical

13.1 Sera NX040 Mechanical Details

Tolerances

Board Outline:+/-0.13mm
Board Height:+/-0.15mm

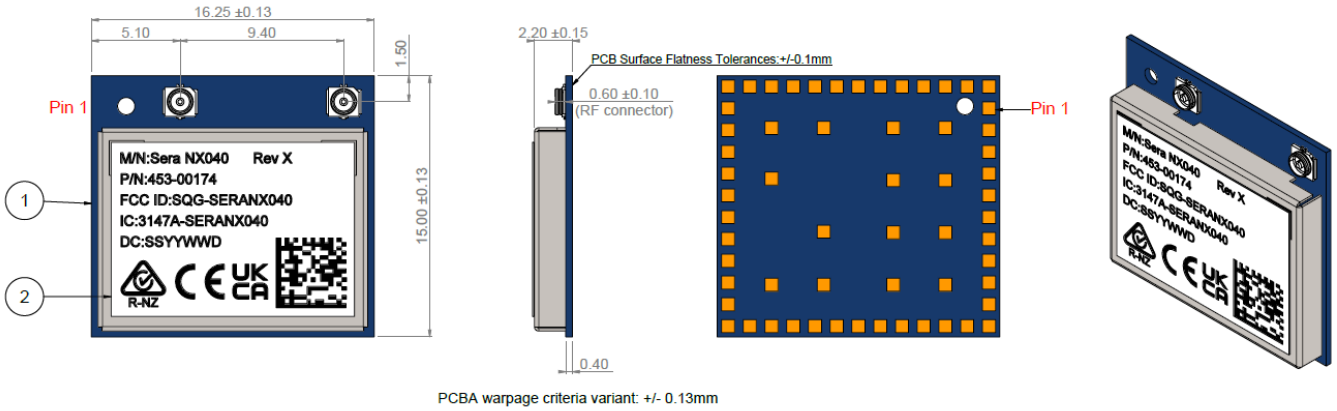


Figure 15: Mechanical Details - MHF4L Variant

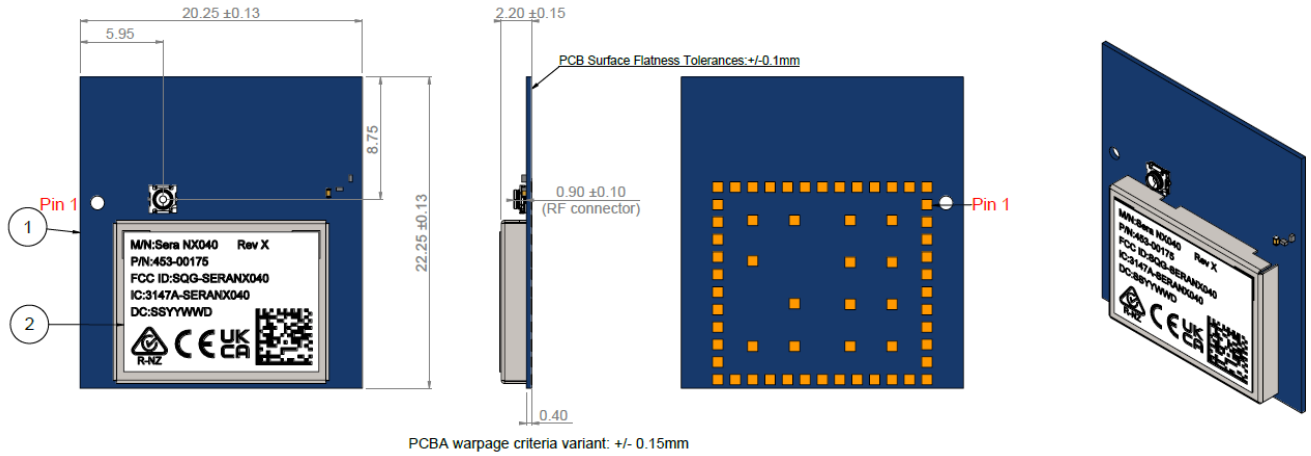


Figure 16: Mechanical Details - Trace Antenna Variant

Development kit schematics can be found in the downloads tab of the NX040 product page.

14 Application Note for Surface Mount Modules

14.1 Introduction

Ezurio's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

Sera NX040 part numbers – 453-00174**R** and 453-00175**R** are shipped as Tape / Reel, with a reel containing 500 pcs.

14.2 Shipping

14.2.1 Module Packaging Configuration

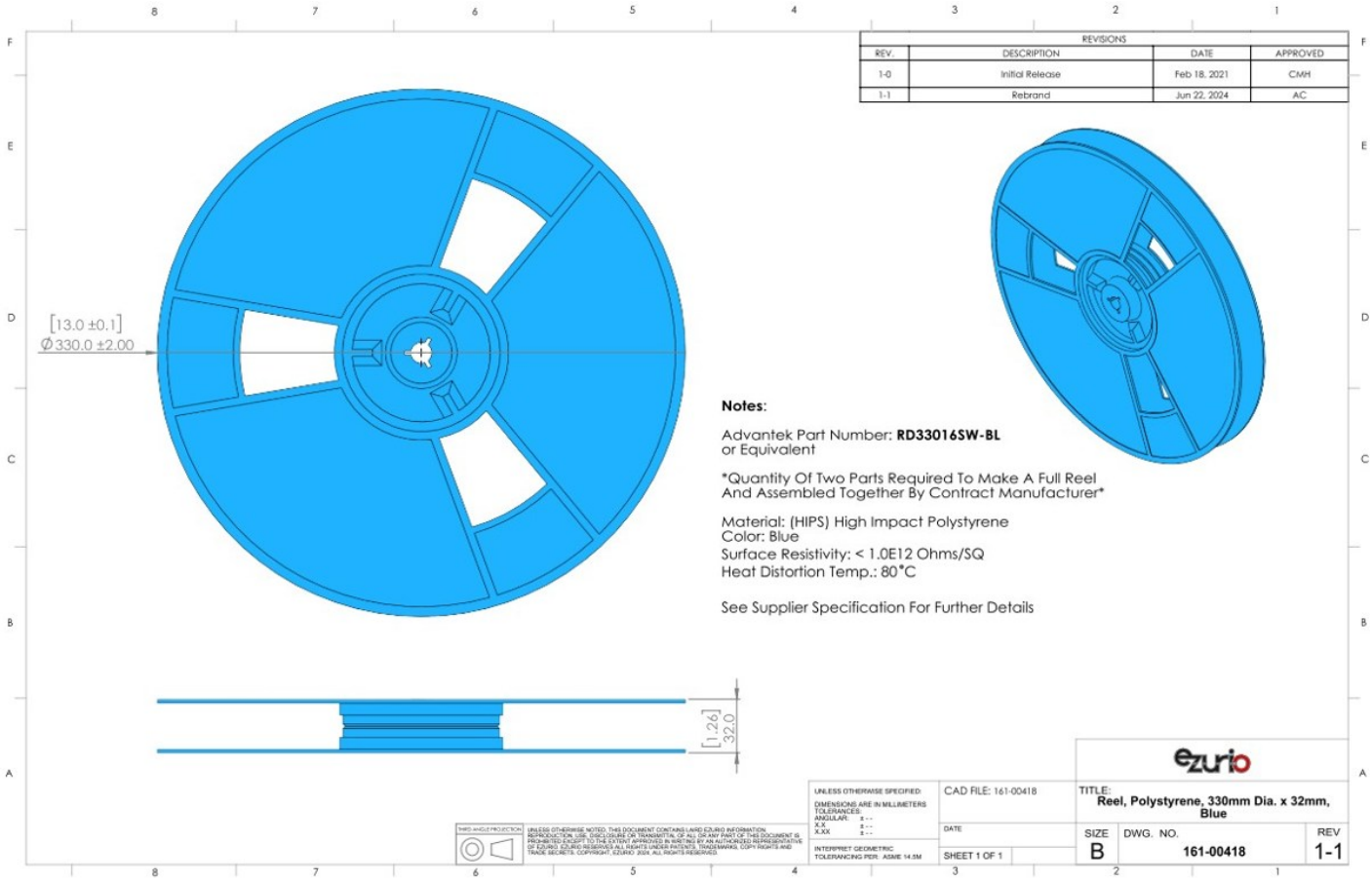


Figure 17: Reel Specifications, 500 pieces per reel.

Figure 18: Carrier Tape Specifications for the MHF4L Variant.

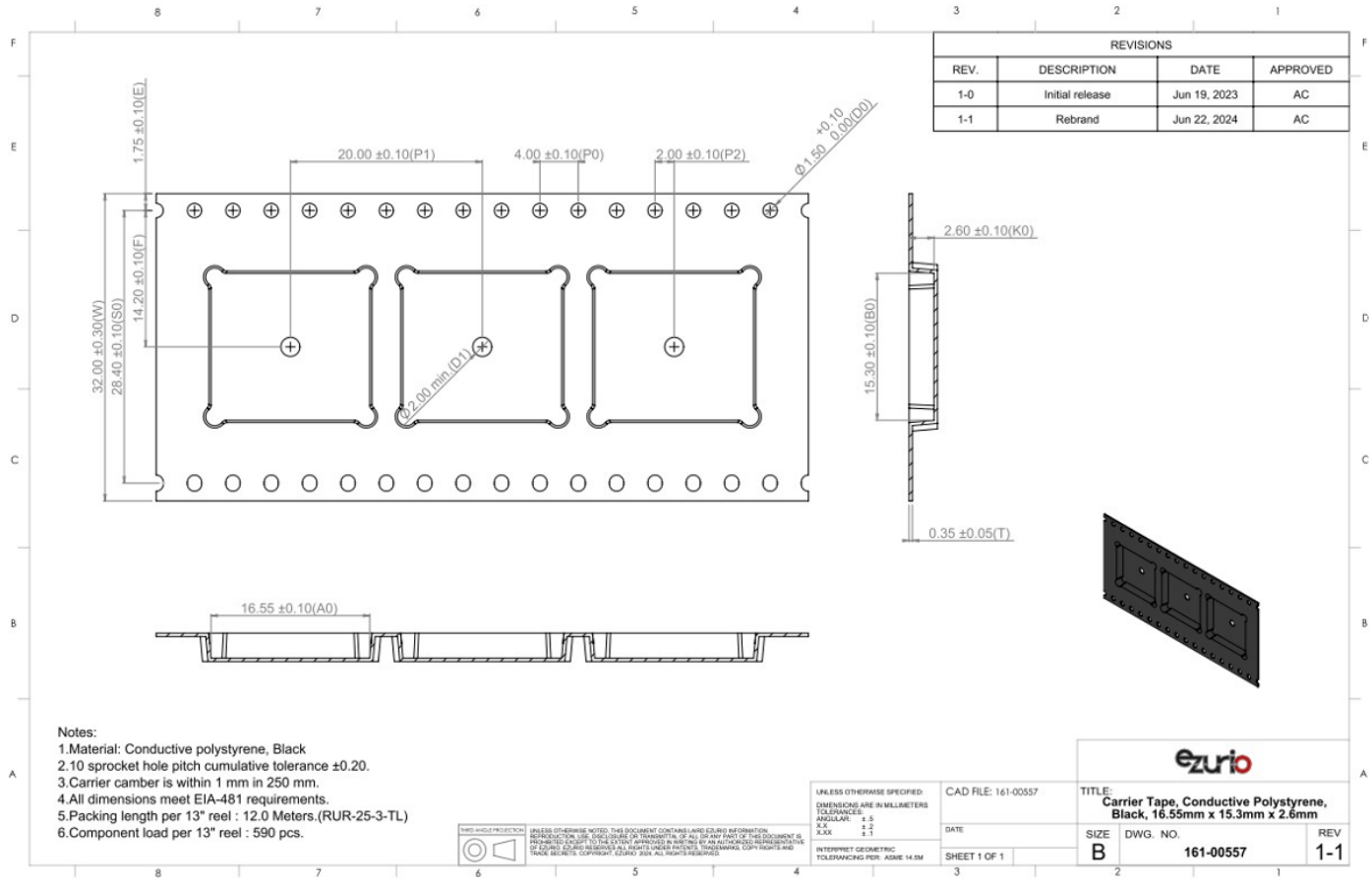
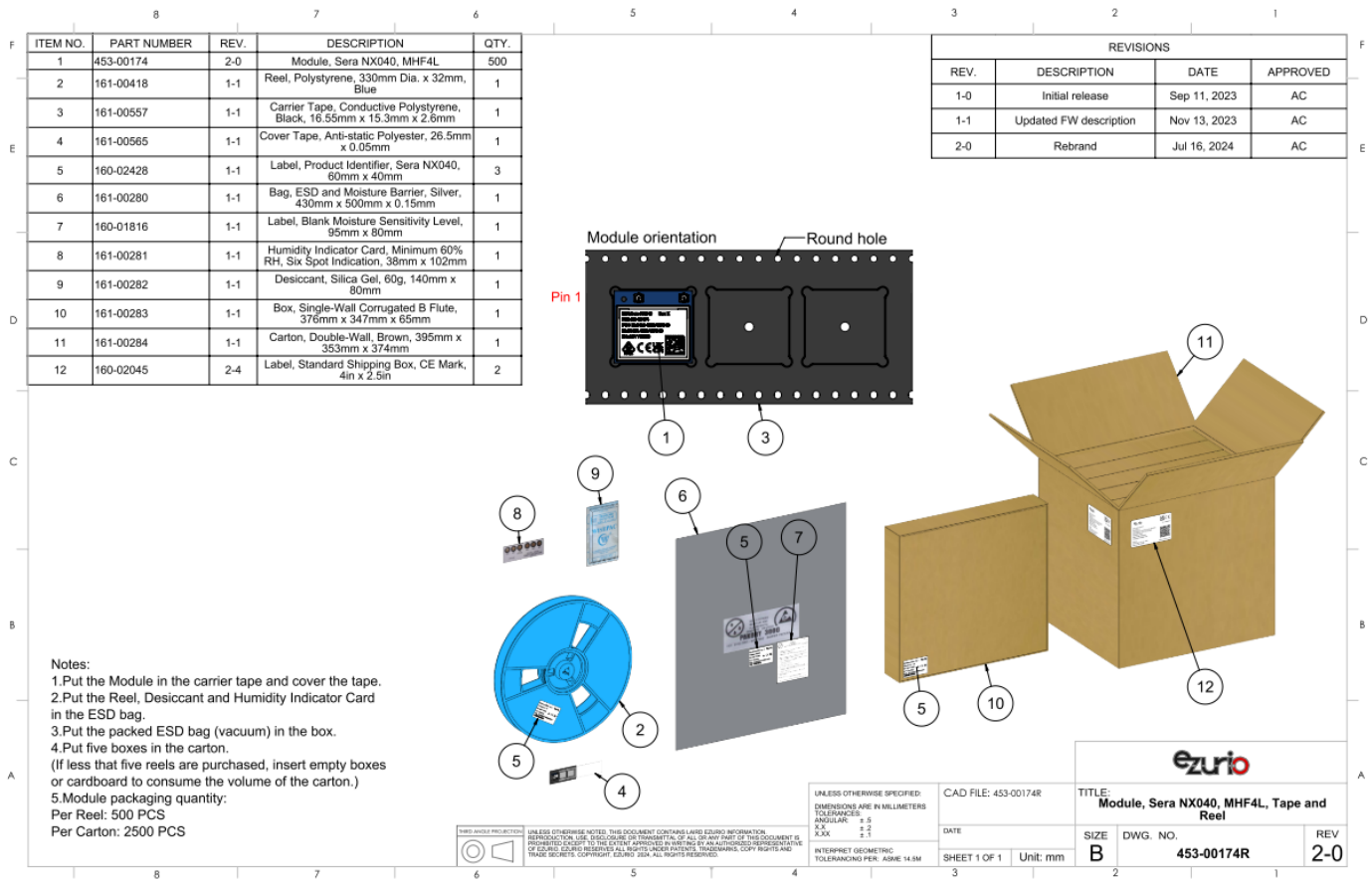


Figure 19: Carrier Tape Specifications for Trace Antenna Variant.



ITEM NO.	PART NUMBER	REV.	DESCRIPTION	QTY.
1	453-00174	2-0	Module, Sera NX040, MHF4L	500
2	161-00418	1-1	Reel, Polystyrene, 330mm Dia. x 32mm, Blue	1
3	161-00557	1-1	Carrier Tape, Conductive Polystyrene, Black, 16.55mm x 15.3mm x 2.6mm	1
4	161-00565	1-1	Cover Tape, Anti-static Polyester, 26.5mm x 0.05mm	1
5	160-02428	1-1	Label, Product Identifier, Sera NX040, 60mm x 40mm	3
6	161-00280	1-1	Bag, ESD and Moisture Barrier, Silver, 430mm x 500mm x 0.15mm	1
7	160-01816	1-1	Label, Blank Moisture Sensitivity Level, 95mm x 80mm	1
8	161-00281	1-1	Humidity Indicator Card, Minimum 60% RH, Six Spot Indication, 38mm x 102mm	1
9	161-00282	1-1	Desiccant, Silica Gel, 60g, 140mm x 80mm	1
10	161-00283	1-1	Box, Single-Wall Corrugated B Flute, 376mm x 347mm x 65mm	1
11	161-00284	1-1	Carton, Double-Wall, Brown, 395mm x 353mm x 374mm	1
12	160-02045	2-4	Label, Standard Shipping Box, CE Mark, 4in x 2.5in	2

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1-0	Initial release	Sep 11, 2023	AC
1-1	Updated FW description	Nov 13, 2023	AC
2-0	Rebrand	Jul 16, 2024	AC

Figure 20: Sera NX040 Packaging Process for MHF4L Variant

There are 500 x Sera NX040 MHF4L modules taped in a reel (and packaged in a pizza box) and five boxes per carton (2,500 modules per carton). Reel, boxes, and carton are labeled with the appropriate labels.

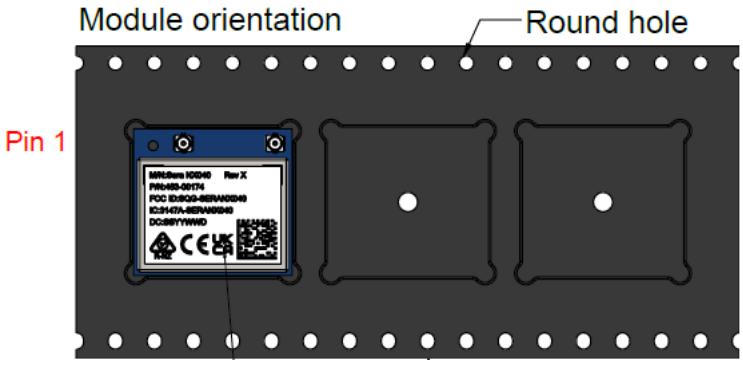
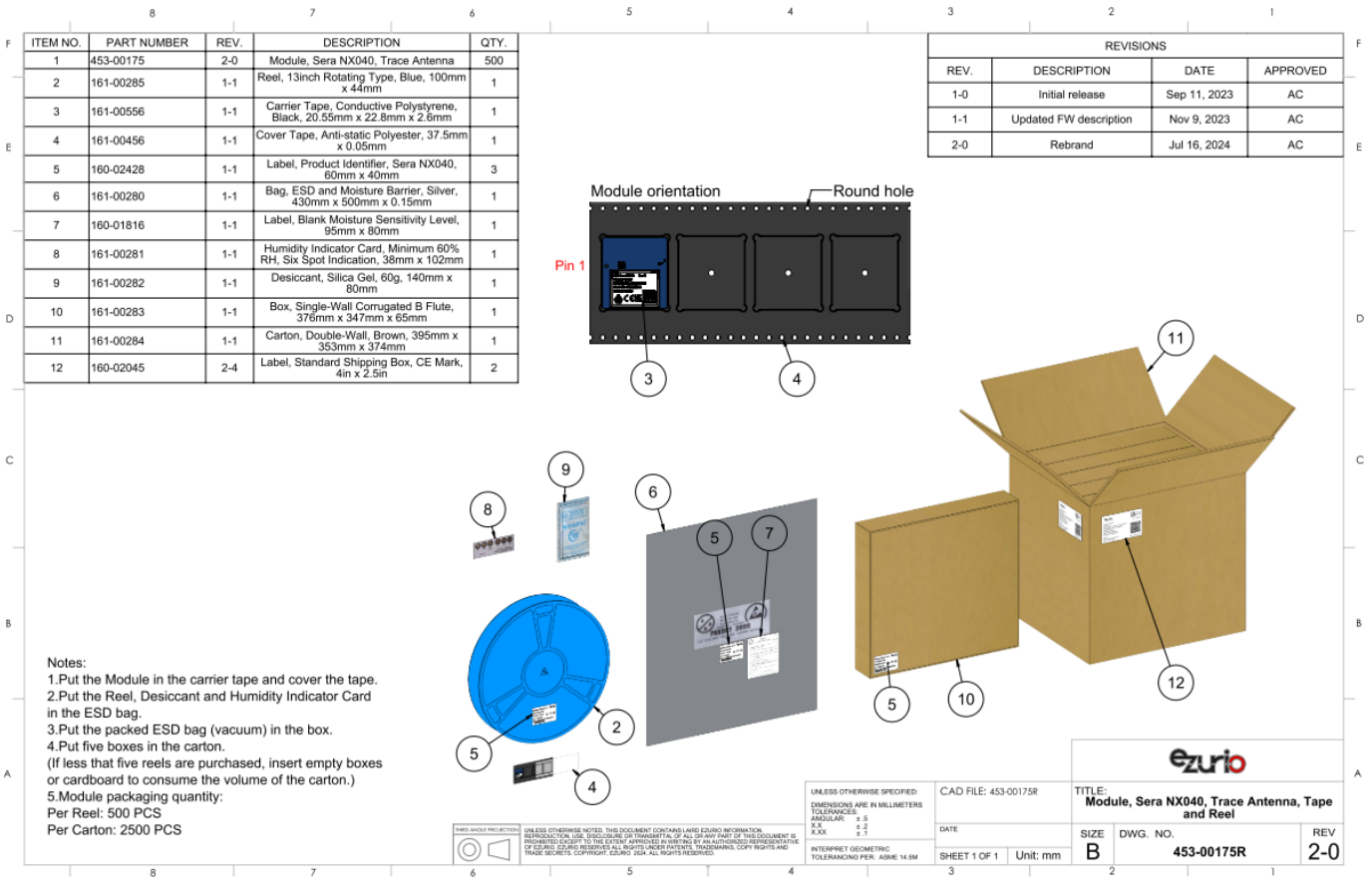


Figure 21: Module Orientation in Carrier Tape Pocket, MHF4L Variant. MHF4L receptacle close to Tape Sprocket Hole side.



ITEM NO.	PART NUMBER	REV.	DESCRIPTION	QTY.
1	453-00175	2-0	Module, Sera NX040, Trace Antenna	500
2	161-00285	1-1	Reel, 13inch Rotating Type, Blue, 100mm x 44mm	1
3	161-00556	1-1	Carrier Tape, Conductive Polystyrene, Black, 20.55mm x 22.8mm x 2.6mm	1
4	161-00456	1-1	Cover Tape, Anti-static Polyester, 37.5mm x 0.05mm	1
5	160-02428	1-1	Label, Product Identifier, Sera NX040, 60mm x 40mm	3
6	161-00280	1-1	Bag, ESD and Moisture Barrier, Silver, 430mm x 500mm x 0.15mm	1
7	160-01816	1-1	Label, Blank Moisture Sensitivity Level, 95mm x 80mm	1
8	161-00281	1-1	Humidity Indicator Card, Minimum 60% RH, Six Spot Indication, 38mm x 102mm	1
9	161-00282	1-1	Desiccant, Silica Gel, 60g, 140mm x 80mm	1
10	161-00283	1-1	Box, Single-Wall Corrugated B Flute, 376mm x 347mm x 65mm	1
11	161-00284	1-1	Carton, Double-Wall, Brown, 395mm x 353mm x 374mm	1
12	160-02045	2-4	Label, Standard Shipping Box, CE Mark, 4in x 2.5in	2

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1-0	Initial release	Sep 11, 2023	AC
1-1	Updated FW description	Nov 9, 2023	AC
2-0	Rebrand	Jul 16, 2024	AC

CAD FILE: 453-00175R	TITLE: Module, Sera NX040, Trace Antenna, Tape and Reel			
DATE	SIZE B	DWG. NO. 453-00175R	REV 2-0	
SHEET 1 OF 1	Unit: mm			

Figure 22: Sera NX040 Packaging Process for Trace Antenna Variant

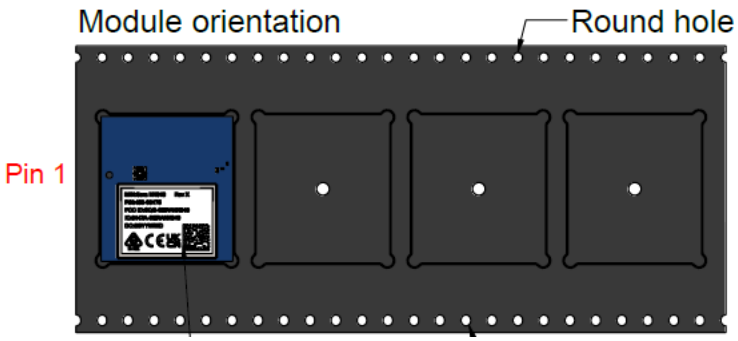


Figure 23: Module Orientation in Carrier Tape Pocket, Trace Antenna Variant. Antenna end of Module close to Tape Sprocket Hole side)

There are 500 x Sera NX040 Trace Antenna modules taped in a reel (and packaged in a pizza box) and five boxes per carton (2,500 modules per carton). Reel, boxes, and carton are labeled with the appropriate labels.

14.2.2 Labeling

All modules are shipped in tape and reel package and sealed in ESD Bags. The Sera NX040 solder-down modules are classified as MSL4 devices.

The following labels are located on the antistatic bag:

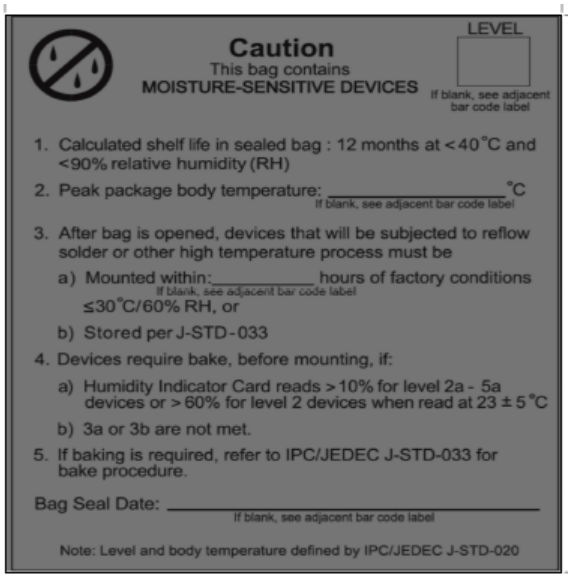


Figure 24: Moisture Sensitivity Level Label

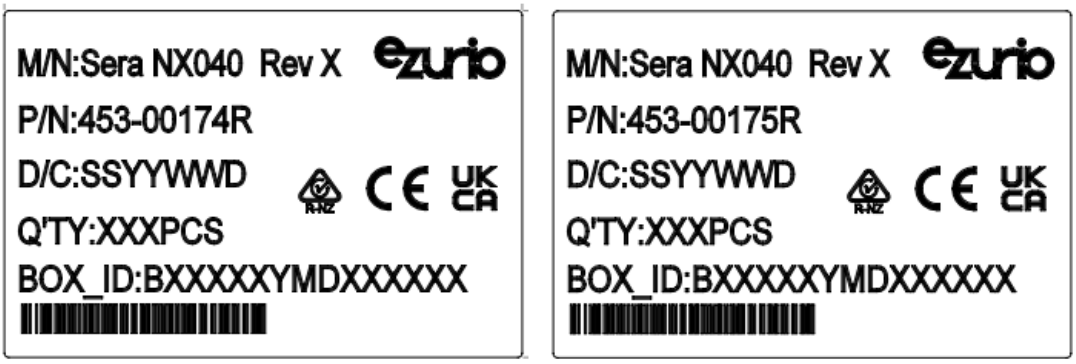


Figure 25: Product Identifier Label

The following labels are placed on the pizza box.

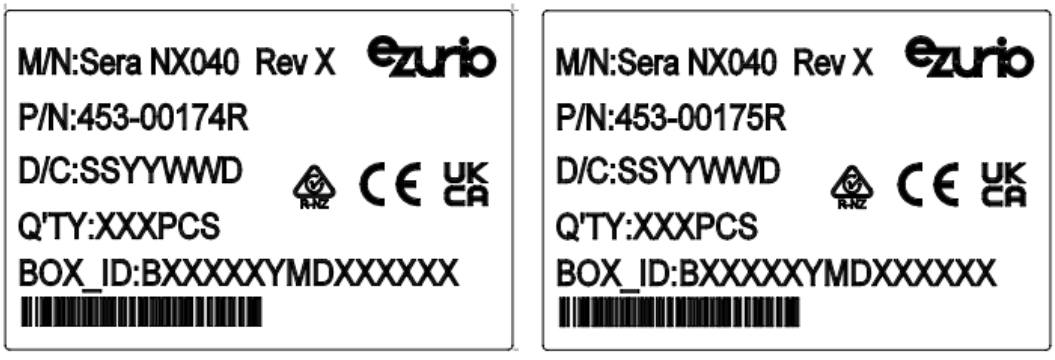


Figure 26: Product Identifier Label

The following labels are placed on the master shipping carton.

Figure 27: Product Identifier Label

14.3 Reflow Parameters

Prior to any reflow, it is important to ensure the modules were packaged to prevent moisture absorption. New packages contain desiccate (to absorb moisture) and a humidity indicator card to display the level maintained during storage and shipment. If directed to *bake units* on the card, see Table 32 and follow instructions specified by IPC/JEDEC J-STD-033. A copy of this standard is available from the JEDEC website: http://www.jedec.org/sites/default/files/docs/jstd033b01.pdf

Any modules not manufactured before exceeding their floor life should be re-packaged with fresh desiccate and a new humidity indicator card. Floor life for MSL (Moisture Sensitivity Level) 4 devices is 72 hours in ambient environment ≤30°C/60%RH.

Table 32: Recommended baking times and temperatures

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
4	11 hours	7 hours	37 hours	23 hours	15 days	9 days

Ezurio surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. Ezurio surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

Important: During reflow, modules should not be above 260° and not for more than 30 seconds. In addition, we recommend that the NX040 module **does not** go through the reflow process more than one time; otherwise, the NX040 internal component soldering may be impacted.

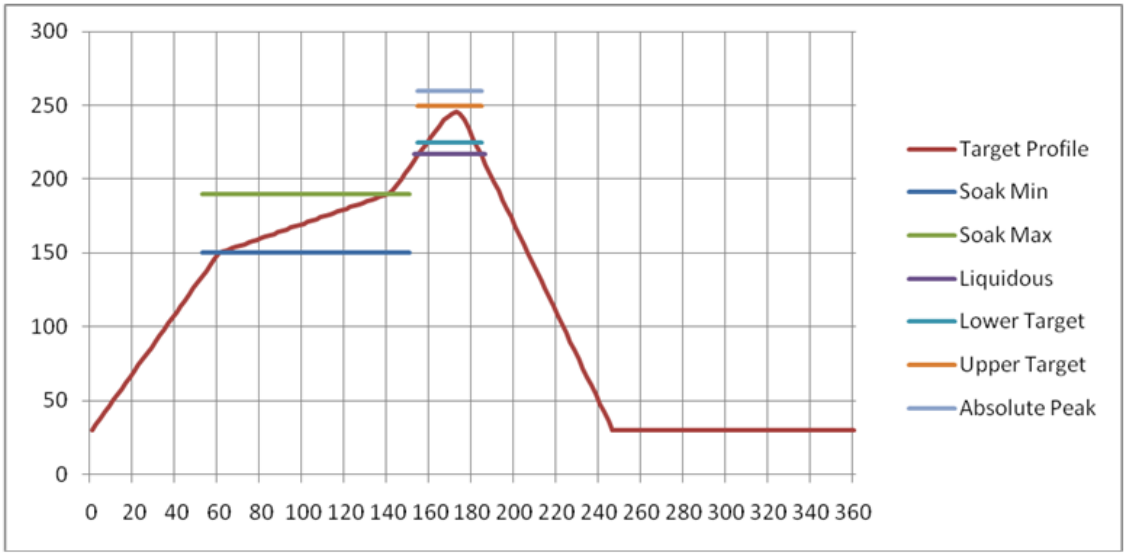


Figure 28: Recommended reflow temperature

Temperatures should not exceed the minimums or maximums presented in Table 33.

Table 33: Recommended maximum and minimum temperatures

Specification	Value	Unit
Temperature Inc./Dec. Rate (max)	1~3	°C / Sec
Temperature Decrease rate (goal)	2-4	°C / Sec
Soak Temp Increase rate (goal)	.5 - 1	°C / Sec
Flux Soak Period (Min)	70	Sec
Flux Soak Period (Max)	120	Sec

Specification	Value	Unit
Flux Soak Temp (Min)	150	°C
Flux Soak Temp (max)	190	°C
Time Above Liquidous (max)	70	Sec
Time Above Liquidous (min)	50	Sec
Time In Target Reflow Range (goal)	30	Sec
Time At Absolute Peak (max)	5	Sec
Liquidous Temperature (SAC305)	218	°C
Lower Target Reflow Temperature	240	°C
Upper Target Reflow Temperature	250	°C
Absolute Peak Temperature	260	°C

15 Reliability Test

15.1 Climatic And Dynamic Reliability Test

Table 34: Climatic and Dynamic Reliability Test Results for Sera NX040 Modules

Test Item	Specification	Standard	Test Result
Thermal Shock	• Temperature: -40 ~ 85℃ • Ramp time: Less than 10 seconds. • Dwell Time: 10 minutes • Number of Cycles: 350 times	*JESD22-A106 *IEC 60068-2-14 for dwell time and number of cycles	Pass
Vibration Non-operating unpackaged device	• Vibration Wave Form: Sine Waveform • Vibration frequency / Displacement: 20-80 Hz/1.5mm • Vibration frequency / Acceleration: 80-2000 Hz/20g • Cycle Time: 4 min/cycle • Number of Cycles: 4 cycle/axis • Vibration Axes：X, Y and Z (Rotate each axis on vertical vibration table)	JEDEC 22-B103B (2016)	Pass
Mechanical Shock Non-operating Unpackaged device	• Pulse shape: Half-sine waveform • Impact acceleration: 1500 g • Pulse duration: 0.5 ms • Number of shocks: 30 shocks (5 shocks for each face) • Orientation: Bottom, top, left, right, front and rear faces	JEDEC 22-B110B.01 (2019)	Pass

15.1.1 Reliability MTBF Prediction

Table 35: MTBF Predictions for Sera NX040 Modules

Ezurio Part Number	Environment	Standard	Test Result 45 ℃ (Hours)
453-00174R 453-00174C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	2,648,932
453-00175R 453-00175C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	2,731,134
453-00174R 453-00174C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	993,350
453-00175R 453-00175C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	1,024,275
Ezurio Part Number	**Environment**	**Standard**	**Test Result 85 ℃ (Hours)**
453-00174R 453-00174C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	541,341
453-00175R 453-00175C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	560,844
453-00174R 453-00174C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	203,003
453-00175R 453-00175C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	210,317

16 Regulatory

Note: For complete regulatory information, refer to the NX040 Regulatory Information document which is also available from the NX040 product page.

The NX040 holds current certifications in the following countries:

Table 36: Regulatory Certifications

Country/Region	Regulatory ID
USA (FCC)	SQG-SERANX040
EU (ETSI)	N/A (No ID Number Required)
UKCA	N/A (No ID Number Required)
Canada (ISED)	3147A-SERANX040
Japan (MIC) - pending	*N/A*
Korea (KC) - pending	*N/A*
Australia (RCM) - pending	*N/A (No ID Number Required)*
New Zealand (RCM) - pending	*N/A (No ID Number Required)*

17 Bluetooth Qualification process

17.1 Overview

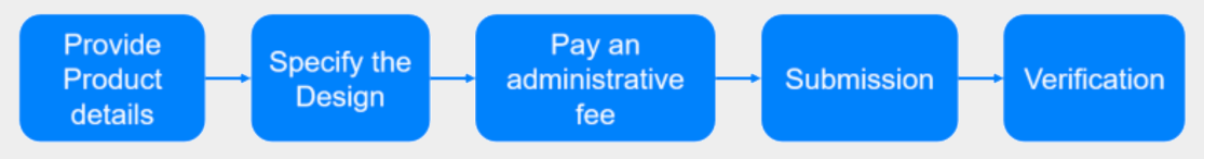
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

17.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference multiple existing designs, that have not been modified, (refer to Section 3.2.2.1 of the Qualification Program Reference Document v3).

For a Product that includes a new Design created by combining two or more unmodified designs that have DNs or QDIDs into one of the permitted combinations in Table 3.1 of the QPRDv3, a Member must also provide the following information:

- DNs or QDIDs for Designs included in the new Design
- The desired Core Configuration of the new Design (if applicable, see Table 3.1 below)
- The active TCRL Package version used for checking the applicable Core Configuration (including transport compatibility) and evaluating test requirements

Any included Design must not implement any Layers using withdrawn specification(s).

When creating a new Design using Option 2a, the Inter-Layer Dependency (ILD) between Layers included in the Design will be checked based on the latest TCRL Package version used among the included Designs.

For the purposes of this document, it is assumed that the member is combining unmodified Core-Controller Configuration and Core-Host Configuration designs, to complete a Core-Complete Configuration.

17.3 Qualification Steps When Referencing multiple existing designs, (unmodified) – Option 2a in the QPRDv3

For this qualification option, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number
    - Product Publication Date (the product publication date may not be later than 90 days after submission)

- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
- If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the multiple DNs or QDIDs used in your, (for Option 2a two or more DNs or QDIDs must be referenced)
   - Select 'I'm finished entering DN's
   - Once the DNs or QDIDs are selected they will appear on the left-hand side, indicating the layers covered by the design (should show Core-Controller and Core Host Layers covered).
   - What do you want to do next? Answer, 'Combine unmodified Designs'.
   - The Qualification Workspace Tool will indicate that a new Design will be created and what type of Core-Complete configuration is selected.
   - An active TCRL will be selected for the design.
   - Perform the Consistency Check, which should result in no inconsistencies
   - If there are any inconsistencies these will need to be resolved before proceeding
   - Save and go to Test Plan and Documentation
5. Test Plan and Documentation
   a. As no modifications have been made to the combined designs the tool should report the following message:
   'No test plan has been generated for your new Design. Test declarations and test reports do not need to be submitted. You can continue to the next step.'
   b. Save and go to Product Qualification fee
6. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
7. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
8. Download Product and Design Details (SDoC):
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

17.4 Example Design Combinations

The following gives an example of a design possible under option 2a:

Ezurio Controller Subsystem + nRF Connect SDK Host Subsystem (Ezurio Sera NX040 based design)

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
Sera NX040 (controller subsystem)	Ezurio	D064946	214713	https://qualification.bluetooth.com/ListingDetails/198129
nRF Connect SDK Host Subsystem	Nordic Semiconductor ASA	D064045	214837	https://qualification.bluetooth.com/ListingDetails/185028

17.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

18 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

Note: Information contained in this document is subject to change.

Ezurio's products are subject to standard Terms & Conditions.