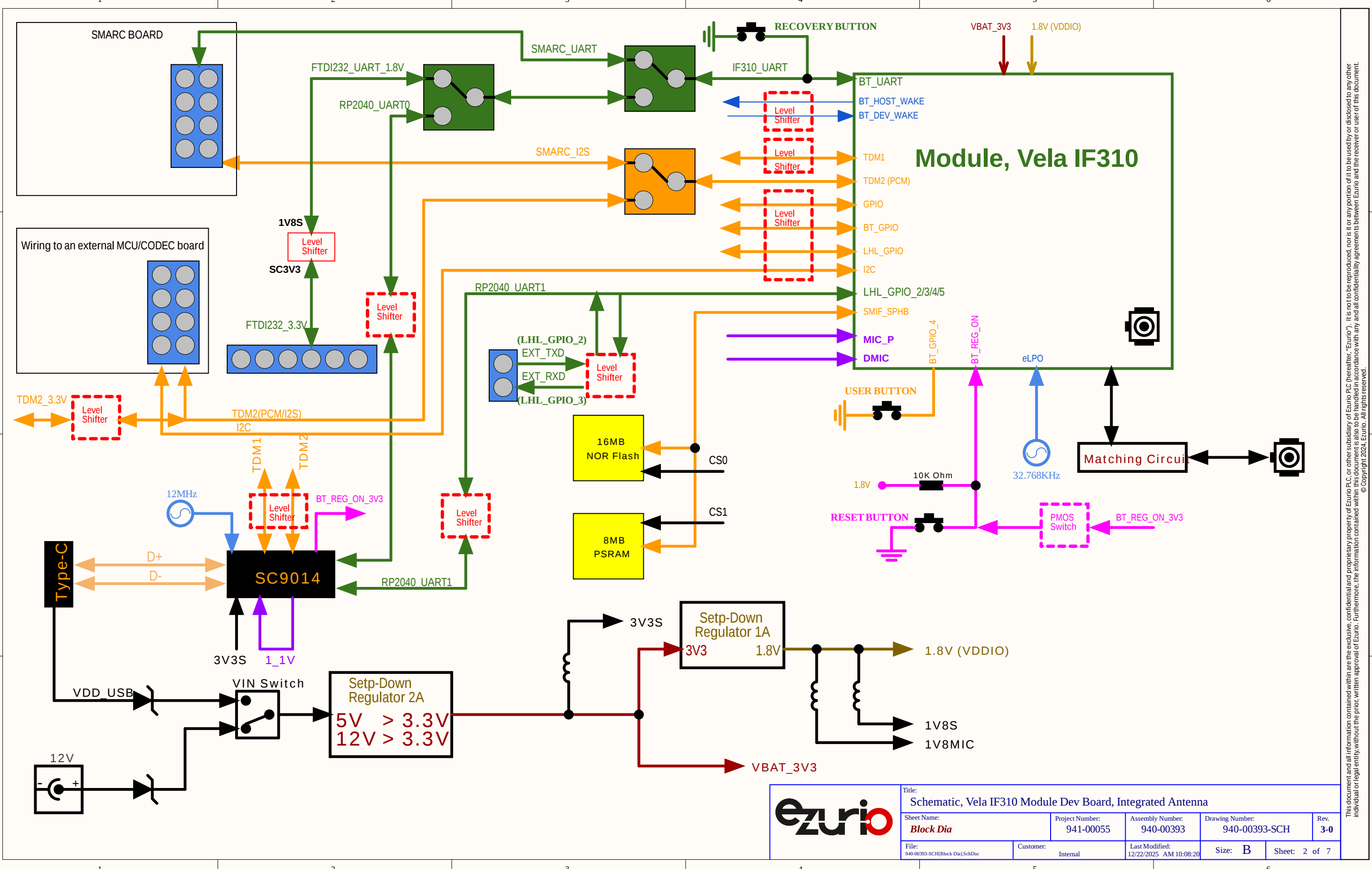


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A	DATE	Rev.	INITIATER	Note																																																																																		
	2025/07/04	R0.A	Jacky Kuo	Initial Release																																																																																		
	2025/07/11	R0.B	Jacky Kuo	1. Add level shifters to switch between 3.3V and 1.8V for TDM1 and TDM2 buses.(U17, 18, 19) 2. Add a level shifter to provide BT_REG_ON externally. (U11) 3. Connected the "SMARC_RESET_OUT_1P8V" to the "BT_REG_ON".																																																																																		
	2025/07/17	R0.C	Jacky Kuo	U10/GPIO16 - BT_DEV_WAKE U10/GPIO17 - BT_HOST_WAKE																																																																																		
	2025/07/28	R0.D	Jacky Kuo	U10/GPIO_18 - TDM2_DO / BT_PCM_OUT U10/GPIO_19 - TDM2_DI / BT_PCM_IN U10/GPIO_20 - TDM2_SCK / BT_PCM_CLK U10/GPIO_21 - TDM2_WS / BT_PCM_SYNC U10/GPIO_25 - TDM1_DO U10/GPIO_26 - TDM1_DI U10/GPIO_27 - TDM1_SCK U10/GPIO_28 - TDM1_WS																																																																																		
	2025/07/31	R0.E	Jacky Kuo	1. Change S10, S11, S12, S14, S15 to 1-bit dip switch. 2. Change S7 to 2-bit dip switch. 3. Change S9 and S13 to 4-bit dip switch. 4. Their corresponding control signal is connected to VCC through a resistor and also connected to the switch to pull it down to GND.																																																																																		
	2025/08/05	R0.F	Jacky Kuo	Change U1 to TPS62932DRLR																																																																																		
	2025/08/15	1-0	Jacky Kuo	1-0 release																																																																																		
	B	2025/10/09	2-0	Jacky Kuo	1. R18 change to 10 KOhm/1%. 2. R19 change to 0 Ohm. 3. Change U10's IOVDD power rail to 3.3V from 1.8V. 4. Added 5 level shifter circuits for U10's UART0/1 signals, TDM signals and WAKEUP signals. 5. Added Q2 circuit for Reset control. 6. C11 change to 0.6nH/0201. 7. Added FB4 for U2 input. 8. Change R28 and R31 value to 5.1 KOhm from 10 KOhm. 9. Added TP8 to TP17 for the unused GPIOs of U10. 10. Added a J32 pin header on the UART bus between U5 and MOD1. 11. Added a J31 pin header on the BT_WAKE signals between U10 and MOD1.																																																																																	
		2025/11/28	3-0	Jacky Kuo	1. Change Q2 to SMS3415 (P-MOS) to match RP2040’s GPIO13 initial state (High Level). 2. Change C11 to 0201/ 0 Ohm.																																																																																	
2025/12/9 2025/12/15			Jacky Kuo Jacky Kuo	3. Updated the definitions for MOD1's pins 8–11, 32, 33, 43, and 47. 4. Changed U18, U19, U23, and U25 to "TI, SN74AVC4T774RSV" level translator. 5. Changed U22 and U24 to "NXP, NTS0104GU12" level translator. (Same as the one used on U8). 6. Changed R131 and R132 to 100 KOhm.																																																																																		
C	PCB1  Ezurio, 750-00055																																																																																					
	<table><tr><td colspan="2">Approvals</td><td colspan="2">Date</td><td colspan="5" rowspan="4">  3F-1, No.145, Xianzheng 9th Rd, Zhubei City, Hsinchu County 30251, Taiwan (R.O.C.) Phone: +886-3-552-9695 www.ezurio.com </td></tr><tr><td>Drawn:</td><td>JK, AL</td><td colspan="2">Apr 22, 2025</td></tr><tr><td>Checked:</td><td>Jacky Kuo</td><td colspan="2">Aug 13, 2025</td></tr><tr><td>Approved:</td><td>AC</td><td colspan="2">Aug 19, 2025</td></tr><tr><td colspan="6">Title:</td><td colspan="5">Schematic, Vela IF310 Module Dev Board, Integrated Antenna</td></tr><tr><td colspan="2">Sheet Name:</td><td colspan="2">Project Number:</td><td colspan="2">Assembly Number:</td><td colspan="2">Drawing Number:</td><td colspan="3">Rev.</td></tr><tr><td colspan="2">History</td><td colspan="2">941-00055</td><td colspan="2">940-00393</td><td colspan="2">940-00393-SCH</td><td colspan="3">3-0</td></tr><tr><td colspan="3">File:</td><td colspan="2">Customer:</td><td colspan="2">Last Modified:</td><td colspan="2">Size:</td><td colspan="2">Sheet:</td></tr><tr><td colspan="3">940-00393-SCH[History].SchDoc</td><td colspan="2">Internal</td><td colspan="2">12/22/2025 AM 10:08:20</td><td colspan="2">B</td><td colspan="2">1 of 7</td></tr></table>											Approvals		Date		 3F-1, No.145, Xianzheng 9th Rd, Zhubei City, Hsinchu County 30251, Taiwan (R.O.C.) Phone: +886-3-552-9695 www.ezurio.com					Drawn:	JK, AL	Apr 22, 2025		Checked:	Jacky Kuo	Aug 13, 2025		Approved:	AC	Aug 19, 2025		Title:						Schematic, Vela IF310 Module Dev Board, Integrated Antenna					Sheet Name:		Project Number:		Assembly Number:		Drawing Number:		Rev.			History		941-00055		940-00393		940-00393-SCH		3-0			File:			Customer:		Last Modified:		Size:		Sheet:		940-00393-SCH[History].SchDoc			Internal		12/22/2025 AM 10:08:20		B		1 of 7
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Title: Schematic, Vela IF310 Module Dev Board, Integrated Antenna				
Sheet Name: Block Dia	Project Number: 941-00055	Assembly Number: 940-00393	Drawing Number: 940-00393-SCH	Rev. 3-0
File: 940-00393-SCH[Block Dia]SchDoc	Customer: Internal	Last Modified: 12/22/2025 AM 10:08:20	Size: B	Sheet: 2 of 7

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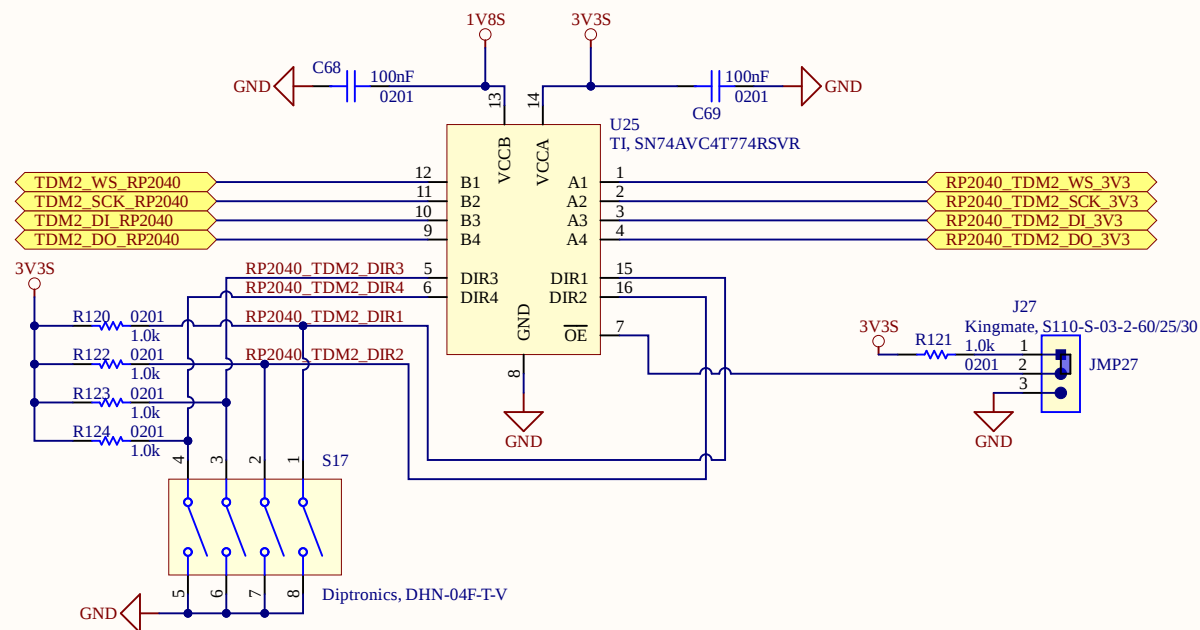
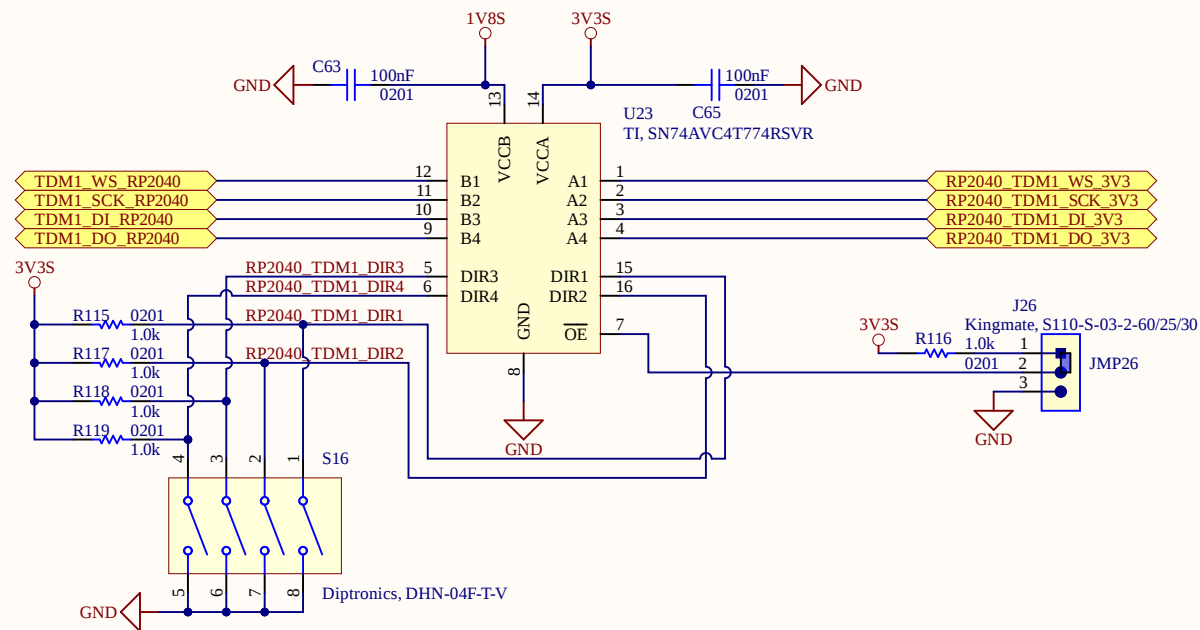
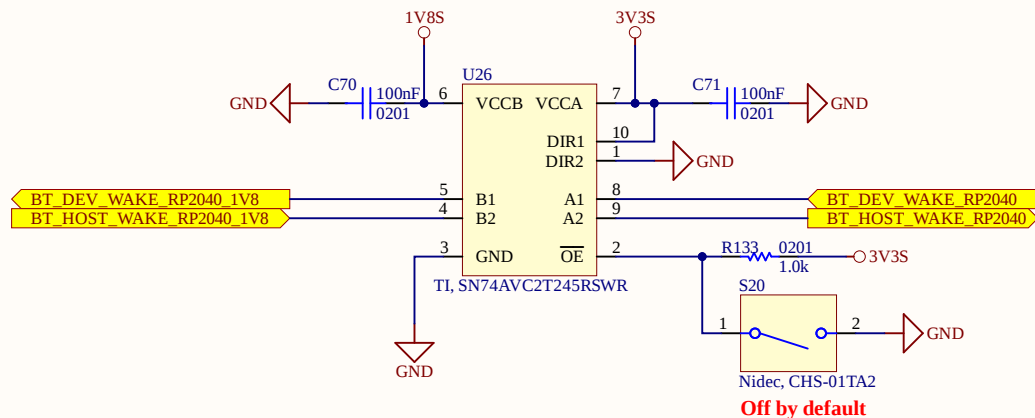
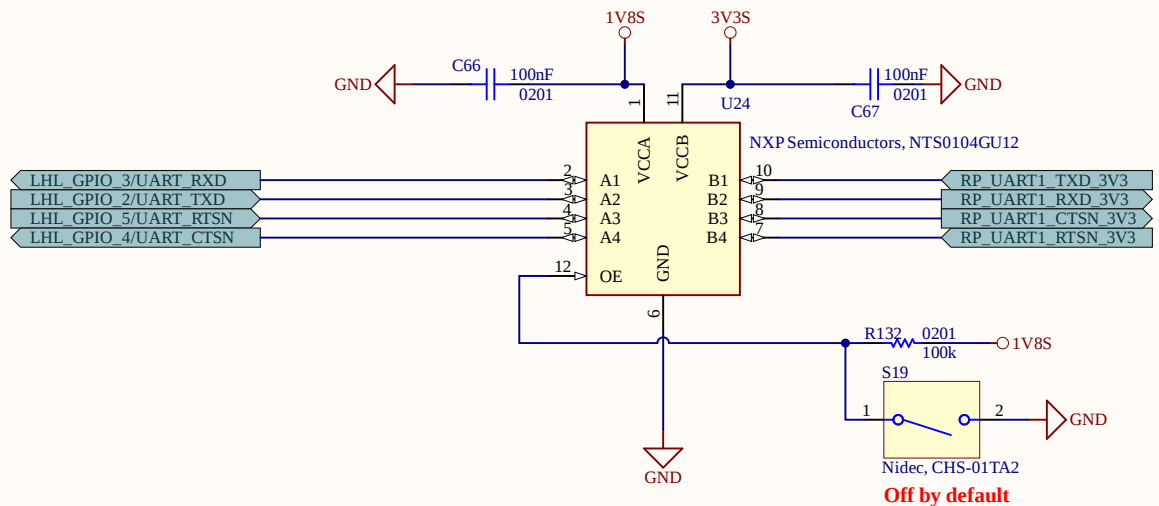
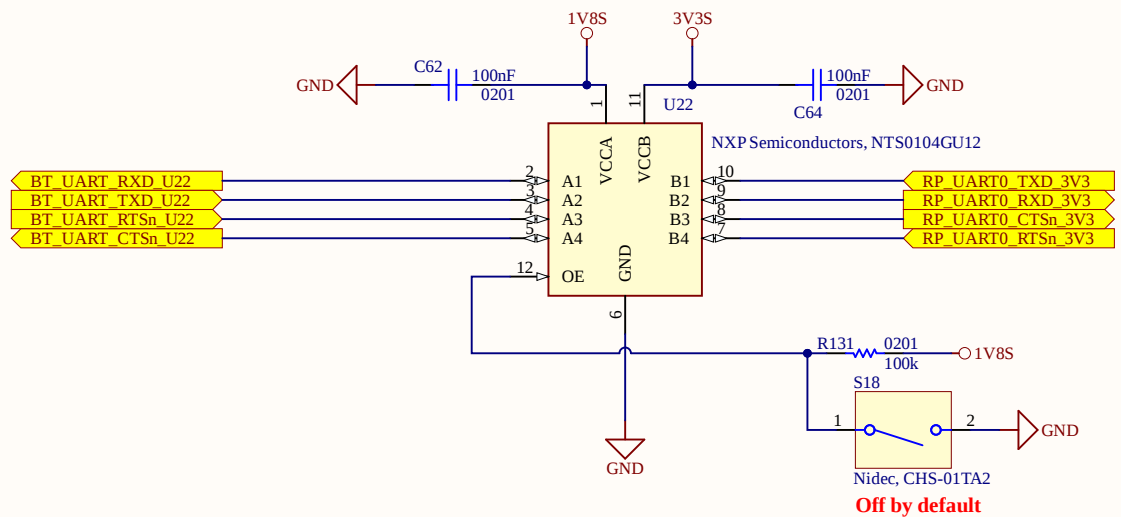
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Title: Schematic, Vela IF310 Module Dev Board, Integrated Antenna

Sheet Name: Level Shifter	Project Number: 941-00055	Assembly Number: 940-00393	Drawing Number: 940-00393-SCH	Rev. 3-0
File: 940-00393-SCH[Level Shifter].SchDoc	Customer: Internal	Last Modified: 12/22/2025 AM 10:08:21	Size: B	Sheet: 7 of 7

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