Datasheet

60-SIPT Series

Version 4.5

Revision History

Version	Date	Notes	Contributors	Approver
1.0	29 Aug 2017	Initial version		Jay White
1.1	08 Sept 2017	Updated Max. Current Consumption table/column headings		Andrew Chen
1.2	19 Sept 2017	Changed Pin 26 from GND to N/C		Andrew Chen
1.3	10 Oct 2017	Added mFlexPIFA antenna information		Bill Steinike
1.4	06 Nov 2017	Updated supporting operating systems; corrected header		Jay White
1.5	05 Dec 2017	Added Korea regulatory ID information		Connie Lin
1.6	26 Mar 2018	Updated antenna port definition and block diagram	Kai Wei	Jay White
1.7	30 Mar 2018	Update Wi-Fi and BT MAC rule	Andrew Chen	Jay White
1.8	02 Apr 2018	Removed SSD and MSD references		Jay White
1.9	23 Aug 2018	Move the MSL from MSL-3 to MSL-4	Andrew Chen	Jay White
1.10	08 Oct 2018	Added following note to WLAN Transmitter Characteristics section: *IEEE PS current measurement with the 60-SIPT DVK was 12 mA for both 2.4 GHz and 5 GHz at all DTIM settings.* Corrected Sensitivity note in Table 3: *CH13/**CH155** (WLAN); CH78 (BT) will decade up to 4-6dB.*	Sean Querry	Andrew Chen
1.11	07 Nov 2018	Removed 802.11s reference		Jay White
1.12	14 Nov 2018	Fixed channels for KC		Andrew Chen
1.13	11 Feb 2019	Corrected the FCC, KC, and IC regulatory IDs	Connie Linn	Jay White
1.14	13 Feb 2019	Updated logos and URLs		Sue White
1.15	17 Apr 2019	Removed DFS Radar Detection info		Jay White
1.16	28 Aug 2019	Updated to BT5.1		Jay White
1.17	26 Sept 2019	Removed AoA/DoA references		Jay White
1.18	11 Oct 2019	Removed Linux and Android version numbers	Joe Conley	Jay White
1.19	14 Oct 2019	Removed advertising extension references… *LE Advertising Length Extension* Updated warranty information (one year vs. three)	Jonathan Kaye	Jay White
1.20	17 Jan 2020	Added *Top View* to Figure 11 to clarify mechanical drawing orientation	Bob Monroe	Jay White
1.21	06 May 2020	Updated block diagram and pin description for Pin4 and Pin 12	Kai.Wei	Jay White
1.22	02 Sept 2020	Updated Regulatory section including new ETSI standards	Ryan Urness	Jay White
1.23	18 Nov 2020	Updated all regulatory information	Ryan Urness	Jay White
2.0	16 Dec 2020	Updated certified antennas and regulatory info	Bob Monroe	Jonathan Kaye
2.1	22 Jan 2021	Transferred all regulatory information to a separate document	Maggie Teng	Jonathan Kaye
2.2	28 Jan 2021	Removed beamforming references	Dan Kephart	Andrew Dobbing
2.3	12 Apr 2021	Updated Bluetooth SIG Declaration ID	Bob Monroe	Jonathan Kaye
2.4	05 May 2021	Updated 5 GHz operating channel numbers for EU, FCC, and MIC	Miles Chung	Andrew Chen
2.5	22 July 2021	Updated Bluetooth version number to 5.1	Miles Chung	Dan Kephart
2.6	23 Aug 2021	Added EN 300 440 support	Maggie Teng	Dave Drogowski
2.7	24 Aug 2021	Updated supported security types	Dan Kephart	Dave Drogowski

Version	Date	Notes	Contributors	Approver
2.8	16 Nov 2021	Removed CCX / WFA Certifications info	Dan Kephart	Dave Drogowski
2.9	23 Dec 2021	Updated Mechanical Specifications	Dave Drogowski	Andrew Chen
3.0	2 May 2022	Updated to latest Wi-Fi/BT specifications	Dave Drogowski	Dan Kephart
3.1	12 May 2022	EU supported 5GHz U-NII-3 band EU and JP do not support CH144	Kai Wei	Andrew Chen
3.2	6 Sept 2022	Updated module weight in		
3.3	17 Feb 2023	Added updated Terms and Conditions	Dave Drogowski	Elaine Baxter
3.4	26 Feb 2024	Updated module height in Mechanical Specifications	Connie Lin	Andrew Chen
4.0	8 May 2024	Ezurio rebranding	Sue White	Dave Drogowski
4.1	29 Oct 2024	Added -Q variants	Dave Drogowski	Dan Kephart
4.2	1 Nov 2024	Updated Bluetooth SIG Qualification	Dave Drogowski	Jonathan Kaye
4.3	13 May 2024	Added Development Kit Part Number	Dan Kephart	Dave Drogowski
4.4	18 Sept 2025	Replaced 802.11 channel information with reference to regulatory release notes	John Nosky	Dave Drogowski
4.5	31 Mar 2026	Added orderable part number 453-00202	Bob Monroe	Dave Drogowski

Contents

1 Scope

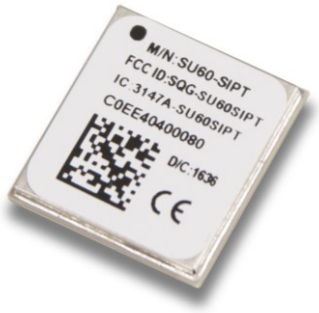
This document describes key hardware aspects of the Ezurio 60-SIPT series system-in-package (SiP) modules providing either SDIO, USB2.0, or PCIe bus interface for WLAN connection and UART/PCM, SDIO/PCM, USB2.0/PCM for Bluetooth® connection. This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from several sources and includes information found in the Marvell 88W8997/88PG823 data sheets issued in April 2016, along with other documents provided from Marvell.

Note that the information in this document is subject to change. Please contact Ezurio to obtain the most recent version of this document.

2 Introduction

2.1 General Description

The 60-SIPT series SiP modules are an integrated, small form factor 2x2 MIMO 802.11 a/b/g/n/ac WLAN plus *Bluetooth* 5.1 dual mode device that is optimized for low-power mobile devices. The integration of all WLAN and *Bluetooth* functionality in a single package supports low cost and simple implementation along with flexibility for platform-specific customization.



This device is pre-calibrated and integrates the complete transmit/receive RF paths including band pass filter, diplexer, switches, reference crystal oscillator, and power manage units (PMU).

The 60-SIPT series device supports IEEE 802.11 ac 2X2 receive MIMO spatial stream multiplexing with data rates up to MCS9 (866.7 Mbps). Bluetooth 5.1. Internal Wi-Fi and BT coexistence scheme provides optimized throughput when Wi-Fi and BT working simultaneously. The device's low power consumption radio architecture and power manage unit (PMU) proprietary power save technologies allow for extended battery life.

In addition, its dual 802.11 and Bluetooth radio includes full digital MAC and baseband engines that handle all 802.11 CCK/OFDM® 2.4/5GHz, and Bluetooth basic rate and EDR baseband and protocol processing.

Dual embedded low-power CPU cores minimize host loading and maximize flexibility to support customer-specific use cases.

The 60-SIPT series SiP modules include two product SKUs which is have different supported software features. Please check Ezurio Sales/FAE for further information. Order information is listed in Table 1.

Table 1: Product ordering information

Order Model	Description
SU60-SIPT	802.11ac + Bluetooth 5.1 60 Series hardware combined with Summit Series Enterprise software
ST60-SIPT	802.11ac + Bluetooth 5.1 60 Series hardware combined with Sterling Series Professional software
453-00202	802.11ac + Bluetooth 5.1 60 Series hardware combined with Sterling Series Professional software
ST60-SIPT-Q	802.11ac + Bluetooth 5.1 60 Series hardware combined with Sterling Series Professional software, Q variant
DVK-ST60-SIPT	Development Board, ST60-SIPT

3 60-SIPT Series Features Summary

The Ezurio 60-SIPT series device features are described in Table 2.

Table 2: 60-SIPT series features

<table>
<tr><th>Feature</th><th>Description</th></tr>
<tr><td></td><td>Integrates the complete transmit/receive RF paths including band pass filter, diplexer, switches, reference crystal oscillator, and power manage unit (PMU).
Supports 20/40/80MHz channel bandwidth.
WLAN/Bluetooth share one antenna.</td></tr>
<tr><td colspan="2">The Bluetooth® word mark and logos are registered trademarks owned by Bluetooth SIG, Inc. Any use of such marks by Ezurio is under license. Other trademarks and trade names are those of their respective owners.</td></tr>
<tr><td></td><td>Dynamic Voltage Scaling (DVS) and Adaptive Voltage Scaling (AVS) features support the latest Marvell SoC and Processor power control scheme.</td></tr>
<tr><td></td><td>RF system tested and calibrated in production</td></tr>
<tr><td></td><td>An external sleep clock of 32.768 KHz is required during power save mode</td></tr>
<tr><td></td><td>• SDIO 3.0 (4-bit and 1-bit), SDR 12/25/50 mode (up to 100 MHz), USB2.0 or PCIe for WLAN
• SDIO 3.0, USB 2.0, HS-UART for Bluetooth HCI (compatible with any upper layer Bluetooth stack)
<table>
<tr><th>Strap Value
CONFIG_HOST [2-0]</th><th>WLAN</th><th>Bluetooth/BLE</th><th>ROM Notes</th></tr>
<tr><td>000</td><td>SDIO</td><td>UART</td><td>-</td></tr>
<tr><td>001</td><td>SDIO</td><td>SDIO</td><td>-</td></tr>
<tr><td>010</td><td>PCIe</td><td>USB 2.0</td><td>Initial USB 2.0 PHY and COM PHY PCIe portion</td></tr>
<tr><td>011</td><td>PCIe</td><td>UART</td><td>Initial only COM PHY PCIe portion</td></tr>
<tr><td>100</td><td>USB 2.0</td><td>UART</td><td>Initial COM PHY USB 2.0</td></tr>
<tr><td>101</td><td>USB 2.0</td><td>USB 2.0</td><td>Initial only USB 2.0 PHY</td></tr>
</table></td></tr>
<tr><td></td><td>• Incorporates a 40 MHz reference frequency source in package
• An external sleep clock is recommended for minimal current consumption. If no sleep clock input is provided, an internal sleep clock (derived from reference clock) is used. An approximate 50 uA current increase on the 3.3V rail.</td></tr>
<tr><td></td><td>• A-MPDU RX (de-aggregation) and TX (aggregation) supports 802.11ac single-MPDU A-MPDU.
• Multi-BSS/Station
• Transmit rate adaption, transmit power control
• Modulation and coding scheme (MCS): 802.11ac—MCS0-9 Nsts=1 and 2.
802.11n—MCS0-15
• 20/40/80 MHz channel bandwidths support
• On-chip gain selectable LNA with optimized noise figure and power consumption
• Internal PA with optimized gain distribution for linearity and noise performance
• Support wide variety of WLAN encryption: TKIP/WEP/AES</td></tr>
</table>

- Bluetooth 5.1, Bluetooth class 1
- Support data rate: 1 Mbps (GFSK), 2 Mbps (π/4-DQPSK), 3 Mbps (8-DPSK)
- Digital audio interface with TDM interface for voice application
- Adaptive Frequency Hopping (AFH) using Package Error Rate (PER)
- Standard SDIO or UART HCI transport layer
- WLAN/Bluetooth coexistence protocol support
- Shared LNA with WLAN/Bluetooth
- Encryption (AES) support

4 Specifications

Table 3: Specifications

Feature	Description
Physical Interface	84-pin LGA package (including 16 thermal ground pads under the package)
Wi-Fi Interface	1-bit or 4-bit Secure Digital I/O; PCIe v3.0 Gen1/Gen2 (2.5/5 Gbps); USB 2.0
Bluetooth/BLE Interface	Host Controller Interface (HCI) using high speed UART, SDIO, USB 2.0
Main Chip	Marvell 88W8997 (WLAN/BT); Marvell 88PG823 (PMU)
Input Voltage Requirements	DC 3.3 V ±10%
I/O Signalling Voltage	DC 3.3 V ± 10% or DC 1.8 V ± 10%
Operating Temperature	-30° to 85°C (-22° to 185°F)
Operating Humidity	10 to 90% (non-condensing)
Storage Temperature	-40° to 85°C (-40° to 185°F)
Storage Humidity	10 to 90% (non-condensing)
Maximum Electrostatic Discharge	Conductive 4KV; Air coupled 8KV follow EN61000-4-2
Size	13 mm (length) x 14 mm (width) x 1.87 mm (thickness)
Weight	0.8053 g
Wi-Fi Media	Direct Sequence-Spread Spectrum (DSSS) Complementary Code Keying (CCK) Orthogonal Frequency Divisional Multiplexing (OFDM)
Bluetooth Media	Frequency Hopping Spread Spectrum (FHSS)
Wi-Fi Media Access Protocol	Carrier sense multiple access with collision avoidance (CSMA/CA) A-MPDU Rx (De-aggregation) and Tx (aggregation) (802.11ac single-MPDU A-MPDU)
Network Architecture Types	Infrastructure and ad-hoc
Wi-Fi Standards	IEEE 802.11a, 802.11b, 802.11d*, 802.11e, 802.11g, 802.11h, 802.11i, 802.11k*, 802.11n, 802.11r, 802.11v*, 802.11ac * Summit version only
Bluetooth Standards	Bluetooth 5.1

Strap Value

CONFIG_HOST [2-0]	WLAN	Bluetooth/ BLE	ROM Notes
000	SDIO	UART	-
001	SDIO	SDIO	-
010	PCIe	USB 2.0	Initial USB 2.0 PHY and COM PHY PCIe portion
011	PCIe	UART	Initial only COM PHY PCIe portion
100	USB 2.0	UART	Initial COM PHY USB 2.0
101	USB 2.0	USB 2.0	Initial only USB 2.0 PHY

Feature	Description
Wi-Fi Data Rates Supported	Support 802.11 ac/a/b/g/n 2X2 MIMO. 802.11b (DSSS, CCK) 1, 2, 5.5, 11 Mbps 802.11a/g (OFDM) 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n (OFDM, HT20/HT40, MCS 0-15) 802.11ac (OFDM, HT20, MCS0-8; OFDM HT40/HT80, MCS 0-9)
Modulation Table	BPSK, QPSK, CCK, 16-QAM, 64-QAM, and 256-QAM.

802.11ac / 802.11n	HT MCS Index	VHT MCS Index	Spatial Streams	Modulation	Coding	20 MHz	
						No SGI	SGI
	0	0	1	BPSK	1/2	6.5	7.2
	1	1	1	QPSK	1/2	13	14.4
	2	2	1	QPSK	3/4	19.5	21.7
	3	3	1	16-QAM	1/2	26	28.9
	4	4	1	16-QAM	3/4	39	43.3
	5	5	1	64-QAM	2/3	52	57.8
	6	6	1	64-QAM	3/4	58.5	65
	7	7	1	64-QAM	5/6	65	72.2
		8	1	256-QAM	3/4	78	86.7
		9	1	256-QAM	5/6	N/A	N/A
	8	0	2	BPSK	1/2	13	14.4
	9	1	2	QPSK	1/2	26	28.9
	10	2	2	QPSK	3/4	39	43.3
	11	3	2	16-QAM	1/2	52	57.8
	12	4	2	16-QAM	3/4	78	86.7
	13	5	2	64-QAM	2/3	104	115.6
	14	6	2	64-QAM	3/4	117	130.3
	15	7	2	64-QAM	5/6	130	144.4
		8	2	256-QAM	3/4	156	173.3
		9	2	256-QAM	5/6	N/A	N/A

Feature	Description	
802.11ac/n Spatial Streams	2 (2x2 MIMO)	
Bluetooth Data Rates Supported	1, 2, 3 Mbps	
Bluetooth Modulation	GFSK@ 1 Mbps Pi/4-DQPSK@ 2 Mbps 8-DPSK@ 3 Mbps	
Wi-Fi Channels and Regulatory Domains	Supported Wi-Fi channels and regulatory domains change over time, see the Regulatory Release Notes (RRN) posted with each software release for the latest information.	
Transmit Power ***Note:*** *Transmit power on each channel varies per individual country regulations. All values are nominal with +/-2 dBm tolerance at room temperature.* *Tolerance could be up to +/-2.5 dBm across operating temperature.* ***Note:*** *HT20 – 20 MHz-wide channels* *HT40 – 40 MHz-wide channels* *HT80 – 80 MHz-wide channels*	802.11a	
	6 Mbps	18 dBm (63 mW)
	54 Mbps	16 dBm (40 mW)
	802.11b	
	1 Mbps	18 dBm (63 mW)
	11 Mbps	18 dBm (63 mW)
	802.11g	
	6 Mbps	18 dBm (63 mW)
	54 Mbps	16 dBm (40 mW)
	802.11n (2.4/5 GHz)	
	6.5 Mbps (MCS0-5/MCS8-13; HT20)	18 dBm (63 mW)
	65 Mbps (MCS6-7/MCS14-15; HT20)	16 dBm (40 mW)
	13.5 Mbps (MCS0-5/MCS8-13; HT40)	16 dBm (40 mW)
	135 Mbps (MCS6-7/MCS14-15; HT40)	14 dBm (25 mW)
	802.11ac (5 GHz)	
	6.5/13 Mbps (MCS0-6; Ntst=1,2; HT20)	18 dBm (63 mW)
	78/156 Mbps (MCS7-8; Ntst=1,2; HT20)	16 dBm (40 mW)
	13.5/27 Mbps (MCS0-5; Ntst=1,2; HT40)	16 dBm (40 mW)
	180/360 Mbps (MCS6-8; Ntst=1,2; HT40)	14 dBm (25 mW)
	200/400 Mbps (MCS9; Ntst=1,2; HT40)	12 dBm (15.8mW)
	29.3/58.5 Mbps (MCS0-5; Ntst=1,2; HT80)	14 dBm (25 mW)
	263.3/526.5 Mbps (MCS6-8; Ntst=1,2; HT80)	12 dBm (15.8 mW)
	390/780 Mbps (MCS9; Ntst=1,2; HT80)	10 dBm (10 mW)
	Bluetooth	
	1 Mbps (1DH5)	10 dBm (12.5 mW)
	2 Mbps	7 dBm (6.3 mW)
	3 Mbps	7 dBm (6.3 mW)
	BLE (1 Mbps)	7 dBm (6.3 mW)

Feature	Description	
Typical Receiver Sensitivity (PER < = 10%) ***Note:*** *All values nominal, +/-3 dBm.* *Sensitivity on CH13/CH155 (WLAN)/CH78 (BT) will decade up to 4-6 dB.*	802.11a:	
	6 Mbps	-89 dBm
	54 Mbps	-74 dBm
	802.11b:	
	1 Mbps	-95 dBm
	11 Mbps	-90 dBm (PER < 8%)
	802.11g:	
	6 Mbps	-91 dBm
	54 Mbps	-75 dBm
	802.11n (2.4 GHz)	
	6.5 Mbps (MCS0; HT20)	-91 dBm
	65 Mbps (MCS7; HT20)	-73 dBm
	13.5 Mbps (MCS0; HT40)	-85 dBm
	135 Mbps (MCS7; HT40)	-70 dBm
	802.11n (5 GHz)	
	6.5 Mbps (MCS0; HT20)	-89 dBm
	65 Mbps (MCS7; HT20)	-70 dBm
	13.5Mbps (MCS0; HT40)	-86 dBm
	135Mbps (MCS7; HT40)	-69 dBm
	802.11ac (5 GHz)	
	6.5 Mbps (MCS0; HT20)	-89 dBm
	78 Mbps (MCS8; HT20)	-67 dBm
	13.5 Mbps (MCS0; HT40)	-86 dBm
	180 Mbps (MCS9; HT40)	-63 dBm
	29.3 Mbps (MCS0; HT80)	-81 dBm
	390/780 Mbps (MCS9; HT80)	-55 dBm
	Bluetooth:	
	1 Mbps (1DH5)	-95 dBm
	2Mbps (2DH5)	-94 dBm
	3 Mbps (3DH5)	-88 dBm
	BLE	-95 dBm
Operating Systems Supported	Linux Android	
Security	Standards	
	Wireless Equivalent Privacy (WEP)	

Feature	Description
	Wi-Fi Protected Access (WPA) WPA2-Personal WPA2-Enterprise WPA3-Personal WPA3-Enterprise Encryption Wireless Equivalent Privacy (WEP, RC4 Algorithm) Temporal Key Integrity Protocol (TKIP, RC4 Algorithm) Advanced Encryption Standard (AES, Rijndael Algorithm) Encryption Key Provisioning Static (40-bit and 128-bit lengths) Pre-Shared (PSK) Dynamic 802.1X Extensible Authentication Protocol Types EAP-FAST, PEAP-MSCHAPv2 EAP-TLS, PEAP-TLS EAP-TTLS, LEAP PEAP-GTC
Compliance	**EU** EN 300 328, 62311:2008 EN 300 440, EN 50665:2017 EN 301 489-1, EN 50385:2017 EN 301 489-17, EU 2015/863 (RoHS 3) EN 301 893 **FCC**, **ISED Canada** 47 CFR FCC Part 15.247, ICES-003 47 CFR FCC Part 15.407, ANSI C63.4:2014 47 CFR FCC Part 2.1091, RSS-247 FCC Part 15 Subpart B Class B **AS/NZS**, **MIC** AS/NZS 2772.2:2011, ARIB STD-T66/RCR STD-33 (2 AS/NZS 4268:2017, ARIB STD-T71 (5 GHz) **KC (Korea)**
Certifications	*Bluetooth*® SIG Qualification

Feature	Description
Warranty	One Year Warranty

All specifications are subject to change without notice

5 WLAN Functional Description

5.1 Overview

The 60-SIPT series SiP module is designed based on the Marvell 88W8997 802.11ac/a/b/g/n chipset. It is optimized for high speed, reliable, and low-power embedded applications. It's integrated with dual-band WLAN (2.4/5GHz) and Bluetooth 5.1. Its functionality includes:

- Improved throughput on the link due to frame aggregation, RIFS (reduced inter-frame spacing), and half guard intervals.
- Support for STBC (Space Time Block Codes) and LDPC (Low Density Parity Check) codes.
- Improved 11n performance due to features such as 11n frame aggregation (A-MPDU and A-MSDU) and low-overhead host-assisted buffering (RX A-MSDU and RX A-MPDU). These techniques can improve performance and efficiency of applications involving large bulk data transfers such as file transfers or high-resolution video streaming.
- IEEE 802.11 ac, 2X2 receive MIMIO spatial stream multiplexing with data rate up to MCS9 (866.7Mbps).

Additional functionality is listed in the following table (Table 4).

Table 4: WLAN functions

Feature	Description
WLAN MAC	• Frame Exchange at the MAC level to deliver data • Received frame filtering and validation (Cyclic Redundancy Check (CRC)) • Generation of MAC header and trailer information (MAC protocol Data Units (MPDUs)) • Fragmentation of data frames (MAC Service Data Units (MSDUs) • Access Mechanism support for fair access to shared wireless medium through (DCF and EDCA) • A-MPDU Aggregation/Deaggregation (support 802.11ac single –MPDU A-MPDU) • 20/40/80 MHz channel Coexistence • RIFS Burst Receive • Management Information Base • Radio Resource Measurement • Quality of Service • Block Acknowledgement • 802.11ac Downlink MIMO (receive) • Dynamic Frequency Selection • TIM Frame TX and RX • Multi-BSS/Station • Transmit Rate Adaptation. • Transmit Power Control
WLAN Base Band	• 802.11ac 2x2 MIMO (with on-chip Marvell RF radio) • Backward compatibility with legacy 802.11 n/a/b/g technology • WLAN/Bluetooth LNA sharing • PHY rate up to 866.7 Mbps • 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz packets in 40 MHz channel, 20 MHz duplicate legacy packets in 40 MHz channel operation. • 80 MHz bandwidth/channel, 4 positions of 20 MHz packets in 80 MHz channel, upper/lower 40 MHz packets in 80 MHz channel, 20 MHz quadruplicate legacy packets in 80 MHz channel mode operation. • Modulation and Coding Scheme (MCS): 802.11ac (MCS0-9. Nsts=1/2); 802.11n (MCS0-15) • 802.11 K Radio Resource Measurement. • 802.11ac /802.11n optional MIMO features:

	20/40/80 MHz Coexistence with middle-packaged detection (GI detection) for enhanced CCA – One spatial stream STBC reception and transmission – LDPC transmission and reception for 802.11ac and 802.11n – 256 QAM (MCS8-9) modulations supported – Short guard interval – RIFS on receive path for 802.11n packets – 802.11n Greenfield TX/RX • Power Save feature
WLAN Security	• WLAN Encryption features supported include: – Temporal Key Integrity Protocol (TKIP)/Wired Equivalent Privacy (WEP) – Advanced Encryption Standard (AES)/Counter-Mode/CBC-MAC Protocol (CCMP) – Advanced Encryption Standard (AES)/Cipher-Based Message Authentication Code (CMAC) – Advanced Encryption Standard (AES)/Galois/Counter Mode Protocol (GCMP) – WLAN Authentication and Private Infrastructure (WPAI)

6 Bluetooth Functional Description

The 60-SIPT series includes a fully-integrated Bluetooth baseband/radio. Several features and functions are listed in Table 5.

Table 5: Bluetooth functions

Feature	Description
Bluetooth Interface	• Voice interface: – Hardware support for continual PCM data transmission/reception without processor overhead. – Standard PCM clock rates from 64 kHz to 2.048 MHz with multi-slot handshake and synchronization. – A-law, U-law, and linear voice PCM encoding/decoding. • SDIO interface • High-Speed UART interface • USB 2.0
Bluetooth Core functionality	• Bluetooth 5.1 • Bluetooth Class 1 • WLAN and Bluetooth share same LNA and antenna • Digital audio interfaces with TDM interface for voice application • Baseband and radio BDR and EDR package type: 1 Mbps, 2 Mbps, 3 Mbps • Fully functional Bluetooth baseband: AFH, forward error correction, header error control, access code correction, CRC, encryption bit stream generation, and whitening. • Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER) • Interlaced scan for faster connection setup • Simultaneous active ACL connection setup • Automatic ACL package type selection • Full master and slave piconet support • Scatter net support • SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement • All standard SCO/eSCO voice coding • All standard pairing, authentication, link key, and encryption operations • Encryption (AES) support
Bluetooth Low Energy (BLE) Core functionality	• Advertiser, Scanner, Initiator, Master, and Slave roles support (connects to 16 links) • WLAN/Bluetooth Coexistence (BCA) protocol support. • Shared RF with BDR/EDR • Encryption (AES) support. • Intelligent Adaptive Frequency Hopping (AFH) • LE privacy 1.2 • LE Secure Connection. • LE Data Length Extension • 2 Mbps LE

7 Block Diagram

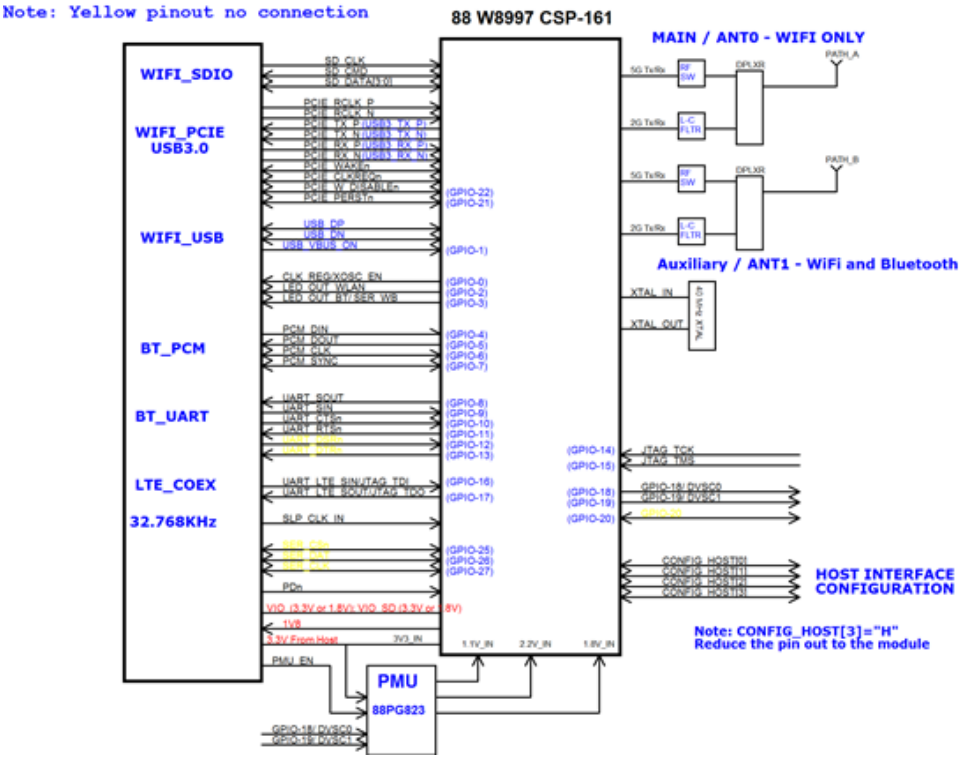


Figure 1: Block diagram

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 6 summarizes the absolute maximum ratings and Table 7 lists the recommended operating conditions for the 60-SIPT Series. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 6: Absolute maximum ratings

Symbol (Domain)	Parameter	Max Rating	Unit
VIO_SD	WLAN host SDIO interface I/O supply (for 1.8V system)	2.2	V
	(for 3.3V system)	4.0	
VIO	I/O configuration power supply (for 1.8V system)	2.2	V
	(for 3.3V system)	4.0	
3V3	External 3.3V power supply	4.0	V
Storage	Storage Temperature	-40 to +85	°C
ANT0; ANT1	Maximum RF input (reference to 50-Ω input)	+10	dBm
ESD	Electrostatic discharge tolerance	2000	V

8.2 Recommended Operating Conditions

Table 7: Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VIO_SD	WLAN host interface I/O supply	1.62/2.97	1.8/3.3	1.98/3.63	V
VIO	WLAN and BT GPIO I/O power supply	1.62/2.97	1.8/3.3	1.98/3.63	V
3V3	External 3.3V power supply	2.97	3.30	3.63	V
T-ambient	Ambient temperature	-30	25	85	°C

8.3 DC Electrical Characteristics

Table 8 and Table 9 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 8: General DC electrical characteristics (For 1.8V operation VIO_SD; VIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High Level Input Voltage	--	1.26		2.2	V
VIL	Low Level Input Voltage	--	-0.4		0.54	V
VHYS	Input Hysteresis	--	100			mV
VOH	Output high Voltage	--	1.4			V
VOL	Output low Voltage	--			0.4	V

Table 9: General DC electrical characteristics (For 3.3V operation VIO_SD; VIO)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High Level Input Voltage	--	2.4		3.6	V
VIL	Low Level Input Voltage	--	-0.4		0.9	V
VHYS	Input Hysteresis	--	100			mV
VOH	Output high Voltage	--	2.9			V
VOL	Output low Voltage	--			0.4	V

Table 10: DC electrical characteristics for 1.8V or 3.3V operation on special pads (PCIE_WAKEn, PCIE_CLKREQn)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH	High Level Input Voltage	--	1.4		3.6	V
VIL	Low Level Input Voltage	--	-0.4		0.8	V
VHYS	Input Hysteresis	--	150			mV
VOL	Output low Voltage	--			0.4	V

8.4 WLAN Radio Receiver Characteristics

Table 11 and Table 12 summarize the WLAN 60-SIPT series receiver characteristics.

Table 11: WLAN receiver characteristics for 2.4 GHz signal chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Frx	Receive input frequency range		2.412		2.484	GHz
Srf	Sensitivity					
	CCK, 1 Mbps	See Note[1]		-95		dBm
	CCK, 11 Mbps			-90		
	OFDM, 6 Mbps			-91		
	OFDM, 54 Mbps			-75		
	HT20, MCS0			-91		
	HT20, MCS7			-73		
Radj	Adjacent channel rejection					
	OFDM, 6 Mbps	See Note[1]		TBD		dB
	OFDM, 54 Mbps			TBD		
	HT20, MCS0			TBD		
	HT20, MCS7			TBD		

Table 12: WLAN Receiver Characteristics for 5 GHz Dual Chain Operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Frx	Receive input frequency range		5.15		5.825	GHz
Srf	Sensitivity					
	OFDM, 6 Mbps	See Note[1]		-89		dBm
	OFDM, 54 Mbps			-74		
	HT20, MCS0			-89		
	HT20, MCS7			-70		
	HT40, MCS0			-86		
	HT40, MCS7			-69		
Radj	Adjacent channel rejection					
	OFDM, 6 Mbps	See Note[1]		TBD		dB
	OFDM, 54 Mbps			TBD		
	HT20, MCS0			TBD		
	HT20, MCS7			TBD		

Note[1]: Performance data are measured under single chain operation.

8.5 WLAN Transmitter Characteristics

Table 13: WLAN transmitter characteristics for 2.4 GHz per chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ftx	Transmit output frequency range		2.412		2.484	GHz
Pout	Output power	See Note[7]				
	11b mask compliant	1-11Mbps		18		dBm
	11g mask compliant	6-36Mbps		18		
	11g EVM compliant	48-54Mbps		16		
	11n HT20 mask compliant	MCS0-5/MCS8-13		18		
	11n HT20 EVM compliant	MCS6-7/MCS14-15		16		
	11n HT40 mask compliant	MCS0-5/MCS8-13		16		
	11n HT40 EVM compliant	MCS6-7/MCS14-15		14		
ATx	Transmit power accuracy at 25 ℃	-	-2.0	-	+2.0	dB

Freq.	Mode/Rate (Mbps)	Output Power Per Chain (dBm)	Maximum Current Consumption	
			Single Chain (mA)[8]	Dual Chains (mA)[8]
2412MHz	1 Mbps	18dBm	340	620
	54 Mbps	16dBm	280	500
	HT20 MCS7	16dBm	280	510
2422MHz	1 Mbps	18dBm	340	620
	54 Mbps	16dBm	280	500
	HT20 MCS7	16dBm	280	510
2472MHz	1 Mbps	18dBm	340	620
	54 Mbps	16dBm	280	500
	HT20 MCS7	16dBm	280	510

Table 14: WLAN transmitter characteristics for 5 GHz per chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ftx	Transmit output frequency range		5.15		5.925	GHz
Pout	Output power	See Note[3]				
	11a mask compliant	6-36Mbps		18		dBm
	11a EVM compliant	48-54Mbps		16		
	11n HT20 mask compliant	MCS0-5/MCS8-13		18		
	11n HT20 EVM compliant	MCS6-7/MCS14-15		16		
	11n HT40 mask compliant	MCS0-5/MCS8-13		16		
	11n HT40 EVM compliant	MCS6-7/MCS14-15		14		

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	11ac HT20 mask compliant	MCS0-6 (Ntst=1,2)		18		
	11ac HT20 EVM compliant	MCS7-8(Ntst=1,2)		16		
	11ac HT40 mask compliant	MCS0-5 (Ntst=1,2)		16		
	11ac HT40 EVM compliant	MCS6-8(Ntst=1,2)		14		
	11ac HT40 EVM compliant	MCS9(Ntst=1,2)		12		
	11ac HT80 mask compliant	MCS0-5 (Ntst=1,2)		14		
	11ac HT80 EVM compliant	MCS6-8(Ntst=1,2)		12		
	11ac HT80 EVM compliant	MCS9(Ntst=1,2)		10		
ATx	Transmit power accuracy at 25 ℃	-	-2.0	-	+2.0	dB

Table 15: WLAN current consumption on 5 GHz

Freq.	Mode/Rate [Mbps]	Output Power Per Chain [dBm]	Maximum Current Consumption	
			Single Chain (mA)	Dual Chains (mA)
5180 MHz	6 Mbps	18 dBm	400	710
	54 Mbps	16 dBm	330	610
	HT20 MCS0	18 dBm	400	720
	HT20 MCS7	16 dBm	360	620
5190 MHz	HT40 MCS7	14 dBm	320	550
5500 MHz	6 Mbps	18 dBm	380	680
	54 Mbps	16 dBm	330	600
	HT20 MCS0	18 dBm	370	690
	HT20 MCS7	16 dBm	320	600
5510 MHz	HT40 MCS7	14 dBm	300	530
5825 MHz	6 Mbps	18 dBm	380	690
	54 Mbps	16 dBm	310	600
	HT20 MCS0	18 dBm	360	710
	HT20 MCS7	16 dBm	340	550
5795 MHz	HT40 MCS7	14 dBm	300	530

Note: Final TX power values on each channel are limited by the regulatory certification test limit.

Note: IEEE PS current measurement with the 60-SIPT DVK was 12 mA for both 2.4 GHz and 5 GHz at all DTIM settings.

9 Bluetooth Radio Characteristics

Table 16 through Table 17 describe the basic rate transmitter performance, enhanced data transmitter performance, basic rate receiver performance, enhanced rate receiver performance, and current consumption conditions at 25°C.

Table 16: Basic rate transmitter performance temperature at 25°C (3.3V)

Test Parameter		Min	Typ	Max	BT Spec.	Unit
Maximum RF Output Power		8	10	11	0 ~ +20	dBm
Frequency Range		2.4	—	2.4835	2.4 ≤ f ≤ 2.4835	GHz
20 dB Bandwidth		—	919.5	—	≤ 1000	KHz
Δf1avg Maximum Modulation		140	165	175	140 < Δf1avg < 175	KHz
Δf2max Minimum Modulation		—	135	—	≥ 115	KHz
Δf2avg/Δf1avg		—	0.9	—	≥ 0.80	—
Initial Carrier Frequency		—	+/-5	—	≤±75	KHz
Drift Rate (DH1 package)		—	4	—	≤ 20	KHz/50 µs
Drift (DH3 packet)		—	8	—	≤25	KHz
Drift (DH5 packet)		—	7	—	≤ 40	KHz
Adjacent Channel Power	F≥ ± 3MHz	—	-50	—	< -40	dBm
	F = ± 2MHz	—	-46	—	≤ -20	dBm
	F = ± 1MHz	—	-15	—	N/A	dBm

Table 17: Enhanced data rate transmitter performance 25°C (3.3V)

Test Parameter		Min	Typ	Max	BT Spec.	Unit
Relative Transmit Power		5	7	9		dBm
Max Carrier Frequency Stability Iwol	2-DH5	—	1	—	≤ ±10	KHz
	3-DH5	—	1	—		
Max Carrier Frequency Stability Iwil	2-DH5	—	4	—	≤ ±75	KHz
	3-DH5	—	4	—		
Max Carrier Frequency Stability Iw0+wil	2-DH5	—	5	—	≤ ±75	KHz
	3-DH5	—	5	—		
RMS DEVM	2-DH5	—	4	—	≤ 20	%
	3-DH5	—	4	—	≤13	%
Peak DEVM	2-DH5	—	9	—	≤ 35	%
	3-DH5	—	9	—	≤ 25	%
99% DEVM	2-DH5	—	12	—	≤ 30	%
	3-DH5	—	12	—	≤ 20	%
EDR Differential Phase Encoding		—	99	—	≥ 99	%
Adjacent Channel Power	F≥ ± 3MHz	—	TBD	—	< -40	dBm
	F = ± 2MHz	—	TBD	—	≤ -20	dBm

Table 18: Basic rate receiver performance at 3.3V

Test Parameter		Min	Typ	Max	BT Spec.	Unit
Sensitivity (1DH5)	BER ≤ 0.1%	—	-95	-92	≤ -70	dBm
Maximum Input	BER ≤ 0.1%	-20	-10	—	≥ -20	dBm
Carrier-to-Interferer Ratio (C/I)	Co-Channel	—	10	11	11	
	C/I (± 1 MHz)	—	-4	0	0	dB
	C/I (± 2 MHz)	—	-45	—	-30	dB
	C/I (± 3 MHz)	—	-49	—	-40	dB
Maximum Level of Intermodulation Interferers		-39	-30	-	≥ -39	dBm

Table 19: Enhanced data rate receiver performance 3.3V

Test Parameter		Min	Typ	Max	Bluetooth Specification	Unit
Sensitivity (BER ≤0.01%)	π/4 DQPSK	—	-94	-91	≤ -70	dBm
	8 DPSK	—	-88	-85	≤ -70	dBm
Maximum Input (BER ≤0.1%)	π/4 DQPSK	-20	—	—	≥ -20	dBm
	8 DPSK	-20	—	—	≥ -20	dBm
Co-Channel C/I (BER ≤0.1%)	π/4 DQPSK	—	10	13	≤ ±13	dB
	8 DPSK	—	16	20	≤ ±20	dB
Adjacent Channel C/I (1MHz)	π/4 DQPSK	—	-9	0	≤ 0	dB
	8 DPSK	—	-6	5	≤5	dB
Second Adjacent Channel C/I (2MHz)	π/4 DQPSK	—	-47	-30	≤ -30	dB
	8 DPSK	—	-42	-25	≤ -25	dB
Third Adjacent Channel C/I (3MHz)	π/4 DQPSK	—	-51	-40	≤ -40	dB
	8 DPSK	—	-48	-33	≤ -33	dB
Out-of-band blocking	30-2000MHz	—	-12.5	—	—	dBm
	2-2.399GHz	—	-12.4	—	—	dBm
	2.484-3GHz	—	-18	—	—	dBm
	3-12.75GHz	—	-2.6	—	—	dBm

10 Host Interface Specifications

10.1 SDIO Specifications

The 60-SIPT series SDIO host interface pins are powered from the VIO_SD voltage supply. The SDIO electrical specifications are identical for the 1-bit SDIO and 4-bit SDIO modes.

10.1.1 Default Speed, High-speed Modes

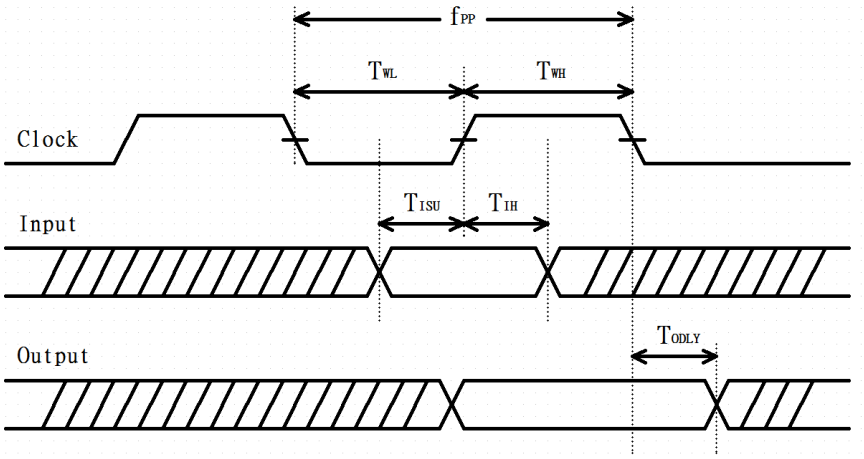


Figure 2: SDIO protocol timing diagram--- default mode (3.3V)

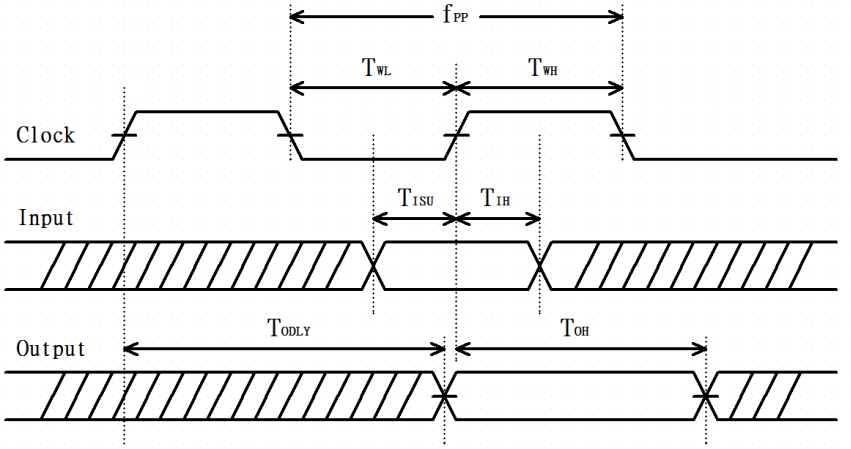


Figure 3: SDIO protocol timing diagram--- High-Speed mode (3.3V)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 20: SDIO timing requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fPP	Clock Frequency	Default Speed	0	-	25	MHz
		High-Speed	0	-	50	
TWL	Clock low time	Default Speed	10	-	-	ns
		High-Speed	7	-	-	
TWH	Clock high time	Default Speed	10	-	-	ns

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
		High-Speed	7	-	-	
TISU	Input Setup time	Default Speed	5	-	-	ns
		High-Speed	6	-	-	
TIH	Input Hold time	Default Speed	5	-	-	ns
		High-Speed	2	-	-	
TODLY	Output delay time	Default Speed	-	-	14	ns
	CL≦40pF (1 card)	High-Speed	-	-	14	
TOH	Output hold time	High-Speed	0	-	-	ns

10.1.2 SDR12, SDR25, SDR50 Mode (up to 100MHz) (1.8V)

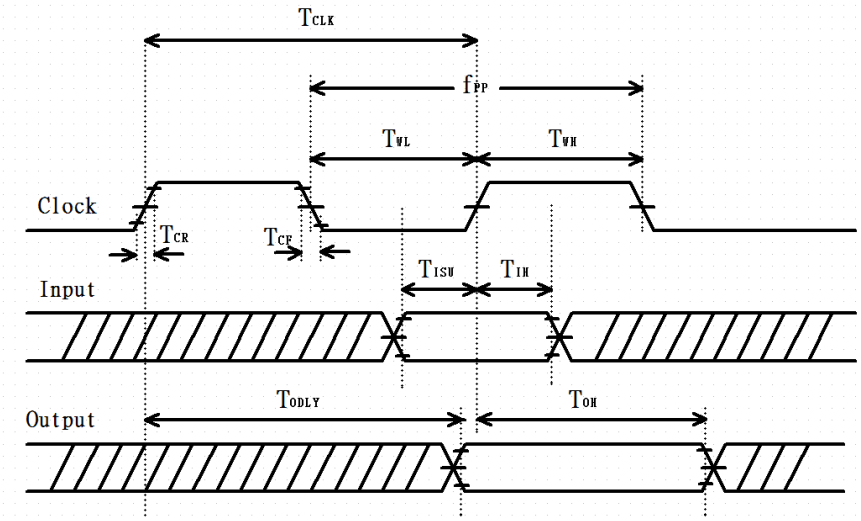


Figure 4: SDIO protocol timing Diagram--- SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 21: SDIO timing requirements--- SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fPP	Clock Frequency	SDR12/25/50	25	-	100	MHz
TISU	Input setup time	SDR12/25/50	3	--	-	ns
TIH	Input Hold time	SDR12/25/50	0.8	-	-	ns
TCLK	Clock Time	SDR12/25/50	10	-	40	ns
TCR, TCF	Raise time, Fall time	SDR12/25/50	-	-	0.2*TCLK	ns
	TCR, TCF＜2ns (max) at 100MHz					
	CCARD=10pF					
TODLY	Output delay time	SDR12/25/50	-	-	7.5	ns
	CL≦30pF					

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
TOH	Output hold time CL=15pF	SDR12/25/50	1.5	-	-	ns

10.1.3 SDR104 Mode (208 MHz) (1.8V)

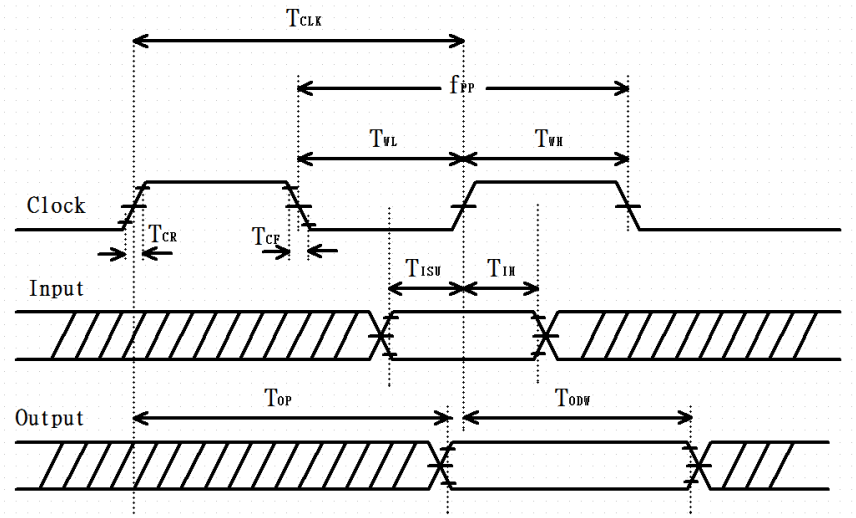


Figure 5: SDIO protocol timing Diagram--- SDR104 modes (up to 208 MHz) (1.8V)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 22: SDIO timing requirements--- SDR104 modes (up to 208MHz) (1.8V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fPP	Clock Frequency	SDR104	0	-	208	MHz
TISU	Input setup time	SDR104	1.4	--	-	ns
TIH	Input Hold time	SDR104	0.8	-	-	ns
TCLK	Clock Time	SDR104	4.8	-	-	ns
TCR, TCF	Raise time, Fall time TCR, TCF < 0.96ns (max) at 208MHz CCARD=10pF	SDR104	-	-	0.2*TCLK	ns
TOP	Card Output phase	SDR104	0	-	10	ns
TODW	Output timing pf variable data window	SDR12/25/50	2.88	-	-	ns

10.1.4 DDR50 Mode (50MHz) (1.8V)

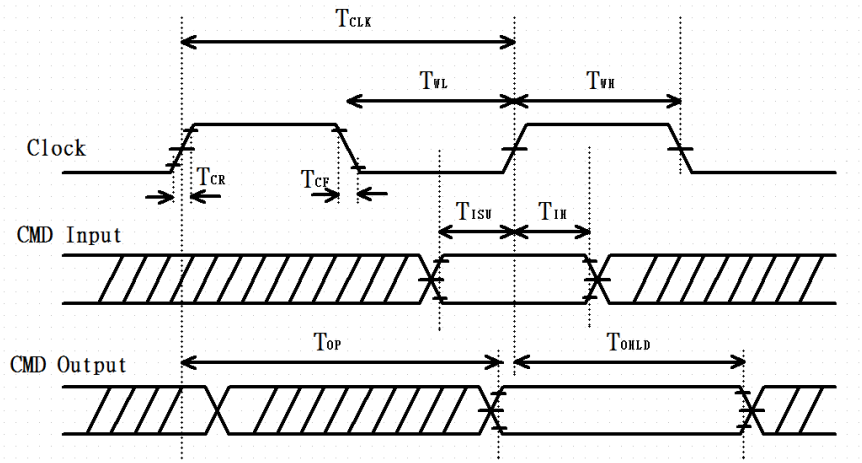


Figure 6: SDIO CMD timing diagram--- DDR50 modes (50 MHz) (1.8V)

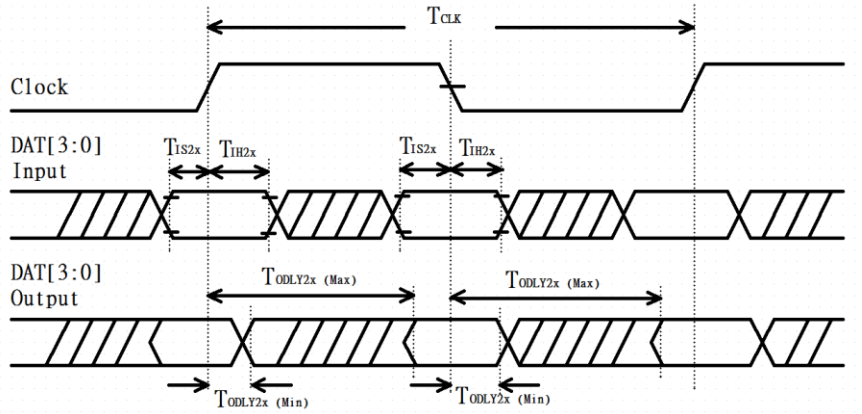


Figure 7: SDIO DAT[3:0] timing Diagram--- DDR50 modes (50 MHz) (1.8V)

Note: In DDR50 mode, DAT[3:0] lines are samples on both edges pf the clock (not applicable for CMD line)

Table 23: SDIO timing requirements – DDR50 modes (50 MHz)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Clock						
TCLK	Clock time 50MHz (max) between rising edge	DDR50	20	--	--	ns
TCR, TCF	Rise time, fall time TCR, TCF < 4.00ns (max) at 50MHz. CCARD=10pF	DDR50	--	--	0.2*TCLK	ns
Clock Duty	--	DDR50	45	--	55	%
CMD Input (referenced to clock rising edge)						
TIS	Input setup time CCARD≦10pF (1 card)	DDR50	6	--	--	ns
TIH	Input hold time	DDR50	0.8	--	--	ns

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
	CCARD≦10pF (1 card)					
CMD Output (referenced to clock rising and failing edge)						
TODLY	Output delay time during data transfer mode CL≦30pF (1 card)	DDR50	--	--	13.7	ns
TOHLD	Output hold time CL≥15pF (1 card)	DDR50	1.5	--	--	ns
DAT[3:0] Input (referenced to clock rising and failing edges)						
TIS2X	Input setup time CCARD≦10pF (1 card)	DDR50	3	--	--	ns
TIH2X	Input hold time CCARD≦10pF (1 card)	DDR50	0.8	--	--	ns
DAT[3:0] Output (referenced to clock rising and failing edges)						
TODLY2X (max)	Output delay time during data transfer mode CL≦25pF (1 card)	DDR50	--	--	7.0	ns
TODLY2X (min)	Output hold time CL≥15pF (1 card))	DDR50	1.5	--	--	ns

10.2 PCI Express Specifications

The PCI Express host interface pins are powered from the 1.8V generated by the PMU inside the 60-SIPT series.

10.2.1 Differential TX Output Electricals

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 24: PCI Express TX Output Specifications – 2.5GT/s

Symbol	Parameter	Min.	Typ.	Max.	Unit
UI	Unit interval (UI) The specified UI is equivalent to a tolerance of +/-300ppm for each Refclk source. Period does not account for SSC induced variations.	399.88	-	400.12	Ps
VTX-DIFF-PP	Differential peak-to-peak TX voltage swing VTX-DIFF-PP=2* | VTXD+ – VTXD-|	0.8	-	1.2	V
VTX-DIFF-PP-LOW	Low power differential peak-to-peak TX voltage swing VTX-DIFF-PP=2* | VTXD+ – VTXD-|	0.4	-	1.2	V
VTX-DE-RATIO-3.5dB	Tx de-emphasis level ratio (3.5dB)	3.0	-	4.0	V
TTX-EYE	Tx eye including all jitter sources	0.75	-	-	UI
TTX-EYE-MEDIAN-to-MAX-JITTER	Maximum time between jitter median and maximum deviation from median	-	-	0.125	UI
TTX-RISE-FALL	Tx rise/fall time	0.125	-	-	UI

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Measured differentially from 20% to 80%				
RLTX-DIFF	Tx package plus Si differential return loss	10	-	-	dB
RLTX-CM	Tx package plus Si common mode return loss	6	-	-	dB
VTX-CM-AC-P	Tx AC common mode voltage	-	20	-	mV
ITX-SHORT	Tx short circuit current limit	-	-	90	mA
VTX-DC-CM	Tx DC common mode voltage	-	-	3.6	V
VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common mode voltage during L0 and electrical idle.	0	-	100	mV
VTX-IDLE-DIFF-AC-p	Electrical idle differential peak output voltage	0	-	20	mV
TTX-IDLE-MIN	Minimum time spent in electrical idle	20	-	-	ns
TTX-IDLE-SET-TO-IDLE	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	-	-	8	ns
TTX-IDLE-TO-DIFF-DATA	Maximum time to transition to valid diff signalling after leaving electrical idle	-	-	8	ns
TCROSLINK	Crosslink random timeout	-	-	1.0	ms
CTX	AC coupling capacitor	75	-	200	nF

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 25: PCI Express TX Output Specifications - 5GT/s

Symbol	Parameter	Min.	Typ.	Max.	Unit
UI	Unit interval (UI) The specified UI is equivalent to a tolerance of +/-300ppm for each Refclk source. Period does not account for SSC induced variations.	199.94	-	200.06	Ps
VTX-DIFF-PP	Differential peak-to-peak TX voltage swing VTX-DIFF-PP=2* | VTXD+ – VTXD- |	0.8	-	1.2	V
VTX-DIFF-PP-LOW	Low power differential peak-to-peak TX voltage swing VTX-DIFF-PP=2* | VTXD+ – VTXD- |	0.4	-	1.2	V
VTX-DE-RATIO-3.5dB	Tx de-emphasis level ratio (3.5dB)	3.0	-	4.0	V
VTX-DE-RATIO-6dB	Tx de-emphasis level ratio (6dB)	5.5	-	6.5	V
TMIN-PULSE	Instantaneous lone pulse width Measured relative to rising/failing pulse	0.9	-	-	UI
TTX-EYE	Tx eye including all jitter sources	0.75	-	-	UI
TTX-HF-DJ-DD	Tx deterministic jitter > 1.5MHz Deterministic jitter only	-	-	0.15	UI
TTX-LF-RMS	Tx RMS jitter < 1.5MHz	-	3.0	-	Ps RMS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Total energy measured over a 10KHz-1.5MHz range				
TTX-RISE-FALL	Tx rise/fall time Measured differentially from 20% to 80%	0.15	-	-	UI
RLTX-DIFF	Tx package plus Si differential return loss (0.05-1.25GHz) (1.25-2.5GHz)	10 8	-	-	dB
RLTX-CM	Tx package plus Si common mode return loss	6	-	-	dB
VTX-CM-AC-PP	Tx AC common mode voltage	-	-	100	mV
ITX-SHORT	Tx short circuit current limit	-	-	90	mA
VTX-DC-CM	Tx DC common mode voltage	-	-	3.6	V
VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common mode voltage during L0 and electrical idle.	0	-	100	mV
VTX-IDLE-DIFF-AC-p	Electrical idle differential peak output voltage VTX-IDLE-DIFF-DC= | VTX-IDLE-D+ – VTX-IDLE-D- | ≦ 20mV	0	-	20	mV
VTX-IDLE-DIFF-DC	DC Electrical idle differential output voltage VTX-IDLE-DIFF-DC= | VTX-IDLE-D+ – VTX-IDLE-D- | ≦5mV	0	-	5	mV
VTX-RCVDETECT	Voltage change allowed during receiver detection	0	-	600	mV
TTX-IDLE-MIN	Minimum time spent in electrical idle	20	-	-	ns
TTX-IDLE-SET-TO-IDLE	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	-	-	8	ns
TTX-IDLE-TO-DIFF-DATA	Maximum time to transition to valid diff signalling after leaving electrical idle	-	-	8	ns
TCROSLINK	Crosslink random timeout	-	-	1.0	ms
CTX	AC coupling capacitor	75	-	200	nF

10.2.2 Differential RX input Electricals

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 26: PCI Express RX Output Specifications – 2.5GT/s

Symbol	Parameter	Min.	Typ.	Max.	Unit
UI	Unit interval (UI) The specified UI is equivalent to a tolerance of +/-300ppm for each Refclk source. Period does not account for SSC induced variations.	399.88	-	400.12	Ps
VRX-DIFF-PP-CC	Differential RX peak-to-peak voltage for common Refclk RX architecture	0.175	-	1.2	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VRX-DIFF-PP-DC	Differential RX peak-to-peak voltage for data clocked Refclk RX architecture	0.175	-	1.2	V
TRX-EYE	Rx eye time opening Minimum eye time at Rx pins to yield a 10^{-12} BER	0.4	-	-	UI
TRX-EYE-MEDIAN-to-MAX-JITTER	Maximum time delta between median and deviation from median	-	-	0.3	UI
VRX-CM-ACp	AC peak common mode input voltage	-	-	150	mV
RLRX-DIFF	Differential return loss	15	-	-	dB
RLRX-CM	Common mode return loss	0	-	3.6	dB
ZRX-DIFF-DC	DC differential input impedance	80	100	120	Ω
ZRX-DC	DC input impedance	40	50	60	Ω
ZRX-HIGH-IMP-DC	Powered down DC input impedance	200	-	-	KΩ
VRX-IDLE-DET-DIFF-p-p	Electrical idle detect threshold	65	-	175	mV
TRX-IDLE-DIFF-ENTERTIME	Unexpected electrical idle enter detect threshold integration time	-	-	10	ms
LRX-SKEW	Total Skew	-	-	20	ns

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 27: PCI Express RX Output Specifications – 5GT/s

Symbol	Parameter	Min.	Typ.	Max.	Unit
UI	Unit interval (UI) The specified UI is equivalent to a tolerance of +/-300ppm for each Refclk source. Period does not account for SSC induced variations.	199.94	-	200.06	ps
VRX-DIFF-PP-CC	Differential RX peak-to-peak voltage for common Refclk RX architecture	0.12	-	1.2	V
VRX-DIFF-PP-DC	Differential RX peak-to-peak voltage for data clocked Refclk RX architecture	0.1	-	1.2	V
TRX-TJ-CC	Maximum Rx inherent total timing error for common Refclk RX architecture	-	-	0.4	UI
TRX-TJ-DC	Maximum Rx inherent total timing error for data clocked RX architecture	-	-	0.34	UI
TRX-DJ-DD-CC	Maximum Rx inherent deterministic timing error for common Refclk RX architecture	-	-	0.3	UI
TRX-DJ-DD-DC	Maximum Rx inherent deterministic timing error for data clocked RX architecture	-	-	0.24	UI
TRX-MIN-PULSE	Minimum width pulse at Rx	0.6	-	-	UI

Symbol	Parameter	Min.	Typ.	Max.	Unit
VRX-CM-ACp	AC peak common mode input voltage	-	-	150	mV
RLRX-DIFF	Differential return loss	15	-	-	dB
RLRX-CM	Common mode return loss	1-	-	3.6	dB
ZRX-DIFF-DC	DC differential input impedance	80	100	120	Ω
ZRX-DC	DC input impedance	40	50	60	Ω
ZRX-HIGH-IMP-DC	Powered down DC input impedance	200	-	-	KΩ
VRX-IDLE-DET-DIFF-p-p	Electrical idle detect threshold	65	-	175	mV
TRX-IDLE-DIFF-ENTERTIME	Unexpected electrical idle enter detect threshold integration time	-	-	10	ms
LRX-SKEW	Total Skew	-	-	20	ns

10.3 USB Specifications

10.3.1 USB LS Driver and Receiver Parameters

Notes: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

The load is 100Ω differential for these parameters, unless other specified.

Table 28: USB LS driver and receiver specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
BR	Baud rate	-	1.5	-	Mbps
BRPPM	Baud rate tolerance	-15000	-	15000	ppm
Driver Specifications					
VOH	Output signal ended high Defined with 1.425KΩ pull-up resistor to 3.6V	2.8	-	3.6	V
VOL	Output signal ended low Defined with 1.425KΩ pull-up resistor to ground	0.0	-	0.3	V
VCRS	Output signal crossover voltage	1.3		2.0	V
TLR	Data fall time Defined from 10% to 90% for raise time and 90% to 10% for fall time	75.0	-	300.0	ns
TLF	Data rise time Defined from 10% to 90% for raise time and 90% to 10% for fall time	75.0	-	300.0	ns
TLRFM	Rise and fall time matching	80.0	-	125.0	%
TUDJ1	Source jitter total: to next transition *Including frequency tolerance. Timing difference between the differential data signals.	-95	-	95	ns

Symbol	Parameter	Min.	Typ.	Max.	Unit
	*Defined at crossover point of differential signals				
TUDJ2	Source jitter total: for paired transitions *Including frequency tolerance. Timing difference between the differential data signals. *Defined at crossover point of differential signals	-150	-	150	ns
Receiver Specifications					
VIH	Input signal ended high	2.0	-	-	V
VIL	Input signal ended low	-	-	0.8	V
VDI	Differential input sensitivity	0.2	-	-	V

10.3.2 USB FS Driver and Receiver Parameters

Notes: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

The load is 100Ω differential for these parameters, unless other specified.

Table 29: USB FS Driver and Receiver Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
BR	Baud rate	-	12.0	-	Mbps
BRPPM	Baud rate tolerance	-2500	-	2500	ppm
Driver Specifications					
VOH	Output signal ended high Defined with 1.425KΩ pull-up resistor to 3.6V	2.8	-	3.6	V
VOL	Output signal ended low Defined with 1.425KΩ pull-up resistor to ground	0.0	-	0.3	V
VCRS	Output signal crossover voltage	1.3		2.0	V
TFR	Output raise time Defined from 10% to 90% for raise time and 90% to 10% for fall time	-4.0	-	20.0	ns
TFL	Output fall time Defined from 10% to 90% for raise time and 90% to 10% for fall time	-4.0	-	20.0	ns
TDJ1	Source jitter total: to next transition *Including frequency tolerance. Timing difference between the differential data signals. *Defined at crossover point of differential signals	-3.5	-	3.5	ns
TDJ2	Source jitter total: for paired transitions *Including frequency tolerance. Timing difference between the differential data signals.	-4.0	-	4.0	ns

Symbol	Parameter	Min.	Typ.	Max.	Unit
	*Defined at crossover point of differential signals				
TFDEOP	Source jitter for differential transition to SE0 transition. Defined at crossover point of differential signals	-2.0	-	5.0	ns
Receiver Specifications					
VIH	Input signal ended high	2.0	-	-	V
VIL	Input signal ended low	-	-	0.8	V
VDI	Differential input sensitivity	0.2	-	-	V
TJR1	Receiver jitter: to next transition Defined at crossover point of differential data signals	-18.5	-	18.5	ns
TJR2	Receiver jitter: for paired transitions Defined at crossover point of differential data signals	-9.0	-	9.0	ns

10.3.3 USB HS Driver and Receiver Parameters

Notes: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

The load is 100Ω differential for these parameters, unless other specified.

Table 30: USB HS Driver and Receiver Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
BR	Baud rate	-	480	-	Mbps
BRPPM	Baud rate tolerance	-500	-	500	ppm
Driver Specifications					
VHSOH	Data signal high	360	-	440	mV
VHSOL	Data signal low	-10	-	10	mV
THSR	Data rise time Defined from 10% to 90% for raise time and 90% to 10% for fall time	500	-	-	ns
THSF	Data fall time Defined from 10% to 90% for raise time and 90% to 10% for fall time	-500	-	-	ns
Receiver Specifications					
VHSCM	Input signal ended low	-50	-	500	mV

10.4 PCM Interface Specifications

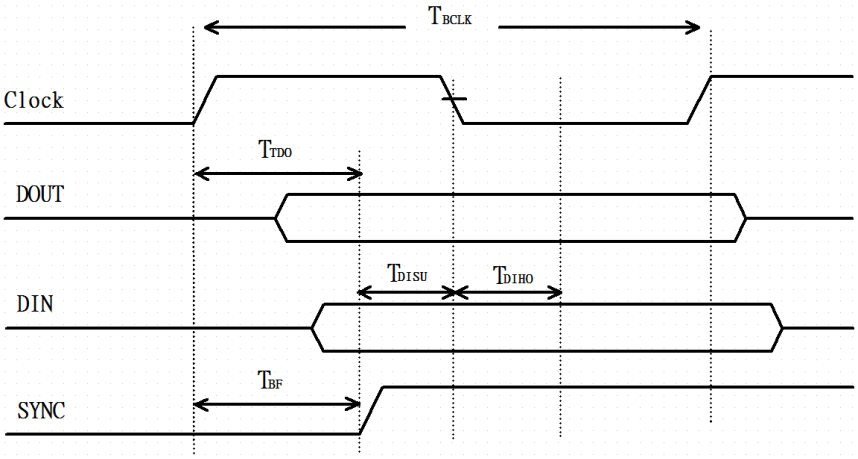


Figure 8: PCM Timing Specification – Master Mode

Table 31: PCM Timing Specification – Master Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
FBCLK	-	-	2/2.048	-	MHz
Duty CycleBCLK	-	0.4	0.5	0.6	-
TBCLK rise/fall	-	-	3	-	ns
TDO	-	-	-	15	ns
TDISU	-	20	-	-	ns
TDIHO	-	15	-	-	ns
TBF	-	-	-	15	ns

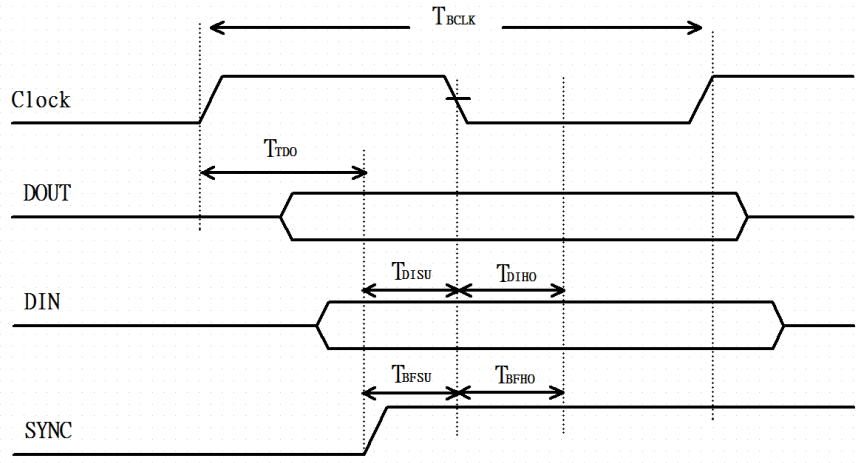


Figure 9: PCM Timing Specification – Slave Mode

Table 32: PCM Timing Specification – Slave Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
FBCLK	-	-	2/2.048	-	MHz
Duty CycleBCLK	-	0.4	0.5	0.6	-

Symbol	Parameter	Min.	Typ.	Max.	Unit
TBCLK rise/fall	-	-	3	-	ns
TDO	-	-	-	30	ns
TDISU	-	15	-	-	ns
TDIHO	-	10	-	-	ns
TBFSU	-	15	-	-	ns
TBFHO	-	10	-	-	ns

11 Pin Definitions

Note: AVDD18 is generated by PMU internally. No need to power from outside the SIP.

Table 33: Pin definitions of 60-SIPT series

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
1	PDn	I	-	Full Power-Down (input) (Active low) 0=full power-down mode; 1=normal mode PDn can accept an input range from 1.8V to 3.6V **PDn must be high for normal operation. Please connect to pin-32 (1.8V_OUT) through 49.9KΩ.**	--
2	GND	-	-	Ground	GND
3	GND	-	-	Ground	GND
4	ANT1 (RF_B)/WIFI+BT	A,I/O	-	RF Transmit/Receive Wi-Fi and BT share the same path.	50Ω Load
5	GND	-	-	Ground	GND
6	GND	-	-	Ground	GND
7	GND	-	-	Ground	GND
8	GND	-	-	Ground	GND
9	GND	-	-	Ground	GND
10	GND	-	-	Ground	GND
11	GND	-	-	Ground	GND
12	ANT0 (RF_A)/WIFI ONLY	A,I/O	-	RF Transmit/Receive Wi-Fi only	50Ω Load
13	GND	-	-	Ground	GND
14	GND	-	-	Ground	GND
15	CONFIG_HOST2	I, PU	AVDD18	Host interface configuration setting. Detail configuration table are shown in Table 32	-

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
				To set a configuration bit to "0", attach a 100kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to "1".	
16	CONFIG_HOST1	I, PU	AVDD18	Host interface configuration setting. Detail configuration table are shown in Table 32 To set a configuration bit to "0", attach a 100kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to "1".	-
17	CONFIG_HOST0	I, PU	AVDD18	Host interface configuration setting. Detail configuration table are shown in Table 32 To set a configuration bit to "0", attach a 100kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to "1".	-
18	GND	-	-	Ground	GND
19	PCM_CLK	I/O	VIO	PCM Clock Signal (Optimal) Optimal clock used for some codecs. Output if Master mode; Input if Slave mode.	N/C
20	PCM_DOUT	O	VIO	PCM Data	N/C
21	PCM_SYNC	I/O	VIO	PCM Sync Pulse Signal Output if Master mode; Input if Slave mode.	N/C
22	PCM_DIN	I	VIO	PCM Data	N/C
23	GPIO0	I/O	VIO	General purpose I/O pin. Reserved for WoW (Wake on WLAN) feature.	N/C
24	GND	-	-	Ground	GND
25	PCIE_WAKEn	I/O	VIO	PCIe wake signal (input/output) (active low)	N/C
26	PCIE_CLKREQn	I/O	VIO	PCIe clock request (input/output) (active low)	N/C
27	PCIE_PERSTn	I, PD	VIO	PCIe host indication to reset the device (input) (active low)	N/C
28	PCIE_W_DISABLEn	I, PU	VIO	PCIe host indication to disable the WLAN function of the device (input) (active low)	N/C
29	LTE_SOUT/ JTAG_TDO	O, PD O, PD	VIO	Serial data to external LTE device/ JTAG Test Data Out (TDO)	N/C
30	LTE_SIN/ JTAG_TDI	I, PD I, PD	VIO	Serial data from external LTE device/ JTAG Test Data Input (TDI)	N/C
31	VIO	Power	-	1.8V/2.5V/3.3V Digital I/O Power Supply	-

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
32	1.8V_OUT	Power	-	1.8V output from 60-SIPT series. Used to pull-up the PDn pin for POR. Note: Do NOT used as power source for other circuits.	N/C
33	GND	-	-	Ground	GND
34	32KHz	I, PU	VIO	Sleep Clock Input An external sleep clock of 32.768KHz with minimum +/- 250ppm is required for power saving mode	-
35	GND	-	-	Ground	GND
36	PCIE_RCLK_N	I	AVDD18	PCIe Differential Clock Input-Negative	N/C
37	PCIE_RCLK_P	I	AVDD18	PCIe Differential Clock Input-Positive	N/C
38	GND	-	-	Ground	GND
39	PCIE_TX_P	O	AVDD18	PCIe Transmit Data-Positive	N/C
40	PCIE_TX_N	O	AVDD18	PCIe Transmit Data-Negative	N/C
41	GND	-	-	Ground	GND
42	PCIE_RX_N	I	AVDD18	PCIe Receive Data-Negative	N/C
43	PCIE_RX_P	I	AVDD18	PCIe Receive Data-Positive	N/C
44	GND	-	-	Ground	GND
45	USB_DN	I/O	3V3	USB Differential Data-Negative	N/C
46	USB_DP	I/O	3V3	USB Differential Data-Positive	N/C
47	GND	-	-	Ground	GND
48	3V3	Power	-	3.3V module power supply **Note:** A 10u MLCC is needed for this pin. Place the capacitor close to this pin as possible. Ref. parts: GRM188R60J106ME47D (MURATA) or CC0805KKX7R6BB106 (YAGO)	-
49	3V3	Power	-	3.3V module power supply **Note:** A 10u MLCC is needed for this pin. Place the capacitor close to this pin as possible. Ref. parts: GRM188R60J106ME47D (MURATA) or CC0805KKX7R6BB106 (YAGO)	-
50	GND	-	-	Ground	GND
51	PMU_EN	I		Enable input for all Regulators inside the 60-SIPT series when it is “H” state. The 60-SIPT will be off when it is “L” state. Note: DO NOT float this pin. Pull-up to 3.3V with 100K for normal operation.	100K, PU

Pin #	Name	Type	Voltage Ref.	Description	If Not Used
				Note: This pin should be connected to a system GPIO so that the module can be reset under software control.	
52	VIO_SD	Power	-	1.8V/3.3V Digital I/O SDIO Power Supply	-
53	SDIO_DATA0	I/O, PU	VIO_SD	SDIO 4-bit Mode DATA line Bit[0]	N/C
54	SDIO_DATA1	I/O, PU	VIO_SD	SDIO 4-bit Mode DATA line Bit[1]	N/C
55	SDIO_DATA2	I/O, PU	VIO_SD	SDIO 4-bit Mode DATA line Bit[2]	N/C
56	SDIO_DATA3	I/O, PU	VIO_SD	SDIO 4-bit Mode DATA line Bit[3]	N/C
57	SDIO_CMD	I/O, PU	VIO_SD	SDIO 4-bit Mode Command/Response	N/C
58	SDIO_CLK	I, PU	VIO_SD	SDIO 4-bit Mode Clock Input	N/C
59	GND	-	-	Ground	GND
60	UART_TXD	O, WPU	VIO	UART Serial Data Output	N/C
61	UART_RXD	I, WPU	VIO	UART Serial Data Input	N/C
62	UART_CTSn	I, PU	VIO	UART Clear to Send (Active low)	N/C
63	UART_RTSn	O, WPU	VIO	UART Request to Send (Active low)	N/C
64	GND	-	-	Ground	GND
65	JTAG_TCK	I, PU	VIO	JTAG Test Clock (input)	N/C
66	JTAG_TMS	I, PU	VIO	JTAG Test Controller Select (input)	N/C
67	LED_OUT_BT	O, PU	VIO	LED indicator for BT with 10 mA drive capability. Reserved for BT wake up Host feature.	N/C
68	LED_OUT_WLAN	O, PU	VIO	LED indicator for WLAN with 10mA drive capability	N/C
69-84	GND	-	-	Thermal Ground Pad **(Important for RF performance and thermal dissipation; please flow the reference design)**	GND

12 Host Configuration Options

60-SIPT series support various host configurations for WLAN and BT. Its detail configurations are shown in following table (Table 34).

Table 34: Wi-Fi host interface configuration table

CONFIG_HOST [2-0]	WLAN	BT/BLE	Note
000	SDIO	UART	-
001	SDIO	SDIO	-
010	PCIe	USB 2.0	Initial USB 2.0 PHY and COM PHY PCIe portion
011	PCIe	UART	Initial only COM PHY PCIe portion
100	USB 2.0	UART	Initial USB 2.0 PHY
101	USB 2.0	USB 2.0	Initial only USB 2.0 PHY

13 Mechanical Specifications

Module dimensions of 60-SIPT series is 13 x 14 x 1.85 mm. Detail drawings are shown in Figure 10.

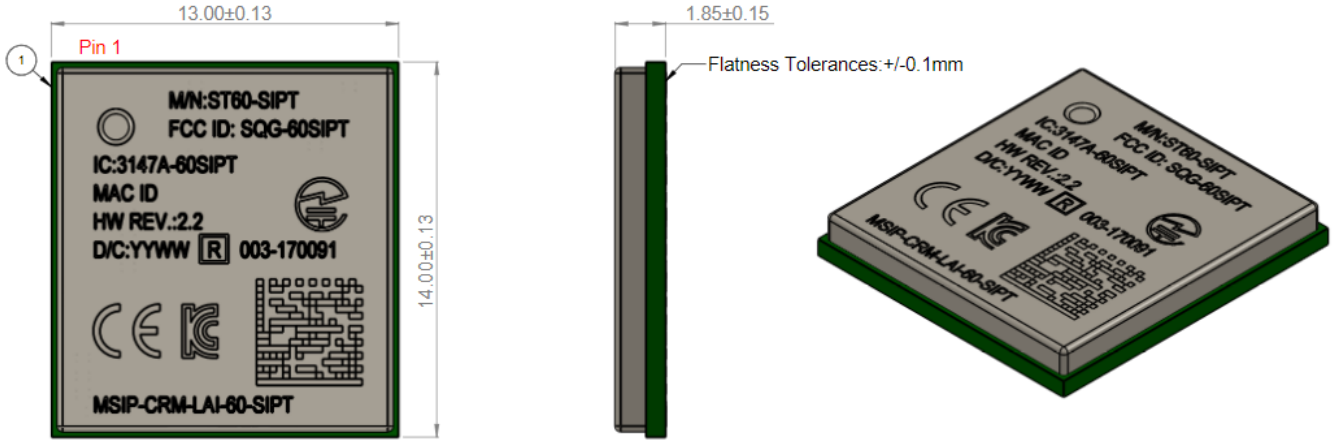


Figure 10: Mechanical drawing - 60-SIPT

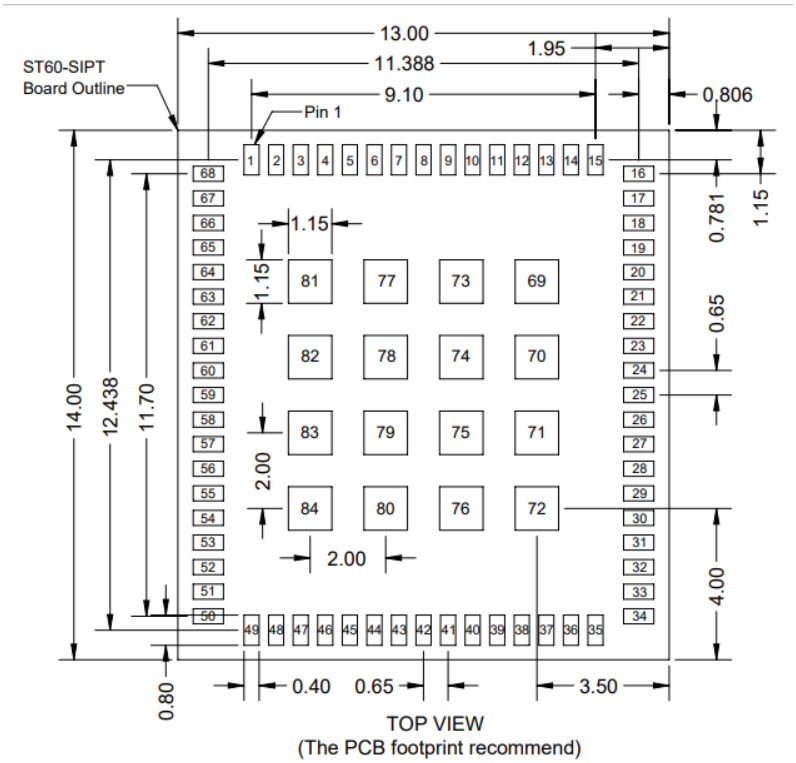


Figure 11: Module dimension of 60-SIPT series – Top View

Note: The Wi-Fi MAC address is located on the product label.

The last digit of Wi-Fi MAC address is assigned to either *0, 4, 8,* or *C*.

The BT MAC address is the Wi-Fi MAC address plus 3.

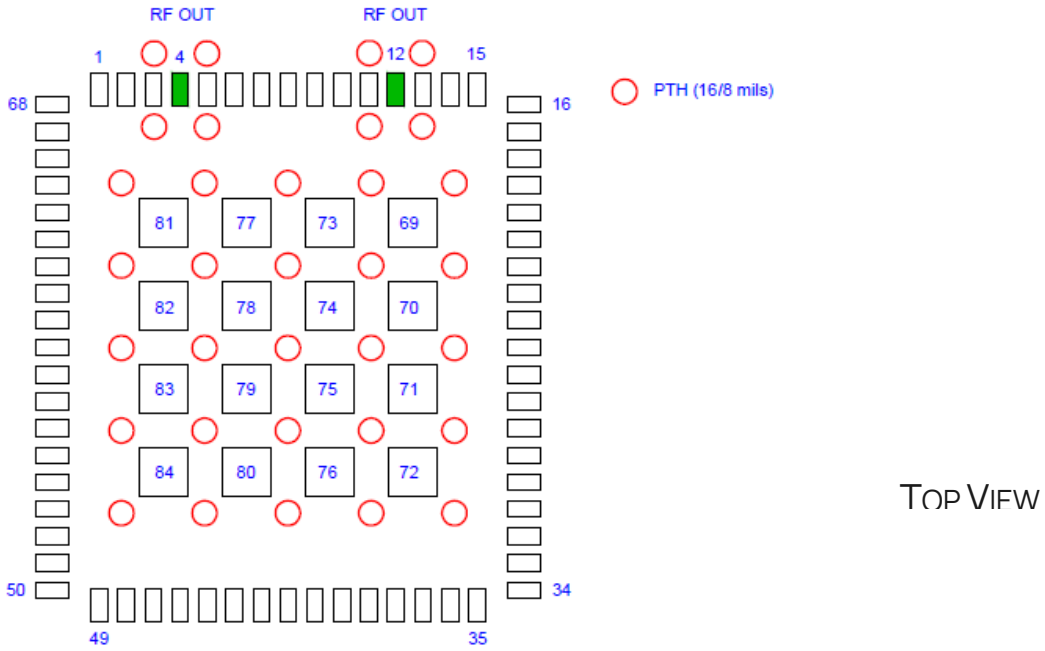


Figure 12: Recommended ground via

Recommend minimal via size and placement for grounding and thermal dissipation. Please double the ground via number when using laser via on HID process. More ground via and the use of 1-oz copper is recommended in our design to get better thermal dissipation.

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

14 RF Layout Design Guidelines

The following is a list of RF layout design guidelines and recommendation when installing a Ezurio radio into your device.

- Do not run antenna cables directly above or directly below the radio.
- Do not place any parts or run any high speed digital lines below the radio.
- If there are other radios or transmitters located on the device (such as a *Bluetooth* radio), place the devices as far apart from each other as possible. Also, make sure there is at least 25 dB isolation between these two antennas.
- Ensure that there is the maximum allowable spacing separating the antenna connectors on the Ezurio radio from the antenna. In addition, do not place antennas directly above or directly below the radio.
- Ezurio recommends the use of a double-shielded cable for the connection between the radio and the antenna elements.
- Be sure to put a 10uF capacitor on EACH 3.3V power pin. Also, place that capacitor to the pin as close as possible to make sure the internal PMU working correctly.
- Use proper electro-static-discharge (ESD) procedures when installing the Ezurio radio module.
- To get maximum throughput when operate at MIMO 2x2, two antennas with at least 25 dB isolation is recommended.
- To avoid negatively impacting Tx power and receiver sensitivity, do not cover the antennas with metallic objects or components.

15 Recommended Storage, Handling, Baking, and Reflow Profile

15.1 Required Storage Conditions

15.1.1 Prior to Opening the Dry Packing

The following are required storage conditions ***prior* to opening the dry packing**:

- Normal temperature: 5~40℃
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means Relative Humidity.

15.1.2 After Opening the Dry Packing

The following are required storage conditions ***after* opening the dry packing** (to prevent moisture absorption):

- Storage conditions for one-time soldering:
  - Temperature: 5-25°C
  - Humidity: 60% or less
  - Period: 72 hours or less after opening
- Storage conditions for two-time soldering

  Storage conditions following opening and prior to performing the 1st reflow:
  - Temperature: 5-25°C
  - Humidity: 60% or less
  - Period: A hours or less after opening

  Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
  - Temperature: 5-25°C
  - Humidity: 60% or less
  - Period: B hours or less after completion of the 1st reflow

  Note: Should keep A+B within 72 hours.

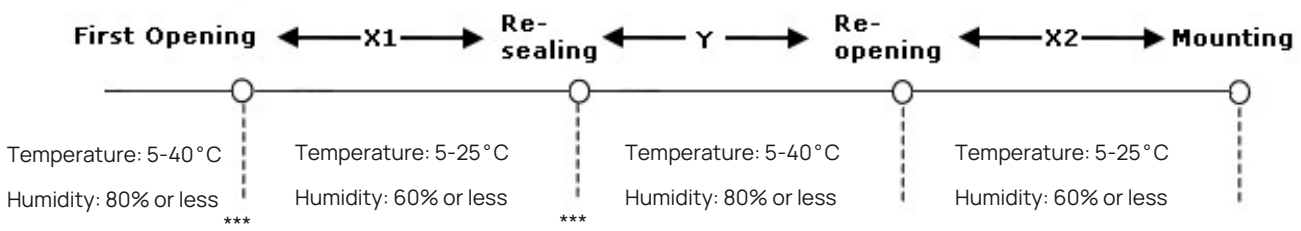
15.1.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices *once* prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

1. Storage temperature and humidity



*** - External atmosphere temperature and humidity of the dry packing

2. Storage period

- X1+X2 – Refer to After Opening the Dry Packing storage requirements. Keep is X1+X2 within 72 hours.
- Y – Keep within two weeks or less.

15.2 Baking Conditions

Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
- Once the packaging is opened, the SiP must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <30℃ and <60% relative humidity.
- If the SiP is not mounted within 72 hours or if, when the Dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125℃ (±5℃).

15.3 Surface Mount Conditions

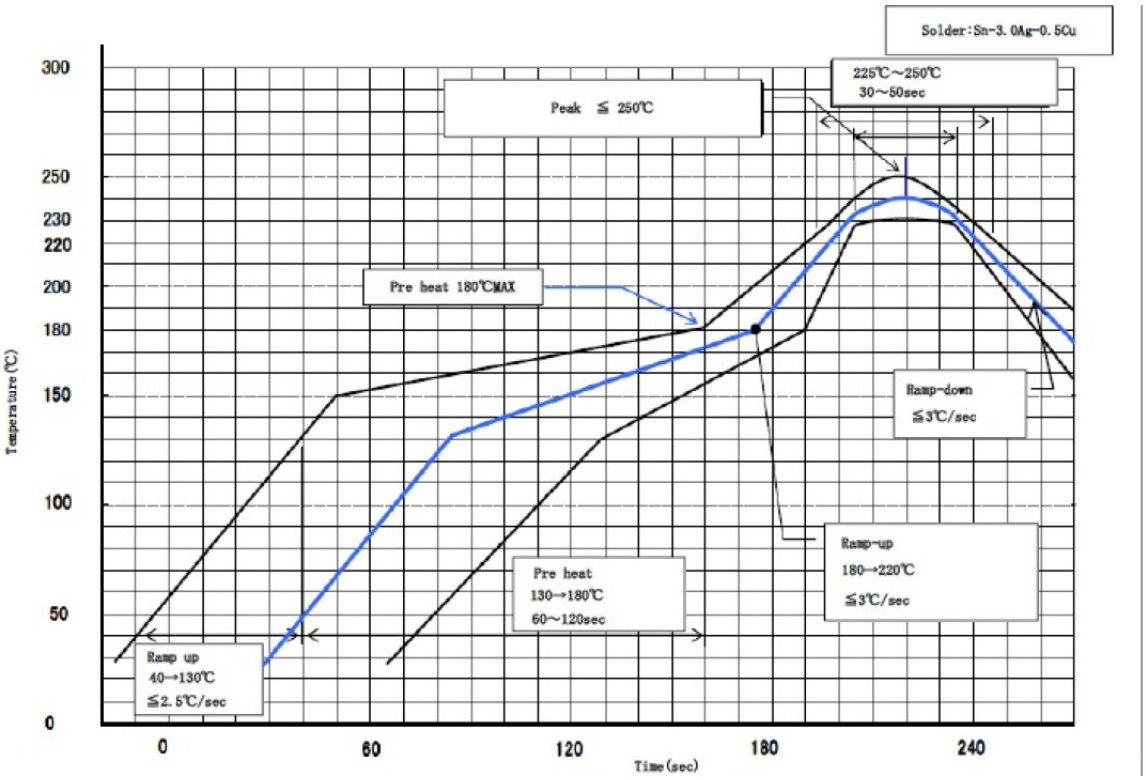
The following soldering conditions are recommended to ensure device quality.

15.3.1 Soldering

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point – IC package surface
- Temperature profile:



Ramp-up : 40 - 130 deg. Less than 2.5 deg./sec

Pre heat : 130 - 180 deg. 60 - 120 sec , 180 deg. MAX

Ramp-up : 180 - 220 deg. Less than 3 deg./sec

Peak Temperature : MAX 250 deg.

225 deg. ~ 250 deg. , 30 ~ 50 sec

Ramp-down : Less than 3 deg./sec

Figure 13: Temperature profile

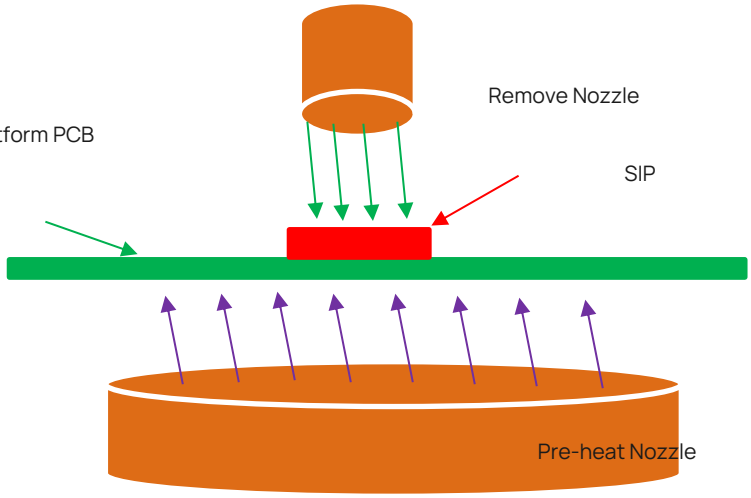
15.3.2 Cautions When Removing the SIP from the Platform for RMA

- Bake the platform before removing the SIP from the platform. Reference baking conditions.
- Remove the SIP by using a hot air gun. This process should be carried out by a skilled technician.

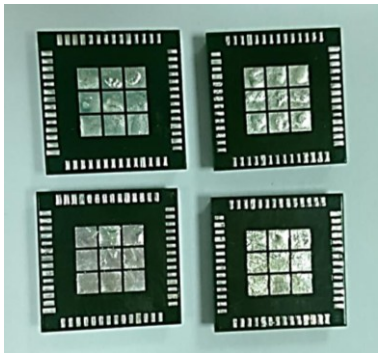
Suggestion conditions:

- One-side component platform:
  - Set the hot plate at 280 °C.
  - Put the platform on the hot plate for 8~10 seconds.
  - Remove the SIP from platform.

- Two-side components platform:
  - Use two hot air guns
  - On the bottom side, use a pre-heated nozzle (temperature setting of 200~250 °C) at a suitable distance from the platform PCB.
  - On the top side, apply a remove nozzle (temperature setting of 330 °C). Heat the SIP until it can be removed from platform PCB.

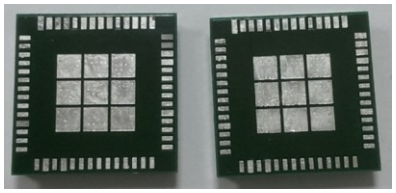


- Remove the residue solder under the bottom side of SIP.



(Not accepted for RMA)

SIP with residue solder on the bottom



(Accepted for RMA analysis)

SIP without residue solder on the bottom

- Remove and clean the residue flux is needed.

15.3.3 Precautions for Use

- Opening/handing/removing must be done on an anti-ESD treated workbench.
  All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.

16 Regulatory

Note: For complete regulatory information, refer to the 60-SIPT Regulatory Information document which is also available from the 60-SIPT product page.

The ST60-SIPT holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-60SIPT
EU	N/A
Canada (ISED)	3147A-60SIPT
Japan (MIC)	003-170091
Korea (KC)	MSIP-CRM-LAI-60-SIPT
Australia	N/A
New Zealand	N/A

17 Ordering Information

Part Number	Description
ST60-SIPT/SU60-SIPT series	2X2 802.11 a/b/g/n/ac with Bluetooth 5.1 dual mode module.
453-00202	802.11ac + Bluetooth 5.1 60 Series hardware combined with Sterling Series Professional software
DVK-ST60-SIPT	Development Board, ST60-SIPT

18 Bluetooth SIG Qualification

18.1 Overview

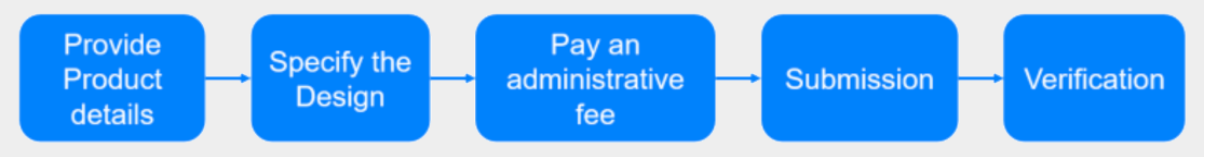
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

18.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference multiple existing designs, that have not been modified, (refer to Section 3.2.2.1 of the Qualification Program Reference Document v3).

For a Product that includes a new Design created by combining two or more unmodified designs that have DNs or QDIDs into one of the permitted combinations in Table 3.1 of the QPRDv3, a Member must also provide the following information:

- DNs or QDIDs for Designs included in the new Design
- The desired Core Configuration of the new Design (if applicable, see Table 3.1 below)
- The active TCRL Package version used for checking the applicable Core Configuration (including transport compatibility) and evaluating test requirements

Any included Design must not implement any Layers using withdrawn specification(s).

When creating a new Design using Option 2a, the Inter-Layer Dependency (ILD) between Layers included in the Design will be checked based on the latest TCRL Package version used among the included Designs.

For the purposes of this document, it is assumed that the member is combining unmodified Core-Controller Configuration and Core-Host Configuration designs, to complete a Core-Complete Configuration.

18.3 Qualification Steps When Referencing multiple existing designs, (unmodified) – Option 2a in the QPRDv3

For this qualification option, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number
    - Product Publication Date (the product publication date may not be later than 90 days after submission)

- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
- If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the multiple DNs or QDIDs used in your, (for Option 2a two or more DNs or QDIDs must be referenced)
   - Select 'I'm finished entering DN's
   - Once the DNs or QDIDs are selected they will appear on the left-hand side, indicating the layers covered by the design (should show Core-Controller and Core Host Layers covered).
   - What do you want to do next? Answer, 'Combine unmodified Designs'.
   - The Qualification Workspace Tool will indicate that a new Design will be created and what type of Core-Complete configuration is selected.
   - An active TCRL will be selected for the design.
   - Perform the Consistency Check, which should result in no inconsistencies
   - If there are any inconsistencies these will need to be resolved before proceeding
   - Save and go to Test Plan and Documentation
5. Test Plan and Documentation
   a. As no modifications have been made to the combined designs the tool should report the following message:
   'No test plan has been generated for your new Design. Test declarations and test reports do not need to be submitted. You can continue to the next step.'
   b. Save and go to Product Qualification fee
6. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
7. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
8. Download Product and Design Details (SDoC):
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:

https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

18.4 Example Design Combinations

The following gives an example of a design possible under option 2a:

Ezurio Controller Subsystem + BlueZ 5.50 Host Stack (Ezurio 60 Series based design)

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
60-SIPT/60-2230/60-SOM	Ezurio	D046328	137590	https://qualification.bluetooth.com/ListingDetails/93157
BlueZ 5.50 Host Stack	Ezurio	D046330	138224	https://qualification.bluetooth.com/ListingDetails/93911

18.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

19 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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