DVK User Guide

Veda IF91x Series

Version 1.0

Revision History

Version	Date	Notes	Contributors	Approver
1.0	22 Apr 2026	Initial Release	Andrew Chen	Andrew Chen

Contents

1 Introduction and Scope

The development kit is designed to support performance validation and software development for projects utilizing our Veda IF91x (IF912; IF913) module. This document is intended to assist manufacturers and related parties with the integration of the Veda IF91x into their host devices. Data in this document is drawn from several sources and includes information found in the Veda IF91x datasheet, Infineon CYW55913/CYW55912/CYW55911/CYW55903/CYW55902/CYW55901 datasheet rev. C , and RP2040 datasheet.

IMPORTANT: The information in this document is subject to change. Please visit the Veda IF912 and IF913 product pages for the latest information.

1.1 Purpose and Scope

The purpose of this document is to provide details regarding the setup and configuration of the Veda IF91x mounted on the development board. This document covers a description and design examples of the Veda IF91x DVK board and its features.

1.2 Related Documents

The following documents are available from the Veda IF912 and IF913 product pages:

- Veda IF912 Product Brief
- Veda IF913 Product Brief
- Veda IF912 Datasheet
- Veda IF913 Datasheet

1.3 Kit Contents

The product kit contains the following:

Item Number	Item Name	Quantity
453-00400-K1	Development Kit, Module, Veda IF913, SIP, Tri Band, External Memory, RF Trace Pin	1
940-00407	PCBA, Dev Board, Module, Veda IF913, SIP, Tri Band, No Embedded Memory, RF Trace Pin	1
940-00291	PCBA, M.2 2230 Daughter Board V2	1
EFB2471A3S-10MH4L	FLEXPIFA 6e, 2.4-2.5/4.9-7.125GHz, MH4L	1
133-00006	Cable, I-PEX High Speed Data, CABLINE-UM 30P AWG40 Blue, 200mm	1
133-00007	Cable, Molex Low Speed Data, FFC/FPC 45P, Pitch=0.3mm, L=203.2mm	1
131-00022	Cable, Type-C USB, 1.2m, 24awg, Black	1
131-00226	Cable, 26AWG, Jumper, Female-Female, 1P-1P, 100mm	6

2 Veda IF91x Development Kit Specifications

Table 1: Development board specifications

Characteristic	Specifications
Configuration Modes	UART
Host Interfaces	USB
Power supplies	• **5V**, which may be provided by either USB Type-C connector or an external source connected to specific pin header • **Module VBAT 3.3V**, which may be provided a specific external pin header or through USB Type-C • **Module VDDIO 3.3V**, which may be provided by a specific external pin header or through USB type-C
Antenna gain	• 1 dBi peak gain by integrated antenna variant • 2.3dBi peak gain supported by attached external antenna variant
Dimension	• 80.5mm X 70.0mm X 1.4mm • 72.5 mm x 50 mm x 14.2 mm

3 Veda IF91x Development Kit – Main Development Board

The Sona development board is a fully featured evaluation platform for the Sona IF91x module. It allows users to evaluate radio performance as well as the creation of prototypes and application-specific designs.

3.1 Key Features

Feature	Description
Radio Front End	• Integrates the complete transmit/receive RF paths including bandpass filter, diplexer, switches, reference crystal oscillator, and power manage unit (PMU) • Supports tri-band (2.4/5-7 GHz): IF913 only. • Support dual-band (2.4/5GHz): IF912 only. • Supports 20MHz channel bandwidth • Supports 1x1 WLAN/Bluetooth antenna configuration
The *Bluetooth*® word mark and logos are registered trademarks owned by Bluetooth SIG, Inc. Any use of such marks by Ezurio is under license. Other trademarks and trade names are those of their respective owners.	
	One buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the Veda IF913. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.
Pre-Calibration	RF system tested and calibrated in production
Sleep Clock	Internal low-power oscillator accuracy is only adequate for WLAN, and not for Bluetooth®, if low power for Bluetooth®Low-Energy required. External 32.768 KHz sleep clock is required for Bluetooth® Low Energy to support low power mode. The 32.768 kHz precision oscillator which meets the requirements listed following table must be used.

Parameter	LPO Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30 – 70	%
Input signal amplitude	200 – 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	› 100k	Ω
	‹ 5	pF
Clock jitter (during initial startup)	‹ 10,000	ppm

Feature	Description
Advanced WLAN	• IEEE 802.11a/b/g/n/ac/ax compliant, tri-band capable (2.4/5-7 GHz) or dual-band (2.4/5GHz). • 1x1 MIMO providing up to 143 Mbps PHY data rate for 2.4/5-7 GHz (1024-QAM modulation) • Supports 20 MHz bandwidth with optional SGI (1024-QAM modulation) • On-chip power amplifiers and low-noise amplifiers for both bands • Support wide variety of WLAN encryption: WPA2(Personal/Enterprise), WPA3 (Personal/Enterprise with 192 bit security).

Advanced Bluetooth	• Bluetooth® 5.4 (Bluetooth® Low Energy)
	  ○ Advertising Coding Selection
	  ○ Encrypted Advertising Data
	  ○ LE Generic Attribute Profile (GATT) Security Levels Characteristic
	• Bluetooth® Low Energy 5.0/5.1/5.2/5.3 features
	  ○ LE long range
	  ○ LE 2 Mbps
	  ○ LE mesh
	  ○ Advertising extensions
	• Host controller interface (HCI) using a high speed UART and PCM/I2S for audio data
	• Low power consumption improves battery life of IoT and embedded devices

4 Hardware Overview

4.1 Block Diagram

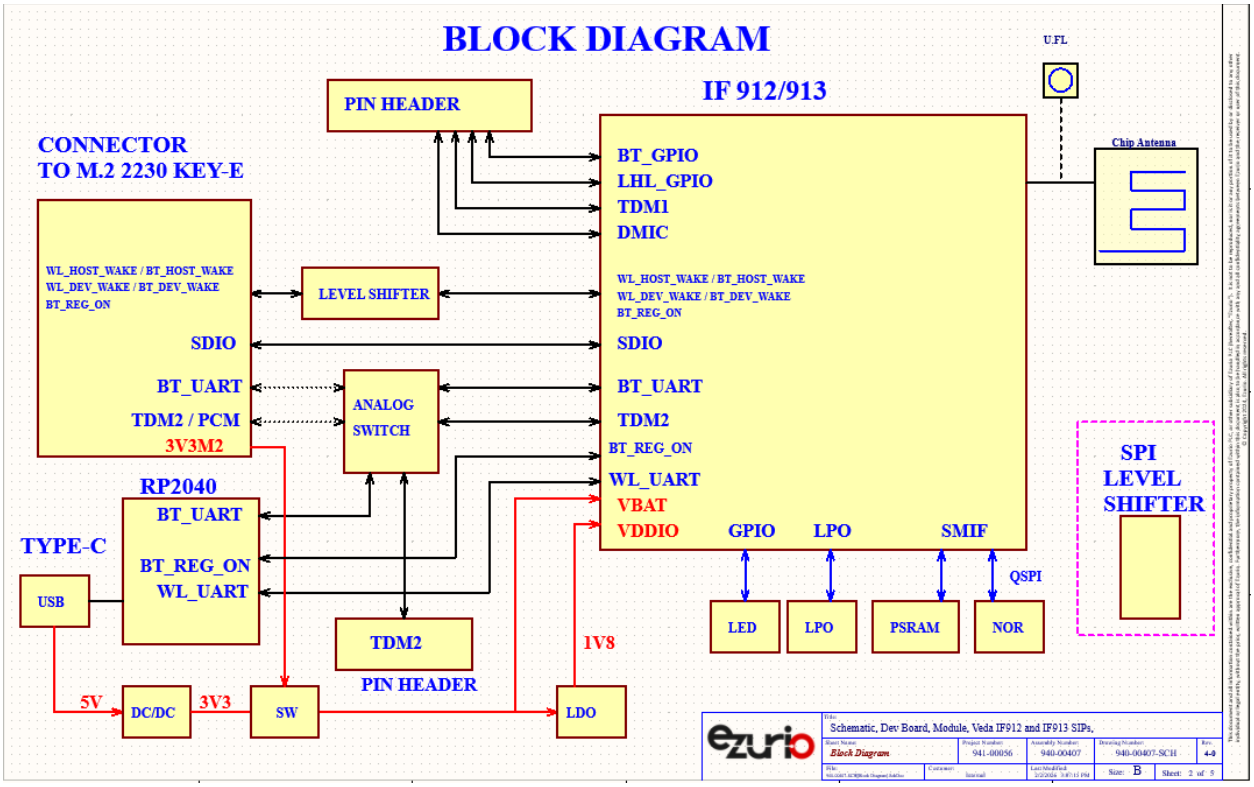


Figure 1: Block diagram of Veda IF91x DVK

5 Understanding the Development Board

This section describes each main components on the dev kit board about Veda IF912/913.

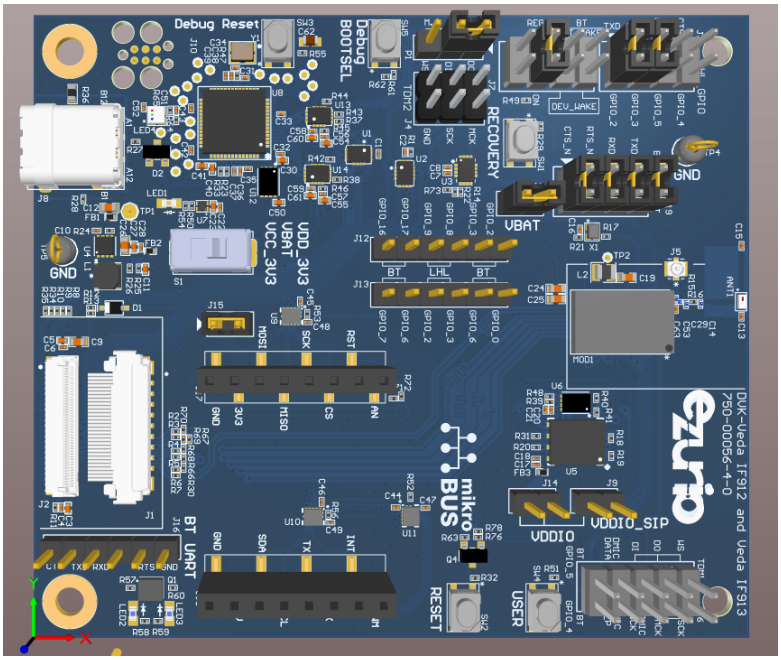
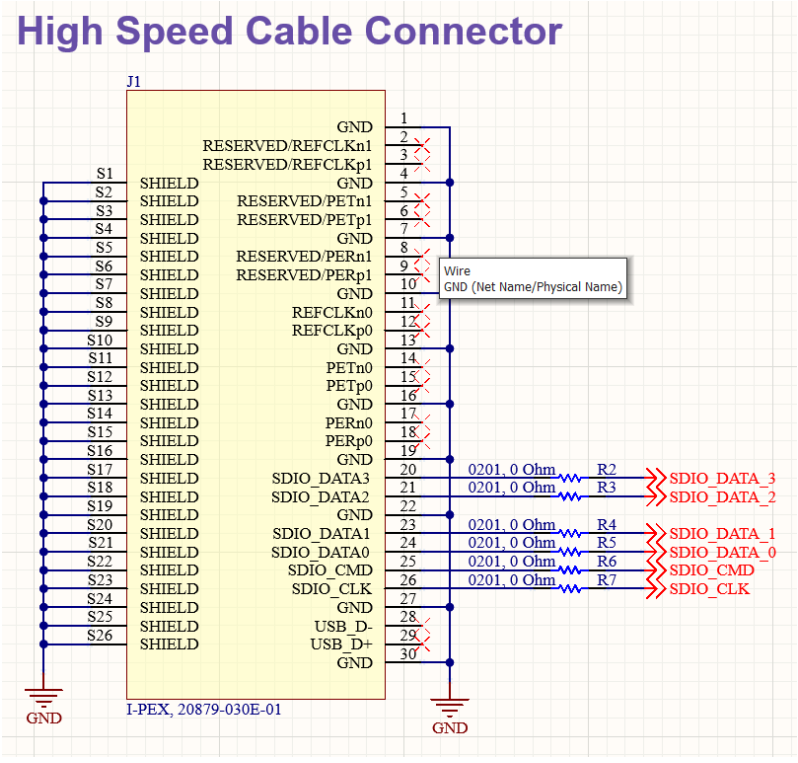
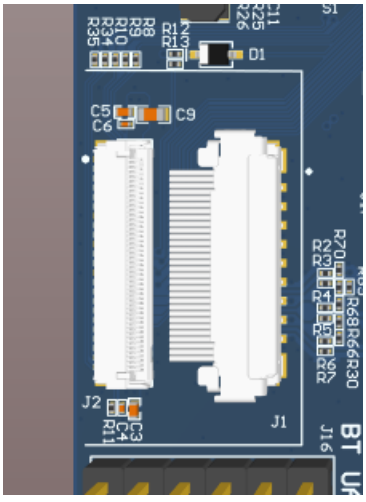


Figure 2: Picture of Veda IF91x DVK

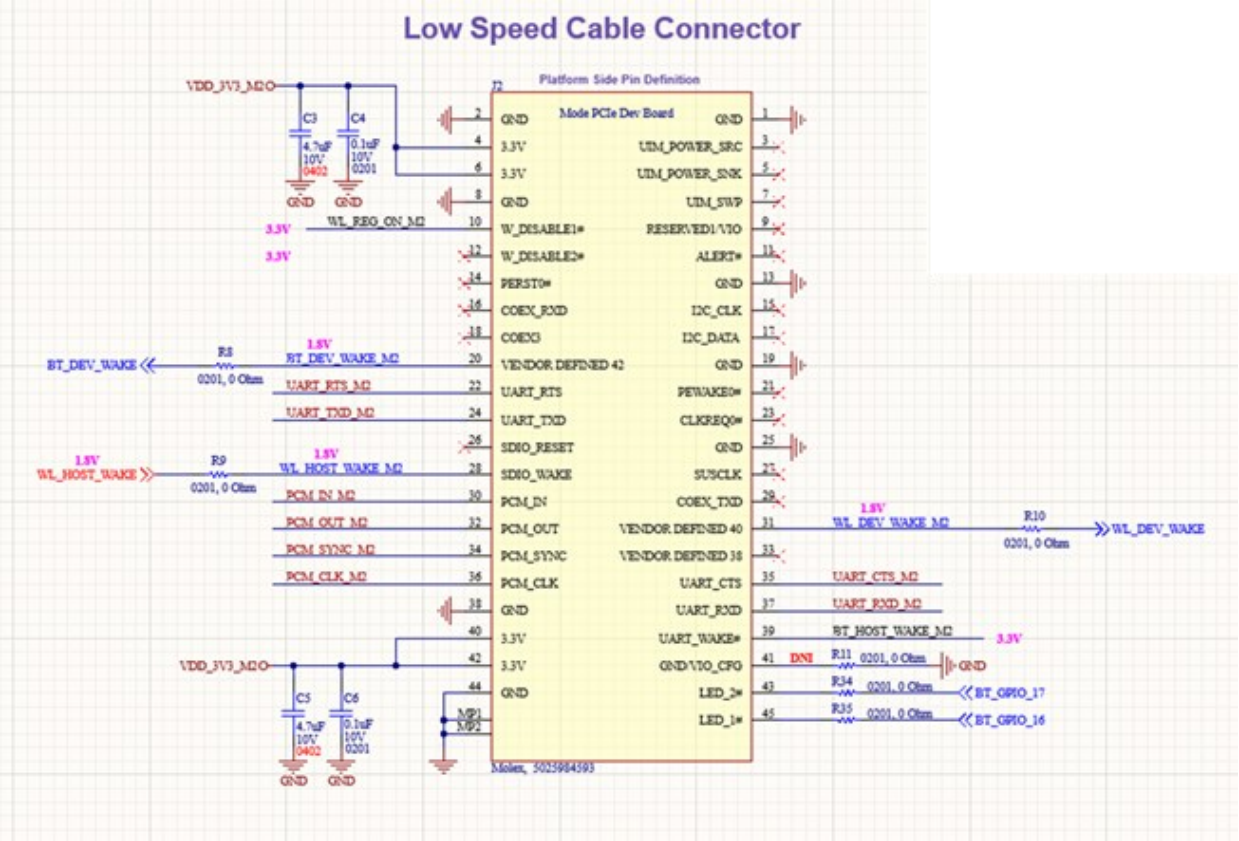
5.1 Component Description

- J1: High speed SDIO connector.





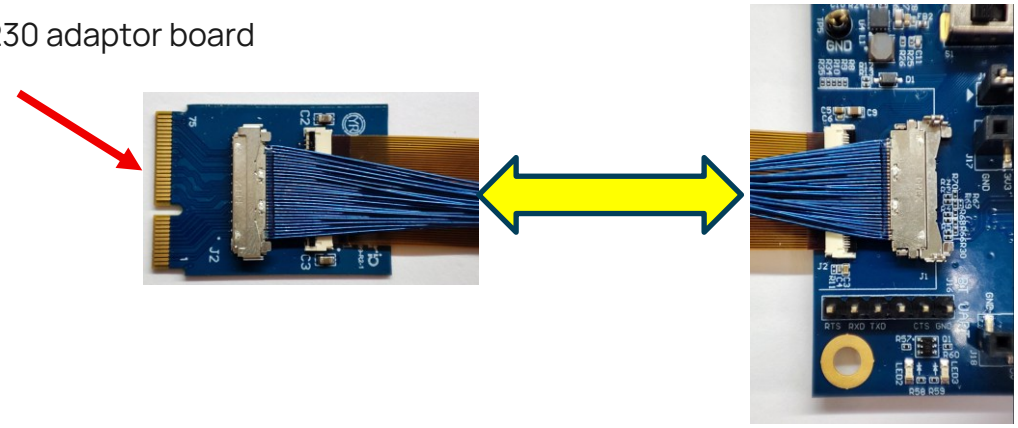
- J2: Low speed signal connector. BT UART and PCM.

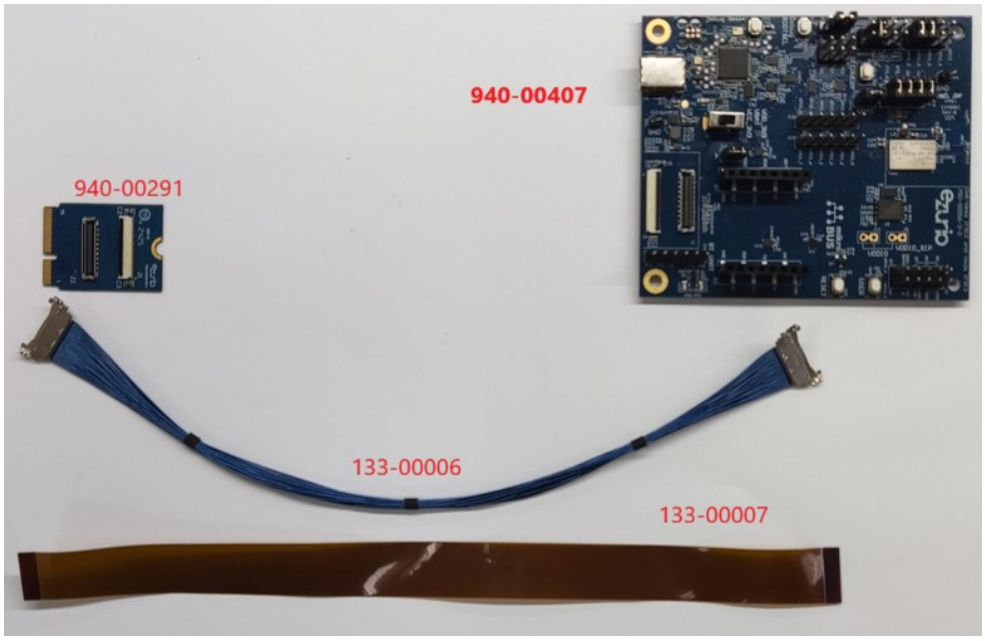


Note: J1 and J2 are used to connect to a M.2 2230 adaptor (940-00291) that allows users to connect to standard M.2 2230 E-key. Wi-Fi is running at SDIO and BT running at UART.

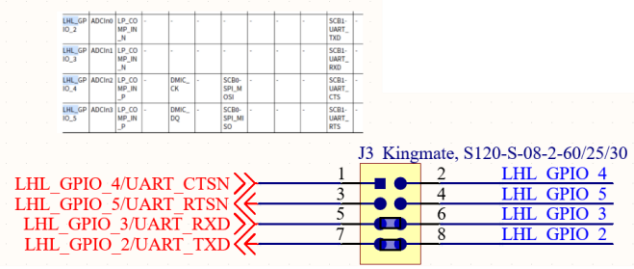
Below picture shows the detail connection of J1 and J2 to the M.2 2230 adaptor board.

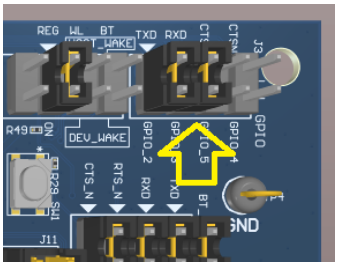
M.2 2230 adaptor board



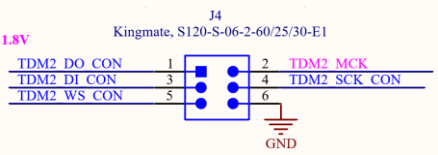


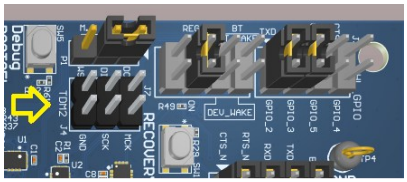
- J3: LHL_GPIO_2 to LHL_GPIO_5. Used for Wi-Fi UART at 1.8V voltage level.



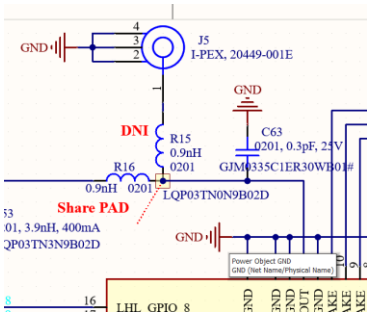


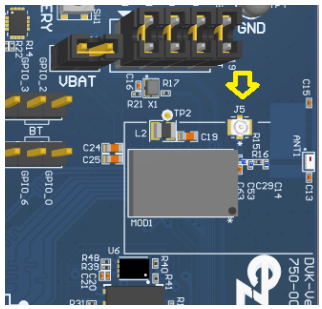
- J4: TDM2





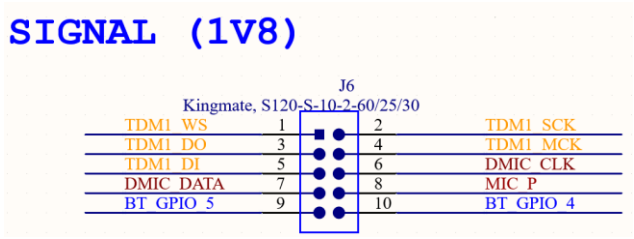
- J5: RF connector.

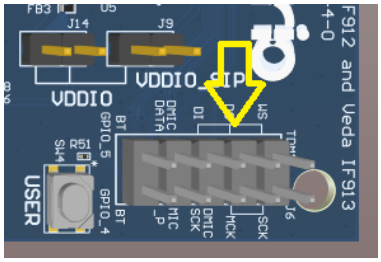




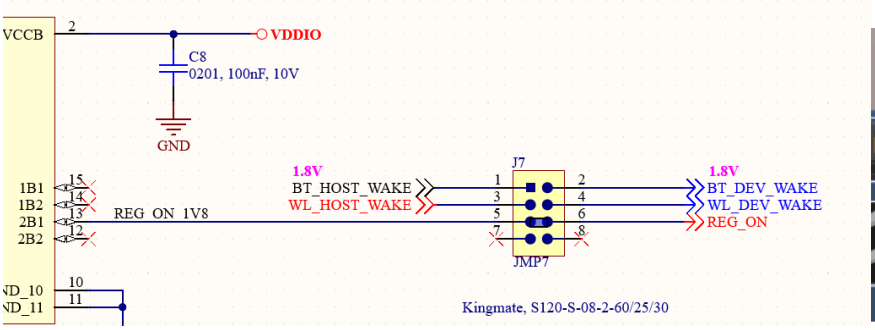
Note: in Default, the RF is connected to chip antenna on the DVK. When you measure the RF signal at J5, please move the R16 to R15 position.

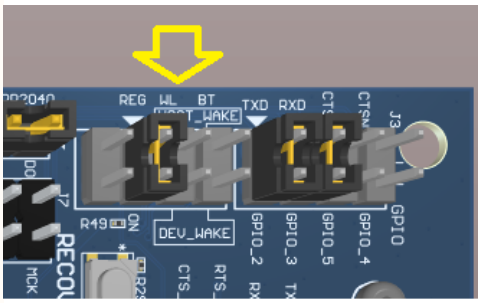
- J6: TDM1/MIC and BT GPIO. Noted: the signal level is 1.8V.



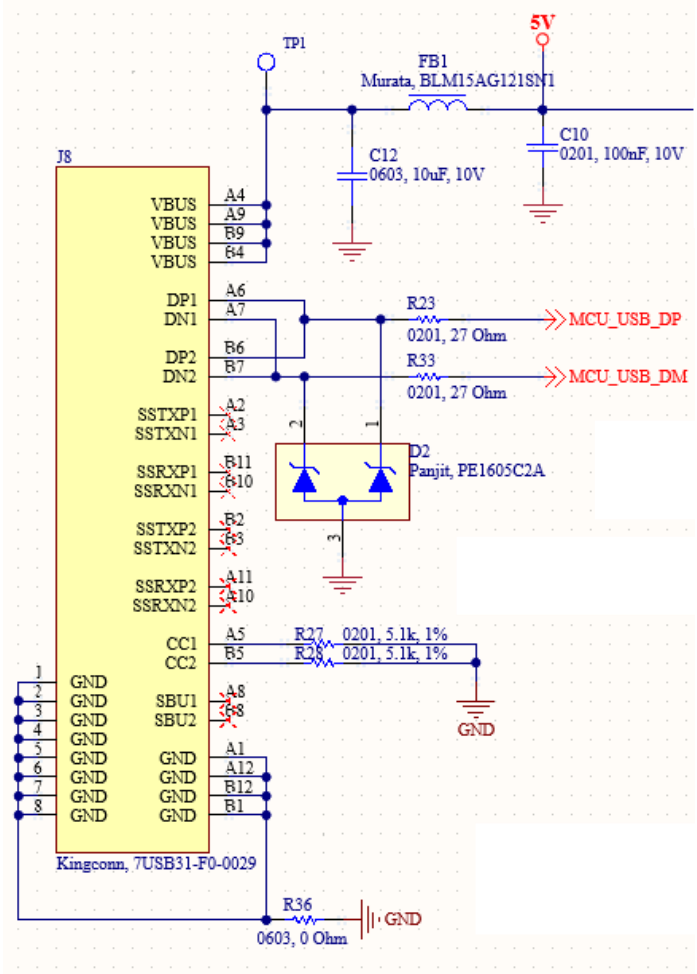


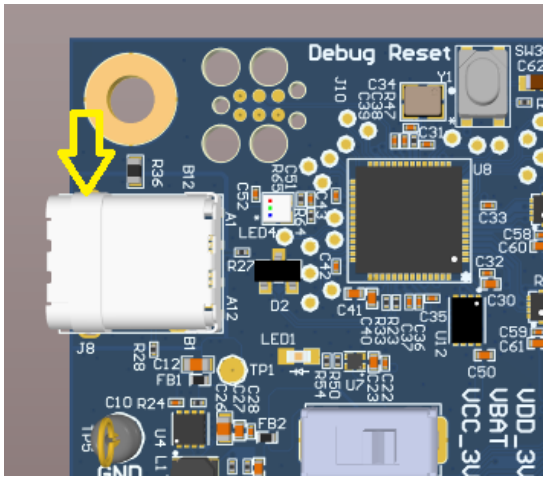
- J7: BT/WL HOST_WAKE and BT/WL DEV_WAKE signal. Noted: the signal level is 1.8V.



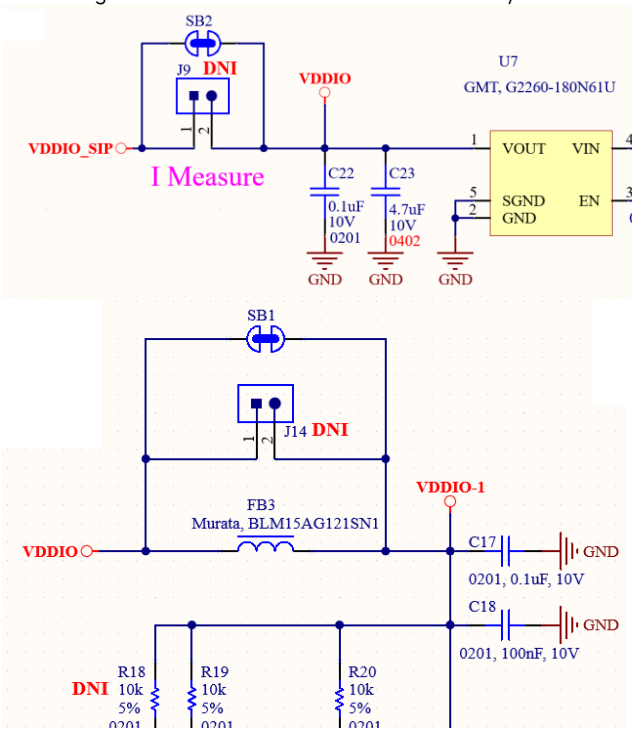


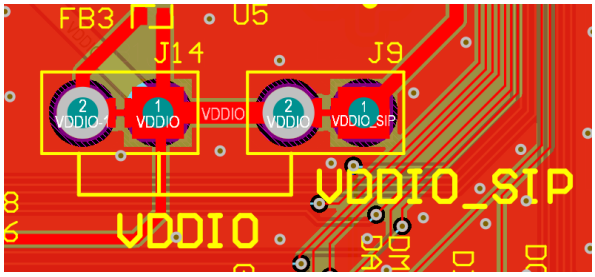
- J8: USB TYP-C connector. For providing DC power and access to the BT/WL UART port.



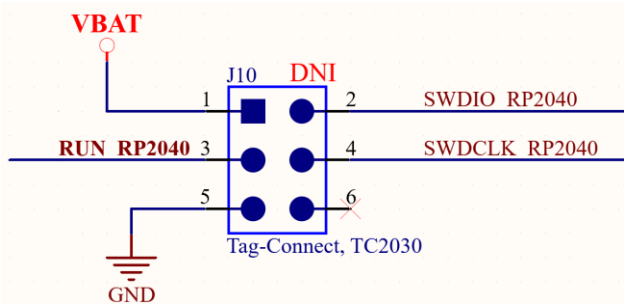


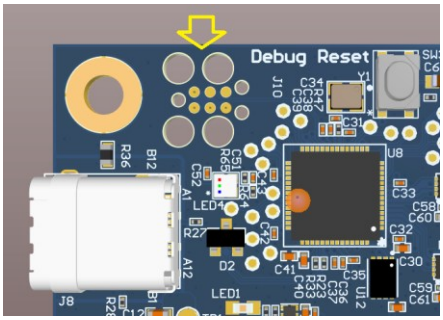
- J9/J14: Default not installed. J9 used for SIP module current measurement for VDDIO by cutting the solder bridge SB2. J14 used for measuring the current used for the external memory.



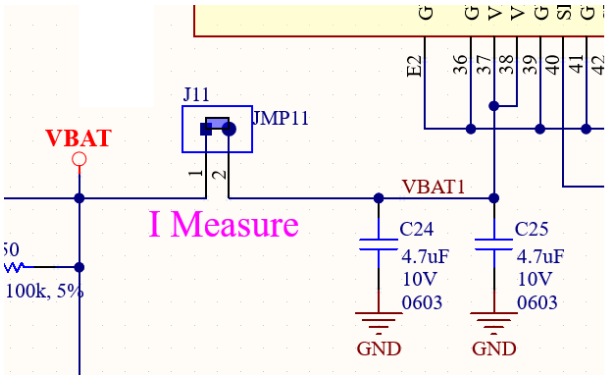


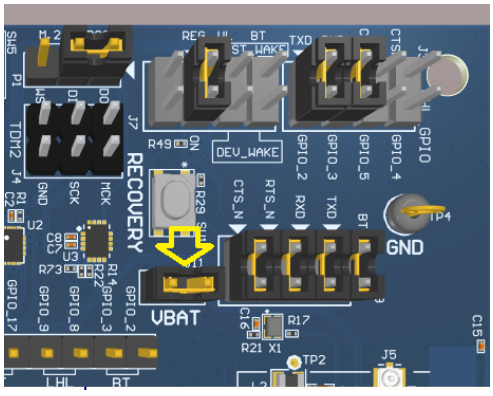
- J10: Debug port for RP2040.



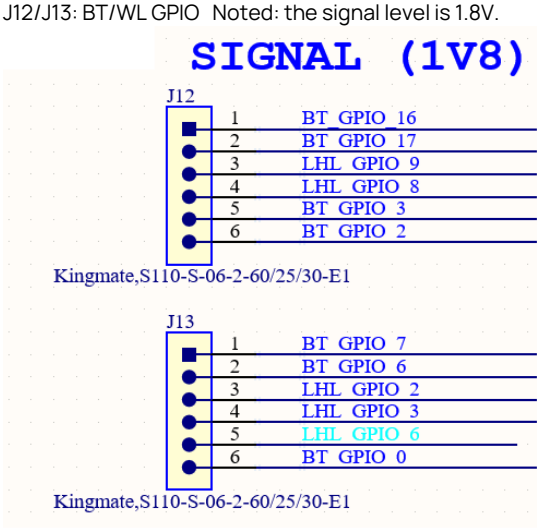


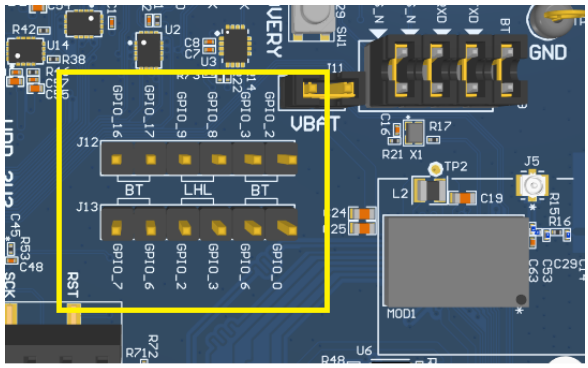
- J11: Current measurement for VBAT on the module.



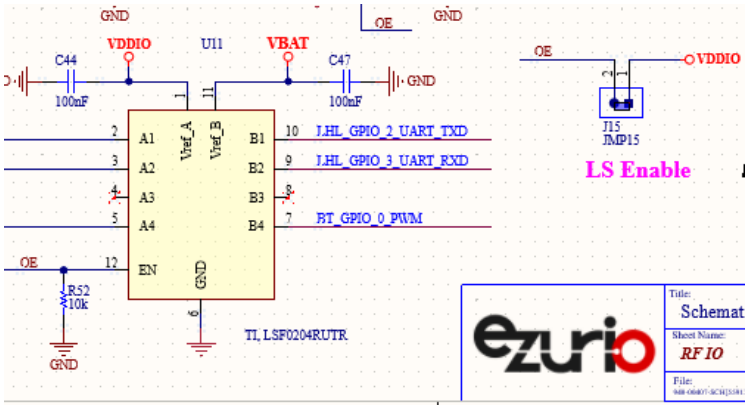


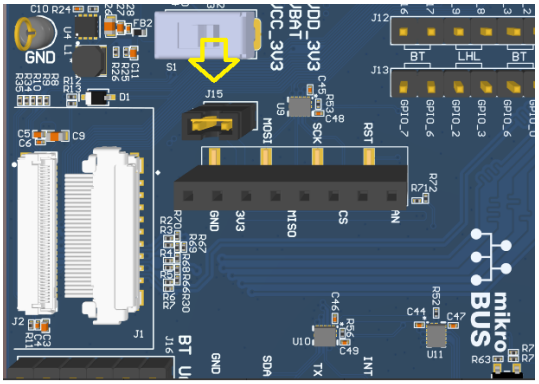
- J12/J13: BT/WL GPIO Noted: the signal level is 1.8V.



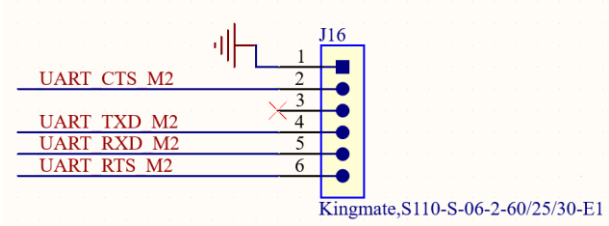


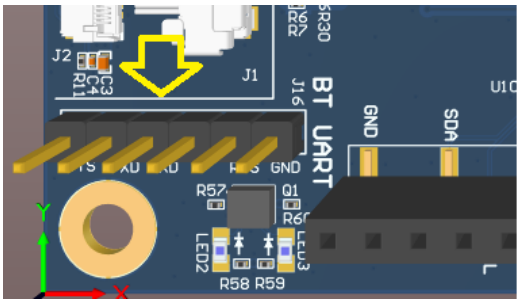
- J15: Jumper to enable the Level Shifter for Mikro-E bus J17 and J18.



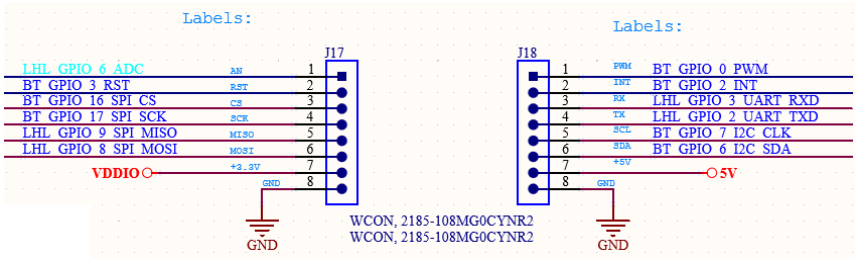


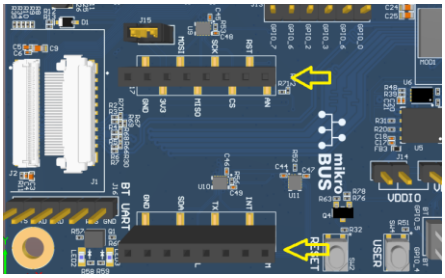
- J16: BT UART when P1 jumper is on pin2-3. Note: UART on J16 is at 3.3V voltage level.



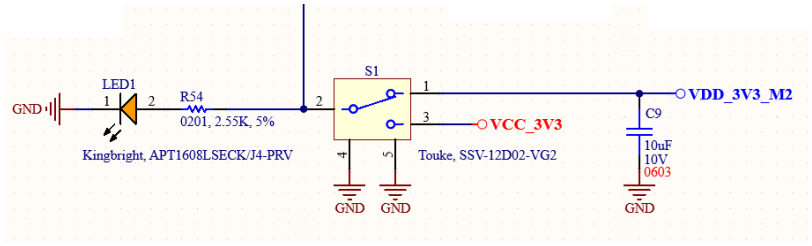


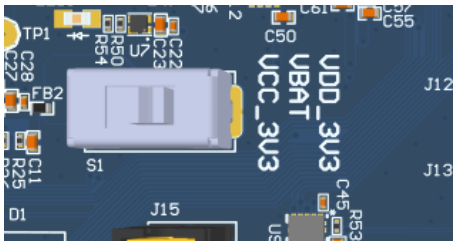
- J17/J18: Mikro E connector (3.3V). Need to place Jumper on J15 when use Mikro E bus.



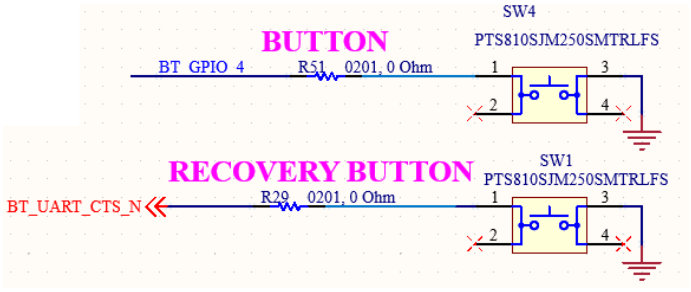


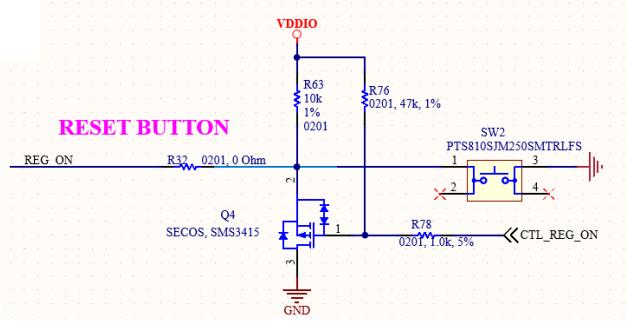
- S1: Select the VBAT power from VCC_3V3 (USB TYPE-C connector) or VDD_3V3 when using M.2 2230 adaptor board.

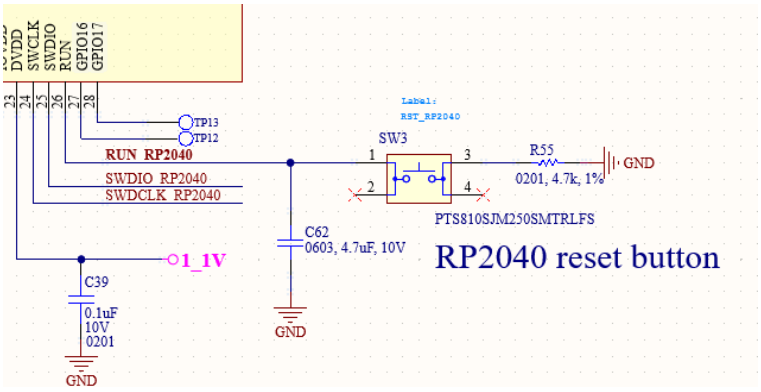


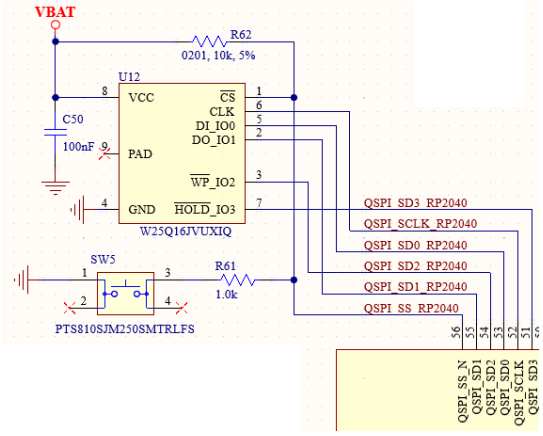


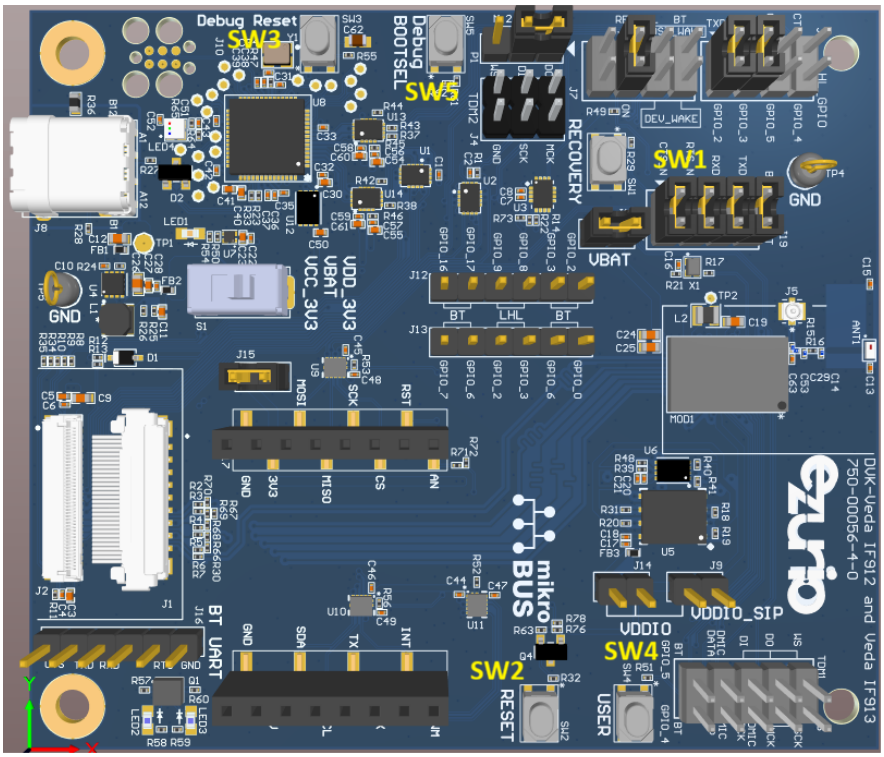
- SW1: Recovery Button.
- SW2: Reset Button.
- SW3: RP2040 (Debug) reset button.
- SW4: User Button.
- SW5: Force RP2040 (Debug) from ROM boot.



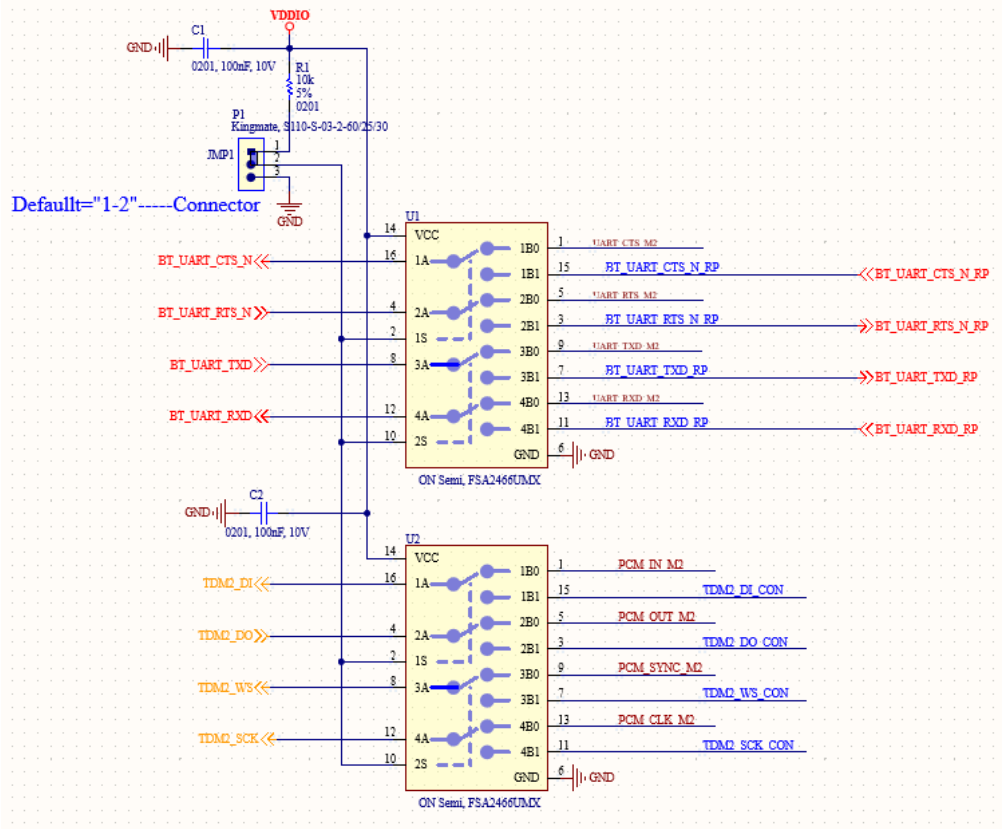


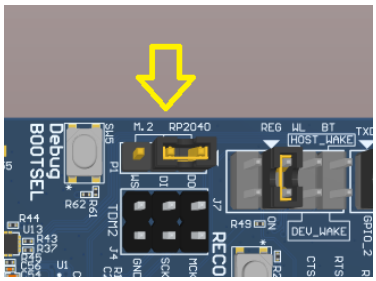






- P1: Default the jumper is set on Pin 1-2. BT UART is connected to the RP2040. And the TDM2 is connected to J4.
  When the Jumper is set on Pin 2-3, the BT UART is connected to J1 and J16. This is used for connect the bus to M.2 2230 E-key adaptor.





6 Software

Please see the Veda IF912 and IF913 product pages for links to the latest software, documentation, drawings, schematics, and more.

7 References

1. Infineon- CYW55913/CYW55912/CYW55911/CYW55903/CYW55902/CYW55901 datasheet 002-36791 Rev. *C , 2024-10-30
2. rp2040-datasheet, Raspberry Pi Ltd.

8 Additional Information

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