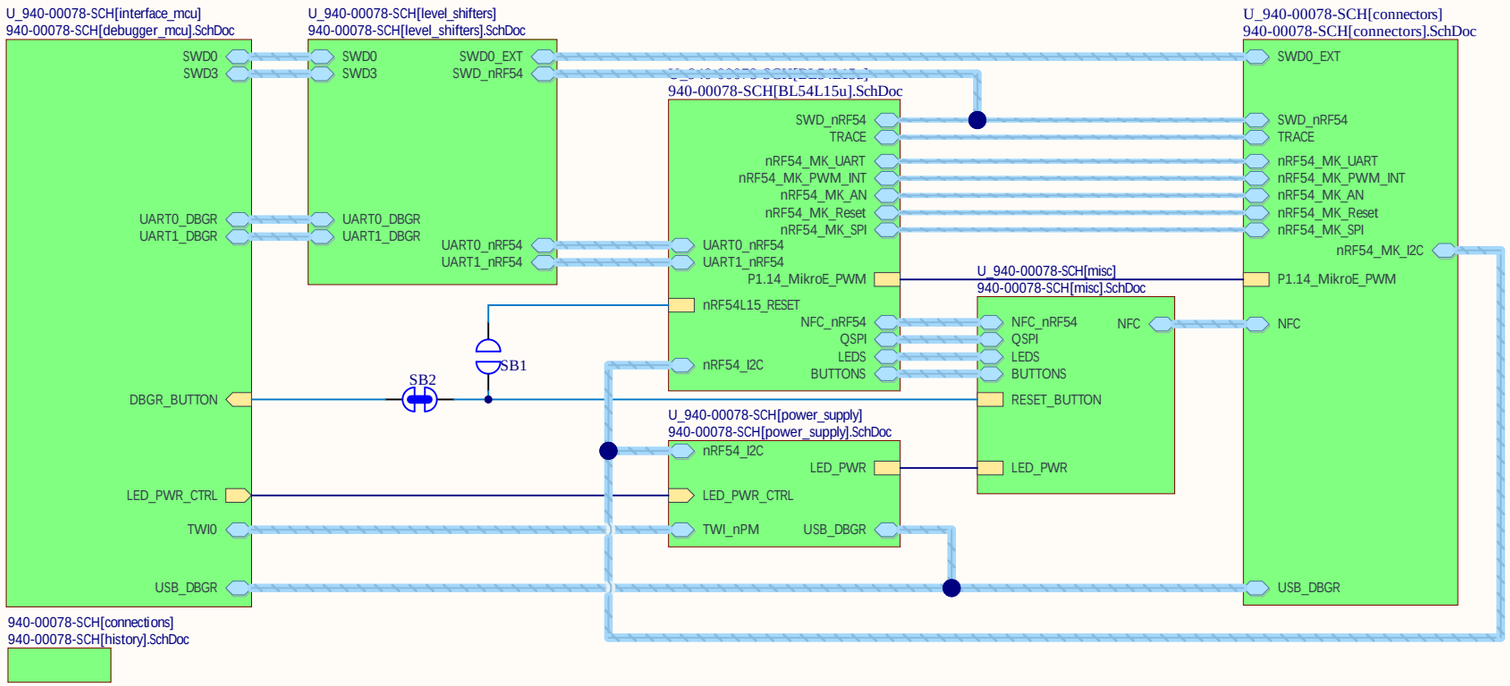
BL54L15u devboard



× The No ERC object is a design directive.
This directive is placed on a node in the circuit to suppress harmless warnings and/or error violation conditions that are detected when the schematic project is compiled.

Board fiducials

PCB1

Ezurio, 750-00032

Approvals	Date
Drawn: RK, AL	8July2024
Checked: RK, AC	25July2024
Approved: AC	25July2024

3F-1, No.145, Xianzheng 9th Rd, Zhubei City,
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Phone: +886-3-552-9695
www.ezurio.com

Title: Schematic, BL54L15u Module Dev Board, Chip Antenna

Sheet Name:	Project Number:	Assembly Number:	Drawing Number:	Rev.
connections	941-00032	940-00078	940-00078-SCH	3-1

File:	Customer:	Last Modified:	Size:	Sheet:
940-00078-SCH[connections].SchDoc	Internal	5/26/2026 PM 03:15:19	B	1 of 8

DATE	REVISION	INITIALS	DESCRIPTION
8July2024	1.0 (EVT1)	RK, AL	EVT1 SCH (based on BL54L15 devboard DVT1 (rev2.0)).
18Sep2024	2-0 (DVT1)	RK, AL	1. Adjust the definition of module pins 1,3,4,5,7,9,11 2. Re-name P5V0 to 5V0 so U5pin1 LDO receives a voltage. 3. Updated the schematic based on Nordic's new design.
12Dec2024 25Dec2024	2-1 (DVT2)	LC, AL	1. Correct the pin4 and pin5 network names of U14 2. Change C41 to NOPOP 3. Add alternative to U12 (TI/ TCA9406YZPR) 4. Change L1 to 0 ohm (YAGEO/ RC0402FR-070RL)
19Mar2025	2-2	LC , AL	1. Change R41 and R42 to 200k/0402 (YAGEO, RC0402FR-07200KL) 2. Change U14 to TI, TXS0102DCU
29May2025	3-0 (PVT)	LC , AL	Fix mikroE SPI device coexistence issue: 1. Change U11 to TXS0102DCU 2. Change R10, R11, R12, R27 to NOPOP
26May2026	3-1	AL	This revision adds the SEGGER logo to the PCB.

Approvals		Date
Drawn:	RK, AL	8July2024
Checked:	RK, AC	25July2024
Approved:	AC	25July2024

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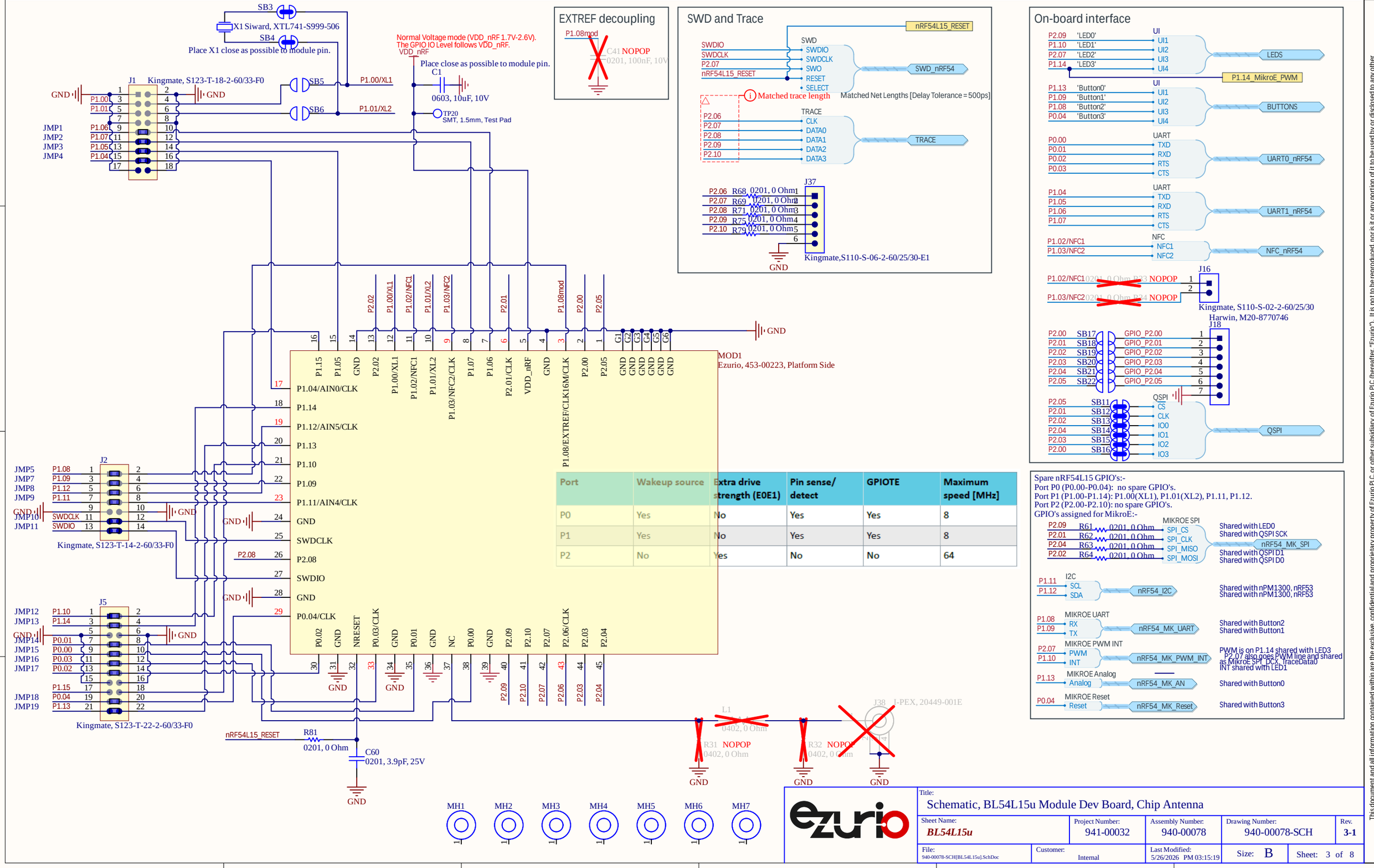
Title:
Schematic, BL54L15u Module Dev Board, Chip Antenna

Sheet Name:	Project Number:	Assembly Number:	Drawing Number:	Rev.
history	941-00032	940-00078	940-00078-SCH	**3-1**

File:	Customer:	Last Modified:	Size:	Sheet:
940-00078-SCH[history].SchDoc	Internal	5/26/2026 PM 03:15:19	B	2 of 8

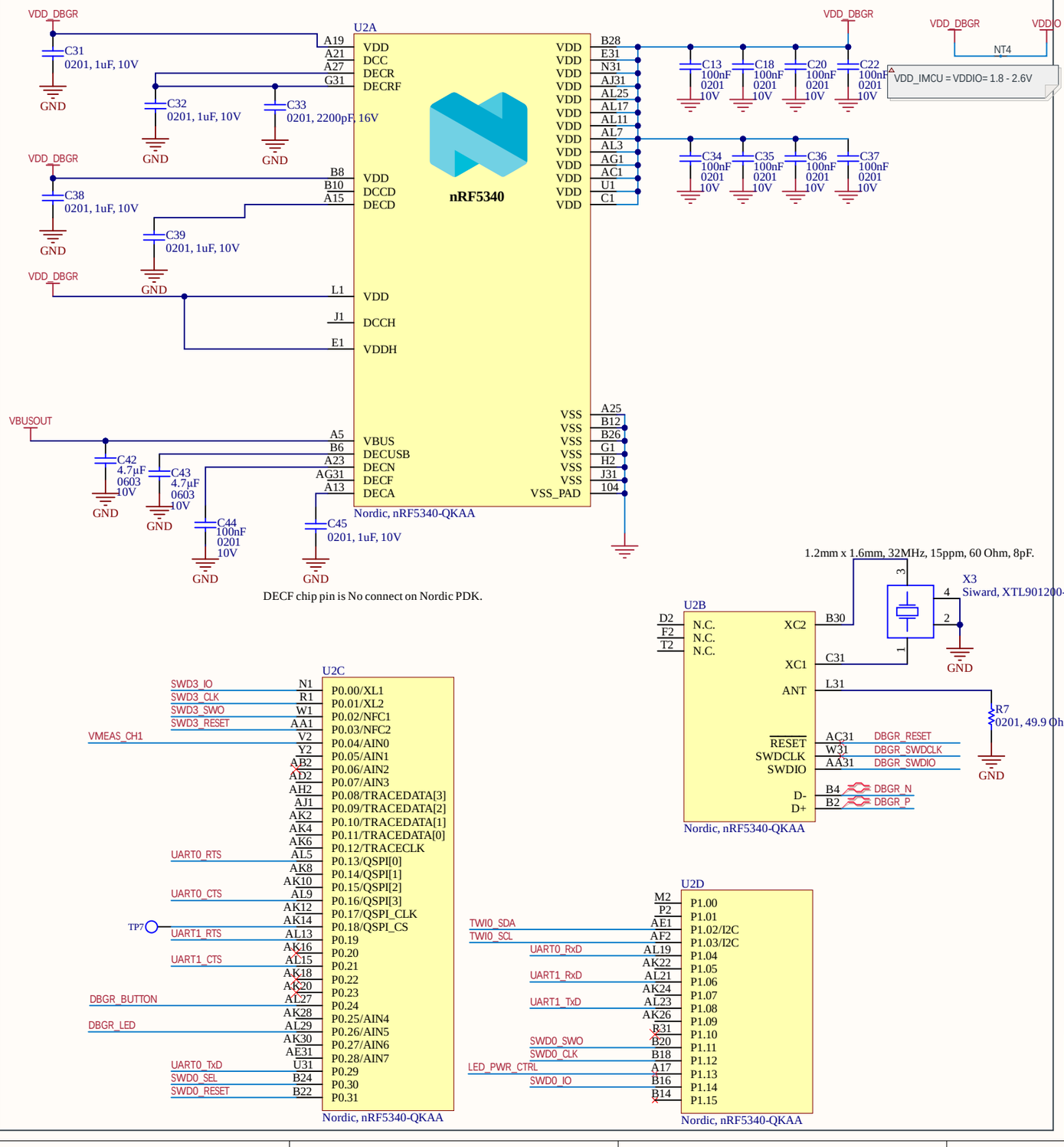


Port	Wakeup source	Extra drive strength (E0E1)	Pin sense/ detect	GPIOTE	Maximum speed [MHz]
P0	Yes	No	Yes	Yes	8
P1	Yes	No	Yes	Yes	8
P2	No	Yes	No	No	64

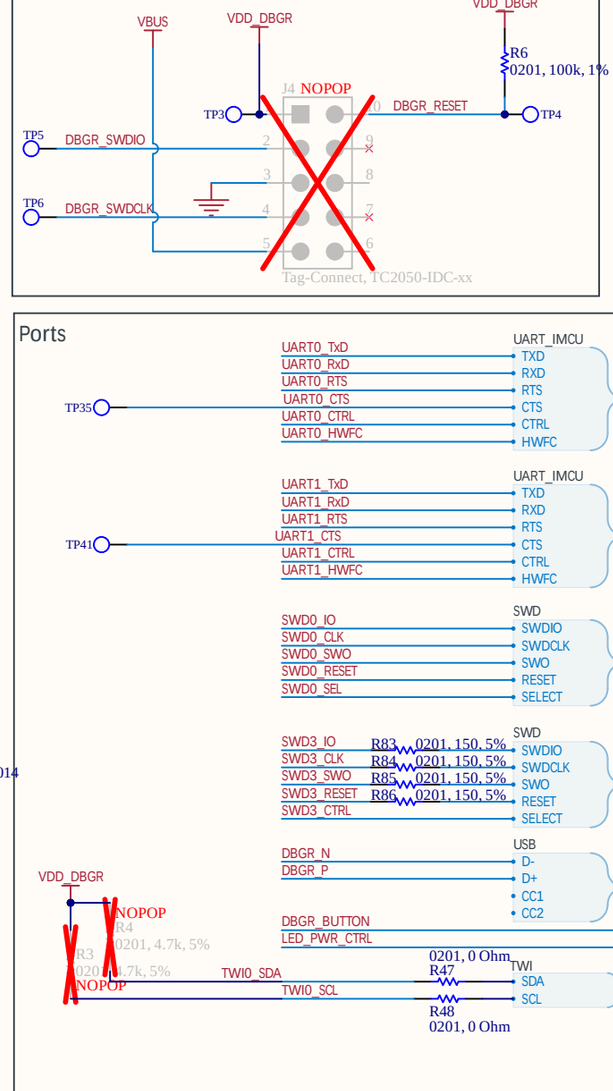
Spare nRF54L15 GPIO's:-
Port P0 (P0.00-P0.04): no spare GPIO's.
Port P1 (P1.00-P1.14): P1.00(XL1), P1.01(XL2), P1.11, P1.12.
Port P2 (P2.00-P2.10): no spare GPIO's.
GPIO's assigned for MikroE:-

Title: Schematic, BL54L15u Module Dev Board, Chip Antenna					
Sheet Name: *BL54L15u*	Project Number: 941-00032	Assembly Number: 940-00078	Drawing Number: 940-00078-SCH	Rev. 3-1	
File: 940-00078-SCH[BL54L15u].SchDoc	Customer: Internal	Last Modified: 5/26/2026 PM 03:15:19	Size: B	Sheet: 3 of 8	

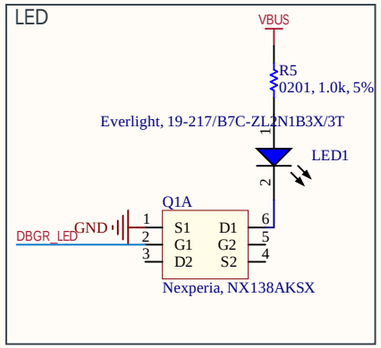
Interface MCU



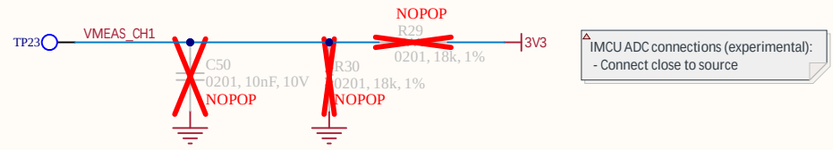
Interface MCU Programming Connector



LED

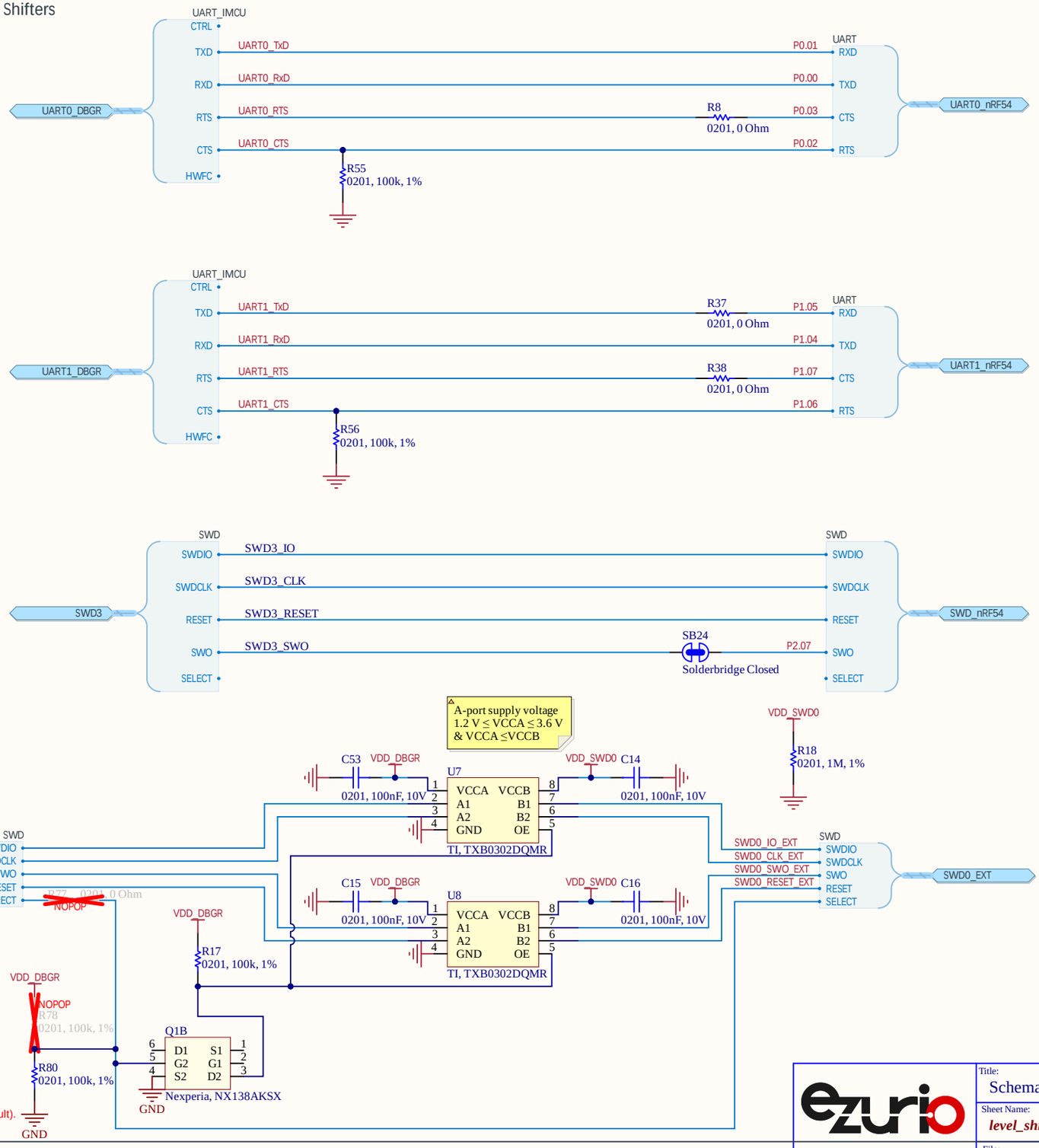


Ports



Title: Schematic, BL54L15u Module Dev Board, Chip Antenna				
Sheet Name: *debugger_mcu*	Project Number: 941-00032	Assembly Number: 940-00078	Drawing Number: 940-00078-SCH	Rev. 3-1
File: 940-00078-SCH[debugger_mcu].SchDoc	Customer: Internal	Last Modified: 5/26/2026 PM 03:15:20	Size: B	Sheet: 4 of 8

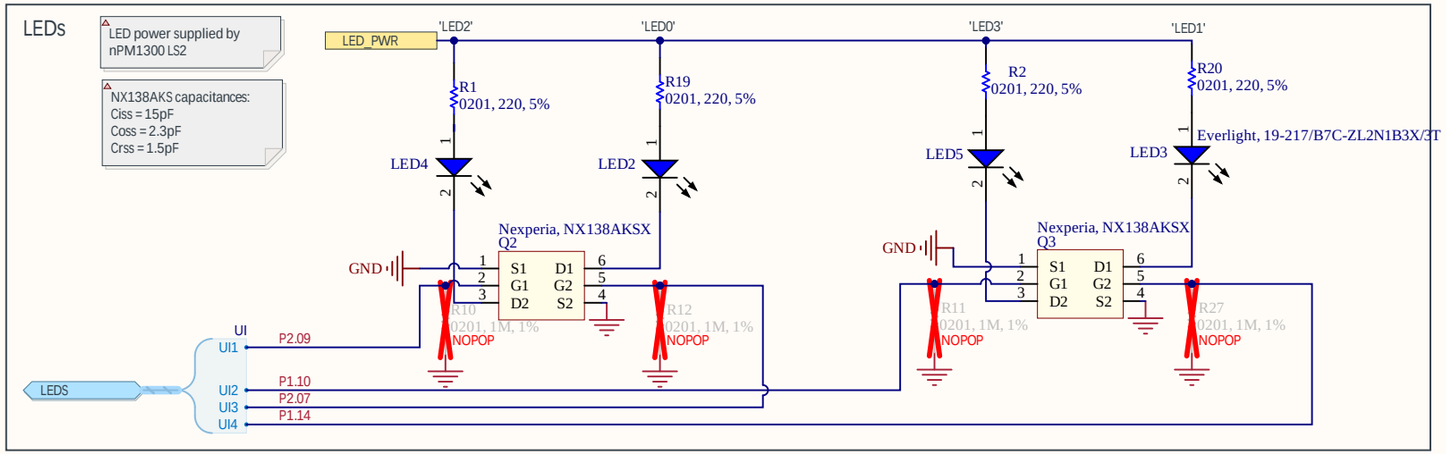
Level Shifters



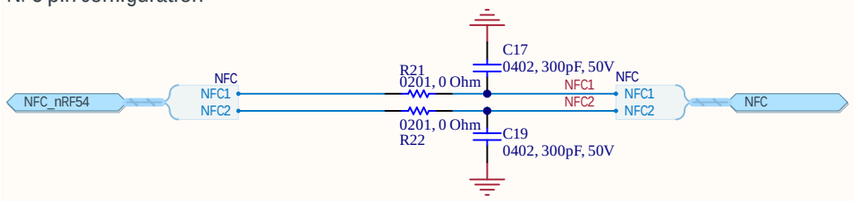
Flow controll and Interface control signal controlled IMCU

Title: Schematic, BL54L15u Module Dev Board, Chip Antenna					
Sheet Name: *level_shifters*		Project Number: 941-00032	Assembly Number: 940-00078	Drawing Number: 940-00078-SCH	Rev. 3-1
File: 940-00078-SCH[level_shifters].SchDoc	Customer: Internal	Last Modified: 5/26/2026 PM 03:15:20	Size: B	Sheet: 5 of 8	

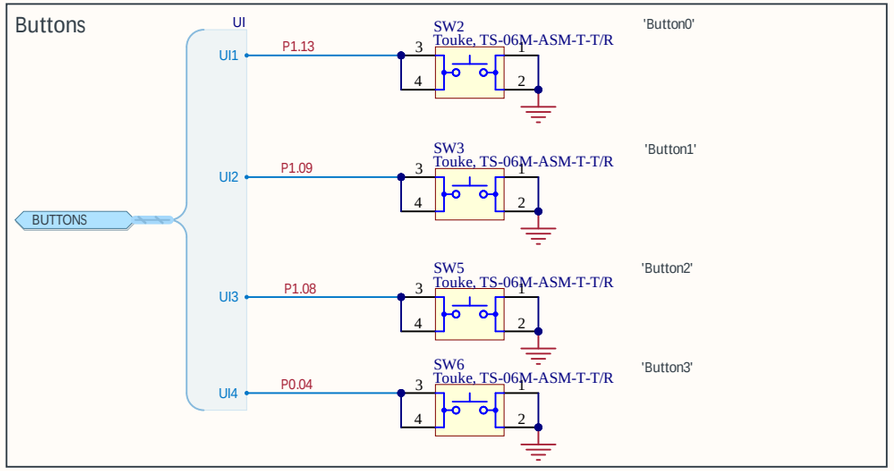
LEDs



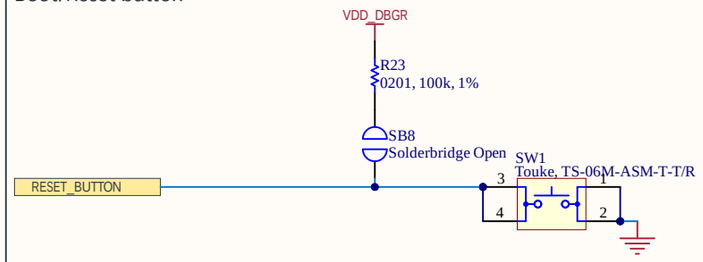
NFC pin configuration



Buttons

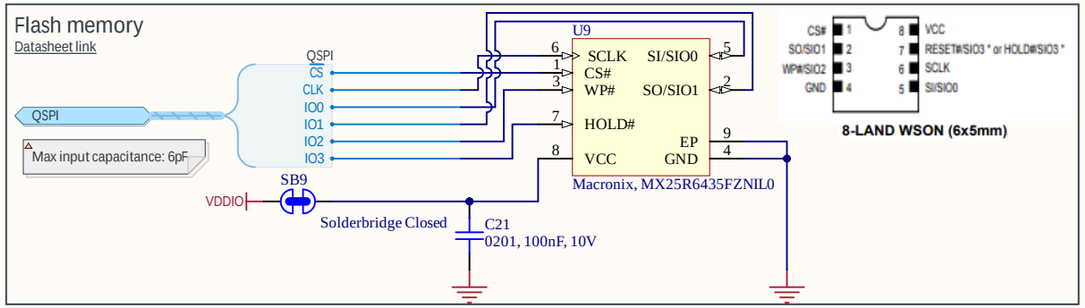


Boot/Reset button



Flash memory

Datasheet link



Title: Schematic, BL54L15u Module Dev Board, Chip Antenna

Sheet Name:	Project Number:	Assembly Number:	Drawing Number:	Rev.
misc	941-00032	940-00078	940-00078-SCH	3-1

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940-00078-SCH[misc].SchDoc	Internal	5/26/2026 PM 03:15:20	B	6 of 8

Power managment

nPM1300 settings:

- VOUT1: 1.2V - 1.8V, max 200mA
- VOUT2: 1.8V - 3.3V, max 200mA
- VOUTLDO1: 1.2V - 1.8V, max 50mA
- VOUTLDO2: 1.2V - 1.8V, max 50mA

VBUS pin supply voltage range 4.0V to 5.5V.

VBAT pin supply voltage range 2.3V to 4.45V.

R39 present to draining VSYS due to EngB/C devices bug

Power domain overview:

VDDM_nRF	Main input power for nRF54L15
VDD_nRF	Main input power for nRF54L15, 1.7V to 2.6V
VDDIO	VDD_nRF used for IO supply
VDD_DBGR	IMCU VDD tapped from VDDIO
VBUS	USB VBUS after power switch
VBUSOUT	VBUSOUT from nPM1300, used by IMCU
5V0	5V VSYS (VBUS) used for input to Buck regulators
3V3	Regulated 3.3V for LEDs

U10 — Nordic, nPM1300-QEAA

VBUS, CC1, CC2, VBAT, NTC, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, LED0, LED1, LED2, VSET1, VSET2, SHPHLD, SCL, SDA, VDDIO, VBUSOUT, VSYS, PVDD, VOUT1, SW1, PVSS1, VOUT2, SW2, PVSS2, LSIN1/VINLDO1/LSIN1, LSIN2/VINLDO2/LSIN2, LSOUT1/VOUTLDO1/LSOUT1, LSOUT2/VOUTLDO2/LSOUT2, AVSS

nPM1300

Kingmate, S113-A-03-2-60/33-F0

Molex, 0530480310

Murata, BLM15AG121SN1

Normal Voltage mode (VDD_nRF 1.7V-2.6V).

Vout1 max using Rset is 2.7V.
Vout2 max using Rset is 3.3V.

Startup VOUT1: 47k -> 1.8V
Startup VOUT2: 270k -> 3.3V*

*Eng B devices RSET2 must be 0R

Symbol	Nominal resistance	Startup output voltage, VOUT1
R_{VSET1}	<100 Ω (grounded)	0 V (OFF)
	4.7 kΩ	1.0 V
	10 kΩ	1.2 V
	22 kΩ	1.5 V
	47 kΩ	1.8 V
	68 kΩ	2.0 V
	100 kΩ	2.2 V
	150 kΩ	2.5 V
	250...500 kΩ	2.7 V

Table 18: Configuring default VOUT1 using an external resistor

Symbol	Nominal resistance	Startup output voltage, VOUT2
R_{VSET2}	<100 Ω (grounded)	0 V (OFF)
	4.7 kΩ	1.8 V
	10 kΩ	2.0 V
	22 kΩ	2.2 V
	47 kΩ	2.4 V
	68 kΩ	2.5 V
	100 kΩ	2.7 V
	150 kΩ	3.0 V
	250...500 kΩ	3.3 V

Table 19: Configuring default VOUT2 using an external resistor

Main power source:

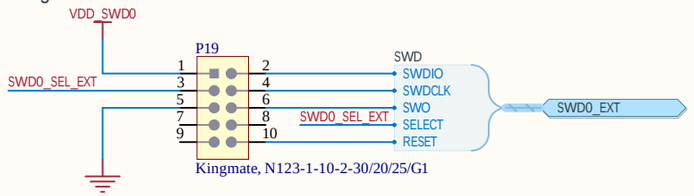
Powering nRF54L15 with nPM1300 Buck:
VOUT range:
1.0V - 3.3V @ 200mA
+-5%
5mVpp ripple
Fsw: 3.6MHz

nPM1300 settings:

- VOUT1 set to 1V8
- VOUT2 set to 3.3V
- VOUT1 and VOUT2 enable in and forced in PWM mode
- VOUT1 and VOUT2 output discharge enable

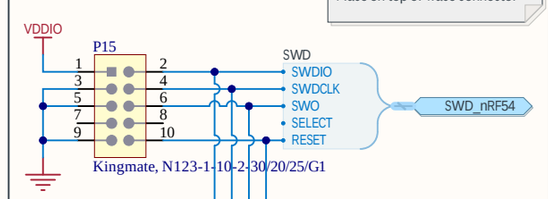
Title: Schematic, BL54L15u Module Dev Board, Chip Antenna					
Sheet Name: *power_supply*	Project Number: 941-00032	Assembly Number: 940-00078	Drawing Number: 940-00078-SCH	Rev. 3-1	
File: 940-00078-SCH[power_supply].SchDoc	Customer: Internal	Last Modified: 5/26/2026 PM 03:15:20	Size: B	Sheet: 7 of 8	

Debug OUT Connector

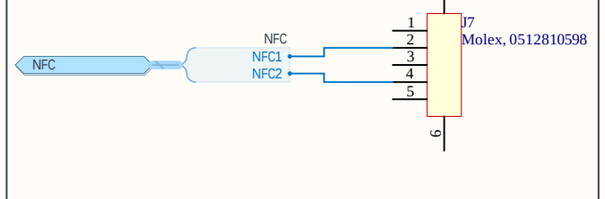


Debug IN Connector

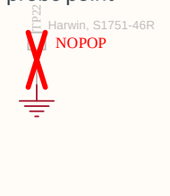
Place on top of Trace connector



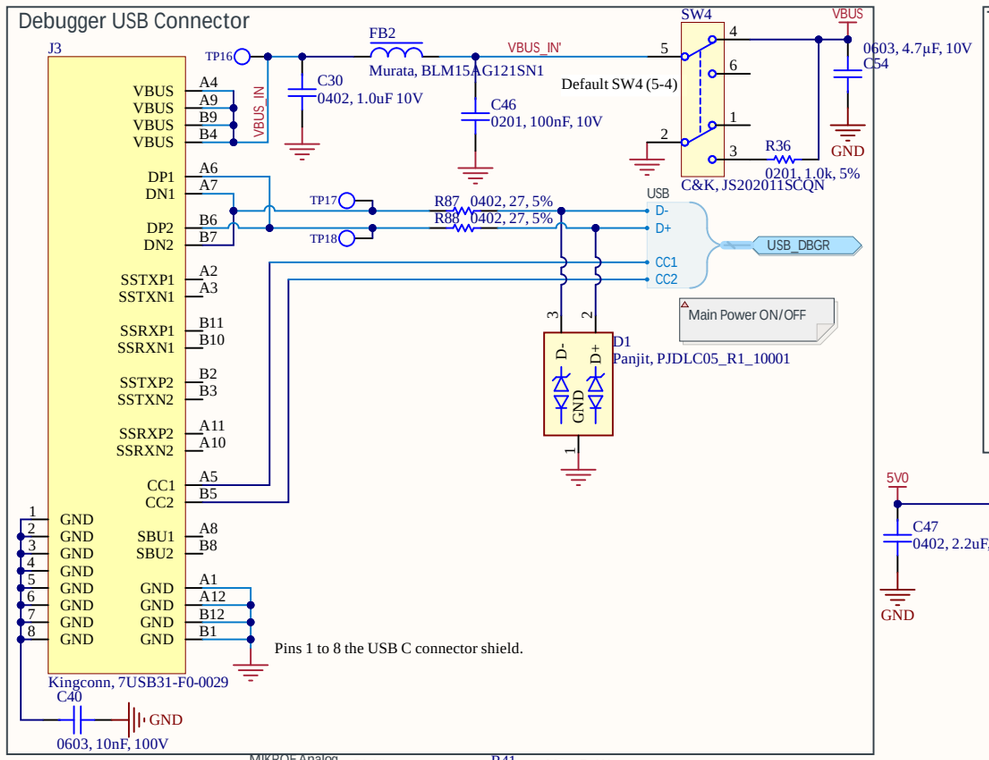
NFCT Antenna Connector



GND probe point

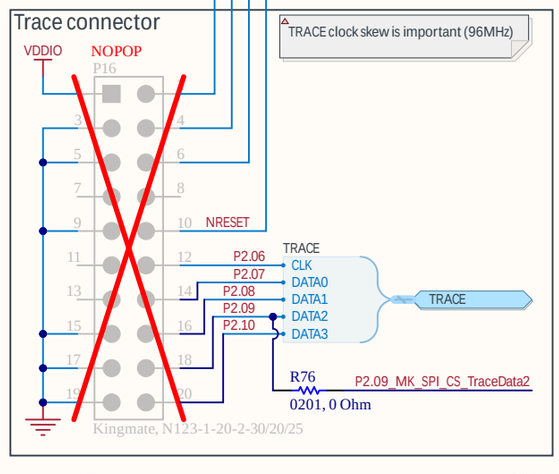


Debugger USB Connector

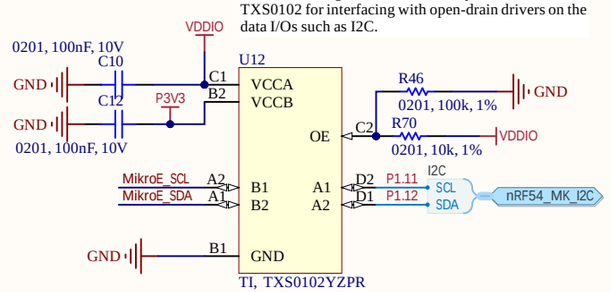


Trace connector

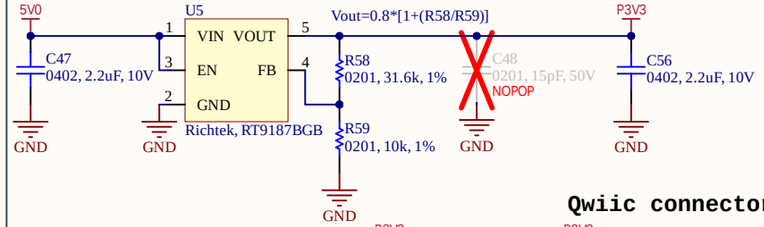
TRACE clock skew is important (96MHz)



TXS0102 device has 10-kΩ internal pullup resistors.
External pullup resistors can be added to reduce the total RC of a signal trace if necessary.
TXS0102 for interfacing with open-drain drivers on the data I/Os such as I2C.

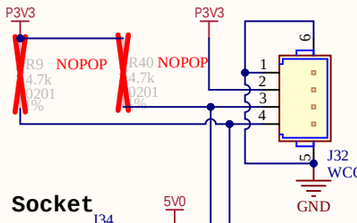


5V0 / U5

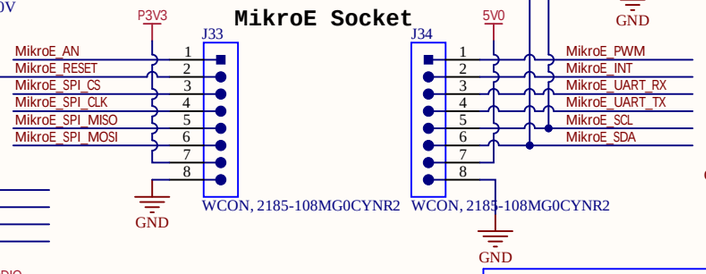


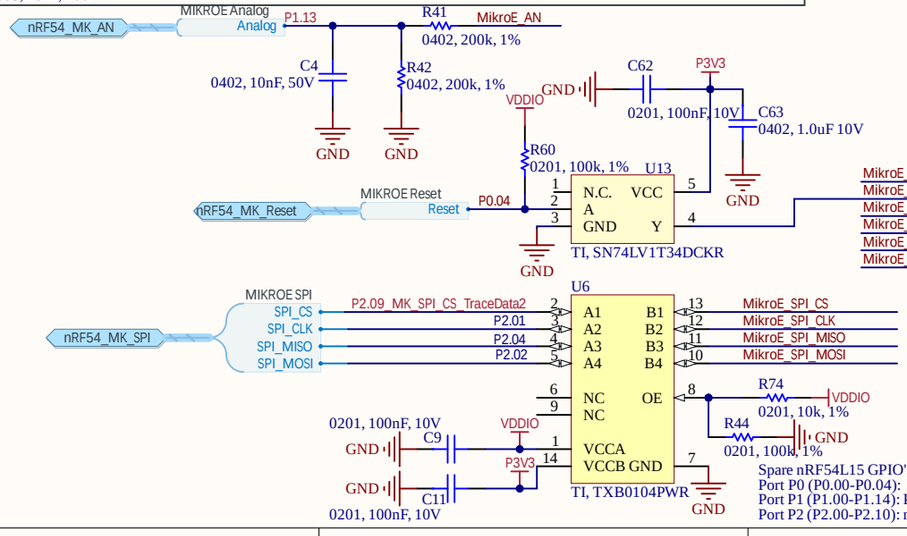
A-port supply voltage
1.2 V ≤ VCCA ≤ 3.6 V
& VCCA ≤VCCB

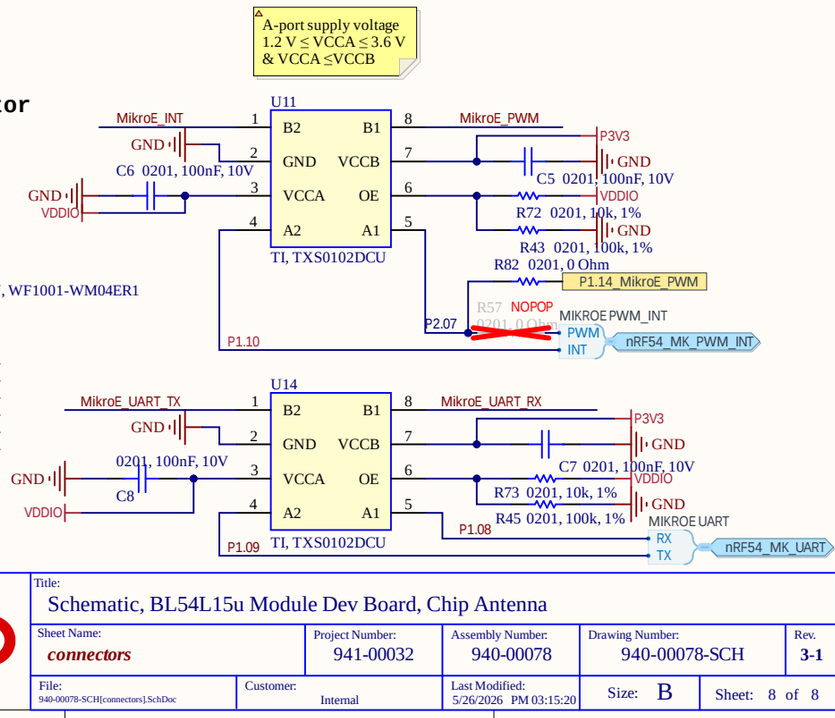
Qwiic connector



MikroE Socket







Title: Schematic, BL54L15u Module Dev Board, Chip Antenna					
Sheet Name: *connectors*		Project Number: 941-00032	Assembly Number: 940-00078	Drawing Number: 940-00078-SCH	Rev. 3-1
File: 940-00078-SCH[connectors].SchDoc	Customer: Internal		Last Modified: 5/26/2026 PM 03:15:20	Size: B	Sheet: 8 of 8