DATE	Description	Modify By
2012/8/1	Initial	Jacky_Kuo
2012/11/5	1.DEL all circuit related to WB40. 2.Page3, pull down U2 pin44 with a 10k ohm resister - R163. 3.Page4, modified Q1 to PMOS. 4.Page6, Change R96, R100, R101, R102, R104, R106, R107, R108, R110 to 1k ohm. 5.Page7, removed codec circuit and reserved a 10pins header. 6.Page7, modified net name "3V3_PCM" to "+3V3_PCM". 7.Page8, add a 3.3V supply rail for single PHY circuit. 8.Page8, added a jumper CON66 for "+3V3_ETH" rail. 9.Page8, change the U26' VIN from "+3V3" to "+5V". 10.Page8, added a jumper CON67 for "+3V3" rail. 11.Page9, fixed D24 and C151 polarity. 12.Page9, added a CON72 for test fixture power On/Off switch.	Jacky_Kuo
2012/12/5	1.Page6, change D10 footprint to correct LED type. 2.Page8, Del. Q2 & Q3	Jacky_Kuo
2012/12/20	1.Page9, change D23 symbol to meet SOD-323 footprint. 2.Page9, change CON72 to 1x3 pin header. 3.Page9, change U27 to RT7247B 4.Page2, correct J1 pin number to meet WB45 J4	Jacky_Kuo
2013/01/07	1.Page6, pull down R99 to GND for the U17 write operation. 2.Page7, change CON52 to 1x6 pin header with 2.0mm pitch. 3.Page7, change CON65 pin assignment to meet CODEC board.	Jacky_Kuo
2013/05/31	1.Page6, modifies U16 supplies rail from +3V3 to +1V8B	Jacky_Kuo
2013/06/19	1.Page8, modifies U26 VIN supplies rail from +5Vto +3V3 (For the both antenna holes which they're need to add hole ring with solder-mask layer)	Jacky_Kuo
2013/08/29	1.Page4, modified R45 and R46 to 0 ohm.	Jacky_Kuo

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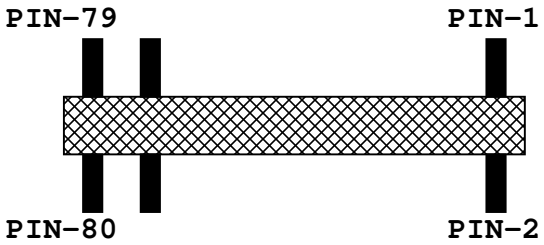
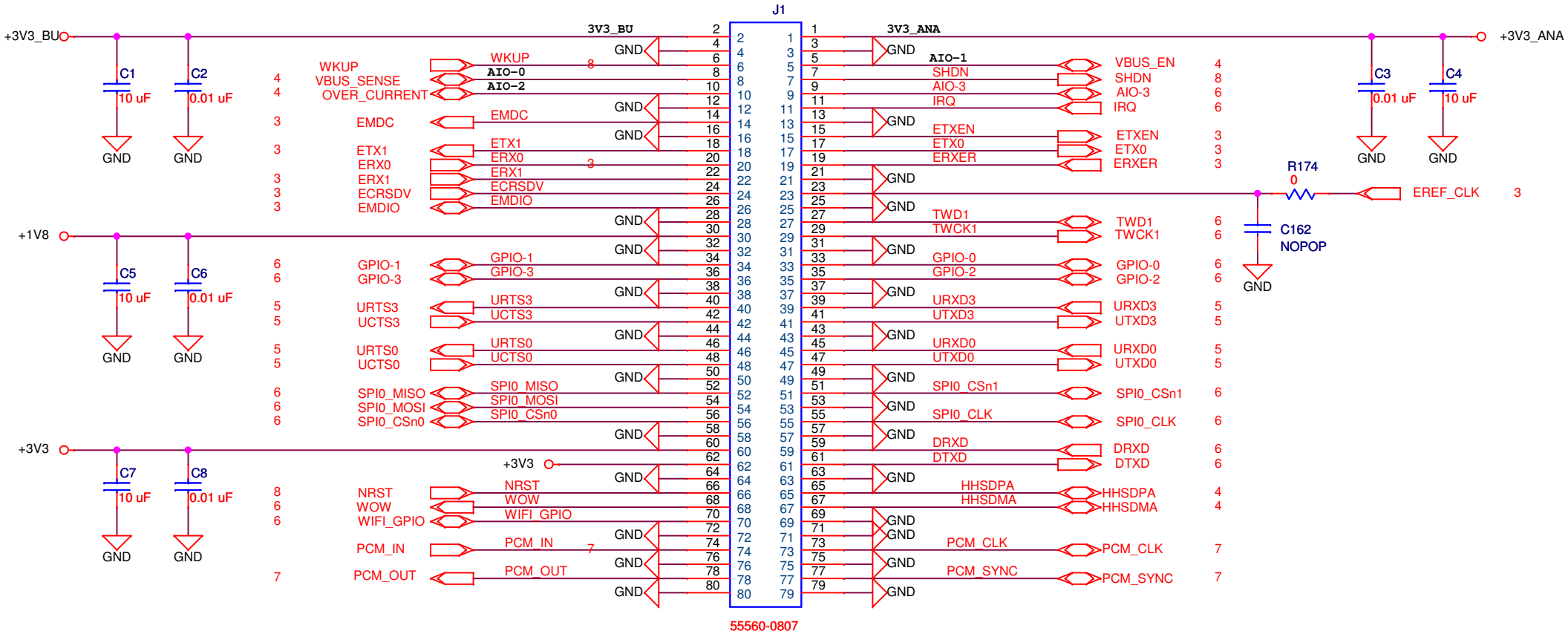
BB PCB PIN OUT (TOP VIEW)



CON3 STAND-OFF (F40M20) — GND

CON1 STAND-OFF (F40M20) — GND

CON2 STAND-OFF (F40M20) — GND



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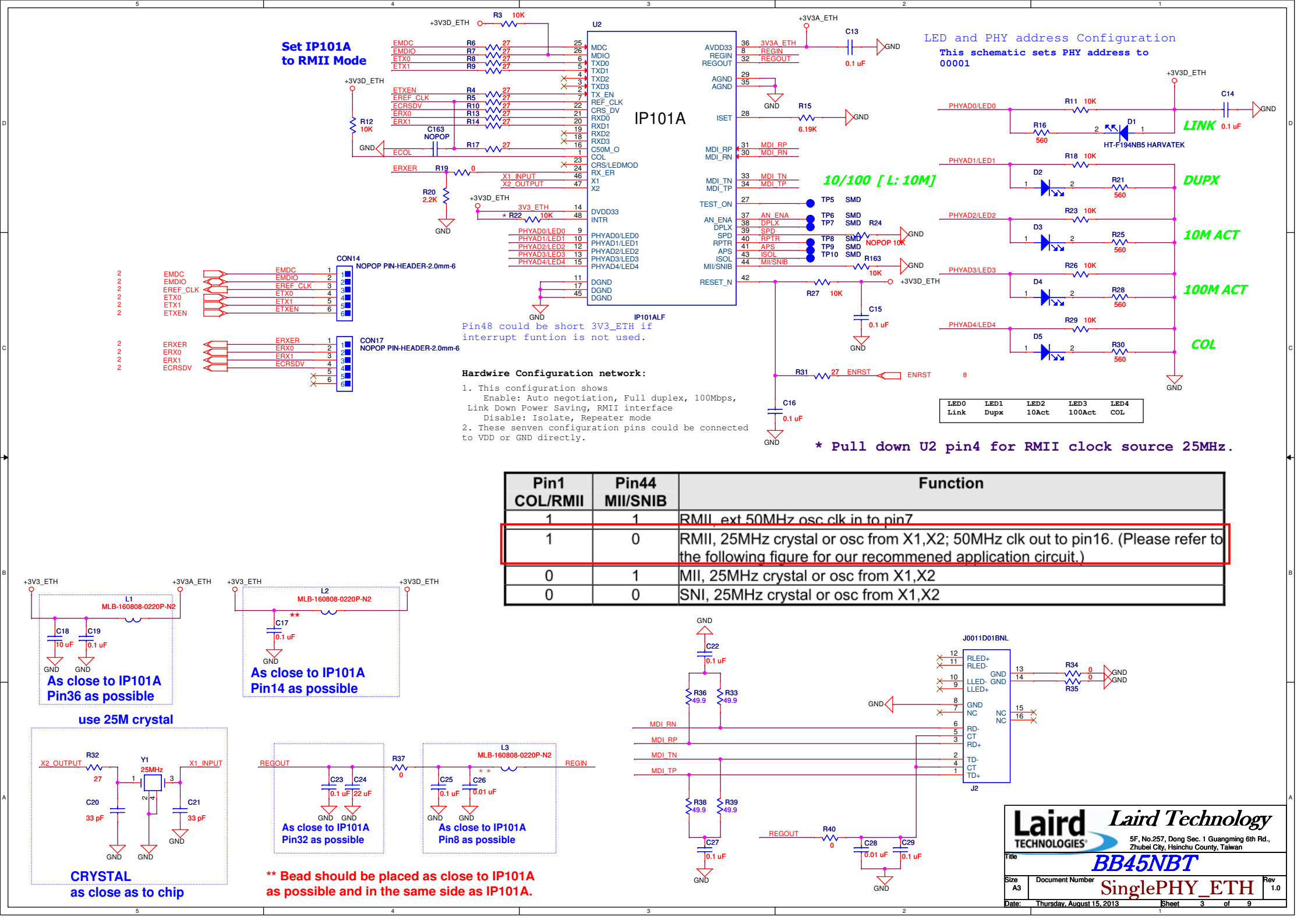

Pin1 COL/RMII	Pin44 MII/SNIB	Function
1	1	RMII, ext 50MHz osc clk in to pin7
1	0	RMII, 25MHz crystal or osc from X1,X2; 50MHz clk out to pin16. (Please refer to the following figure for our recommened application circuit.)
0	1	MII, 25MHz crystal or osc from X1,X2
0	0	SNI, 25MHz crystal or osc from X1,X2

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Size	Document Number	Rev
A3	SinglePHY_ETH	1.0

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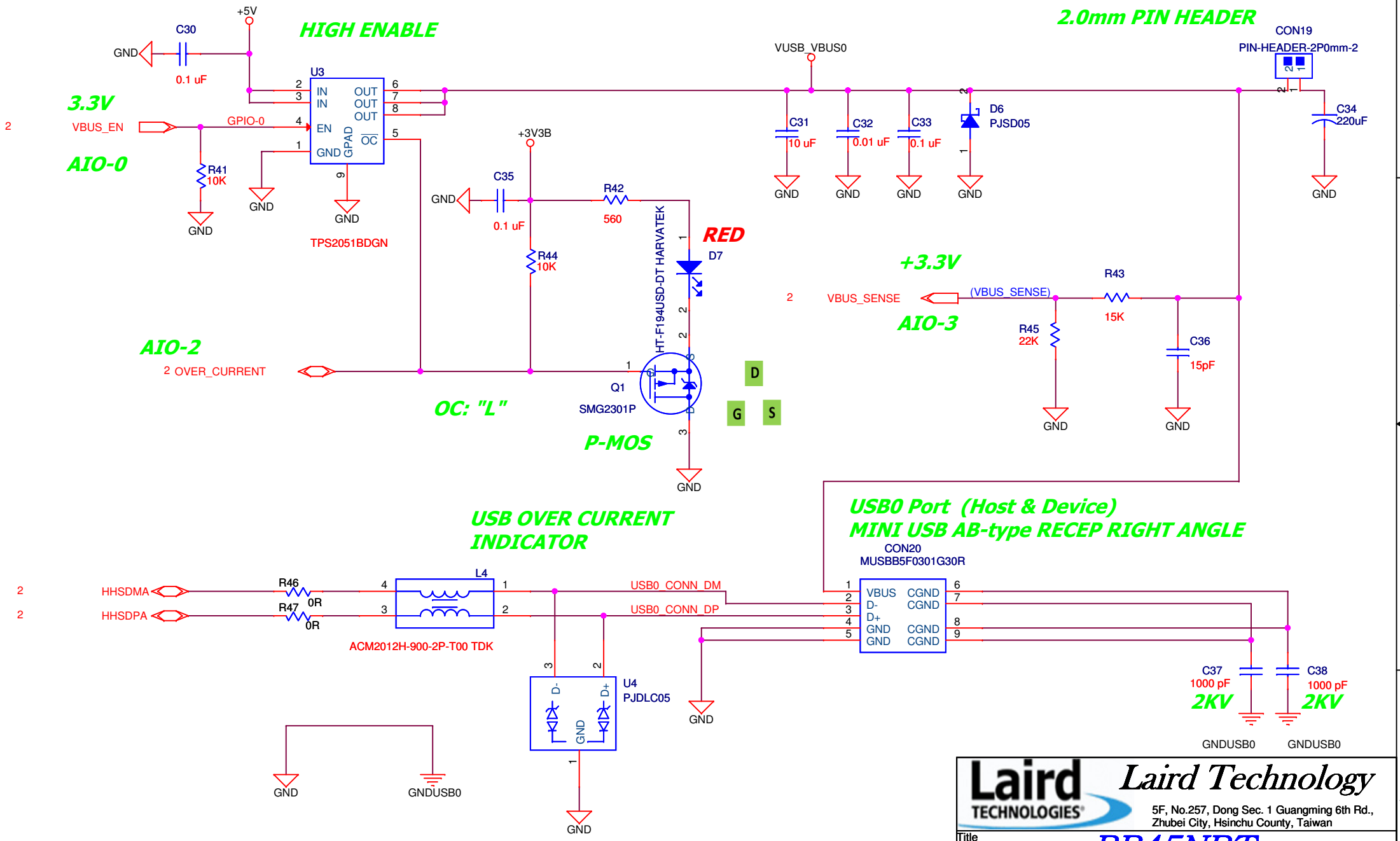

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Size	Document Number	Rev
A4	Atmel SAM-BA USB	1.0

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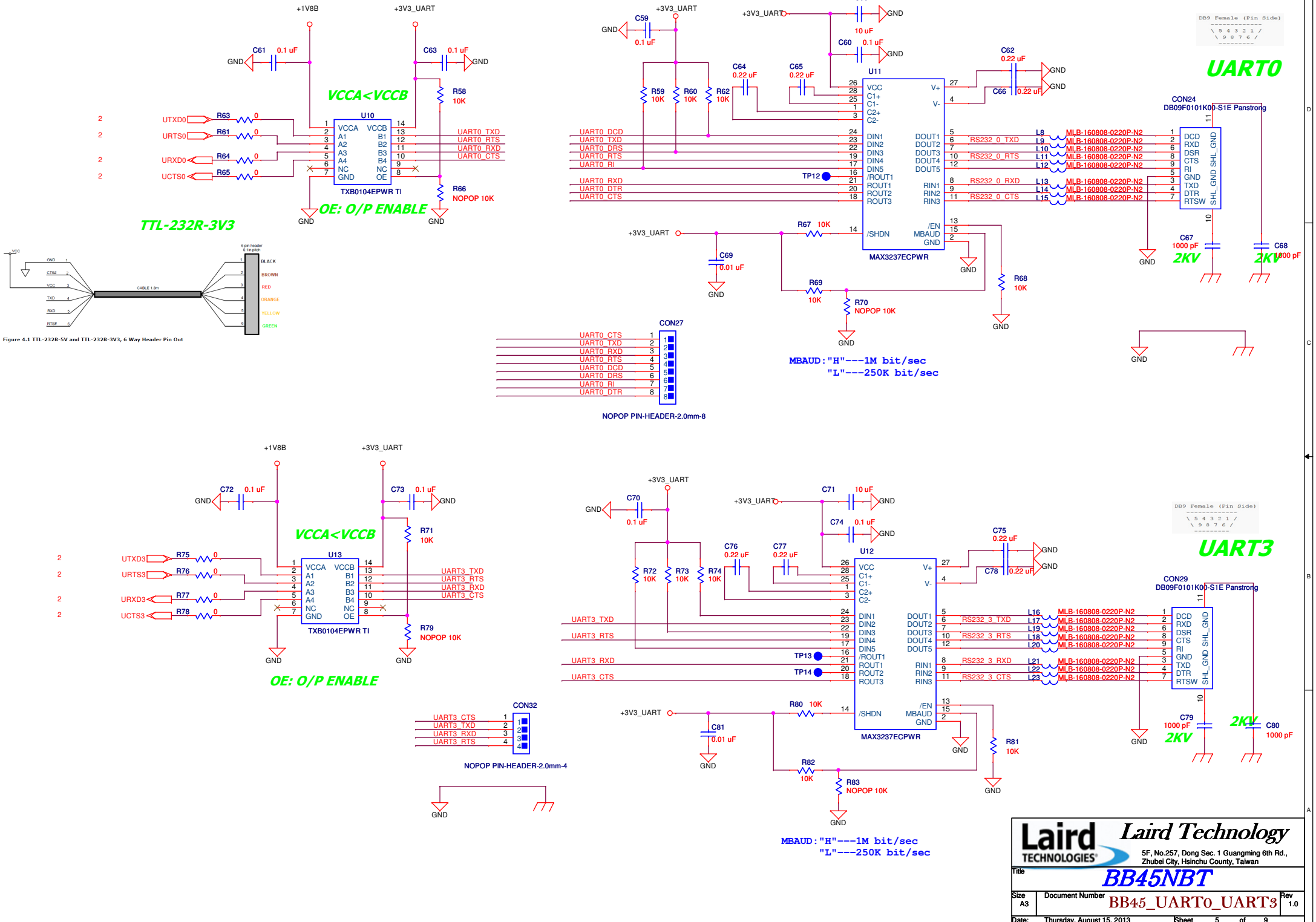
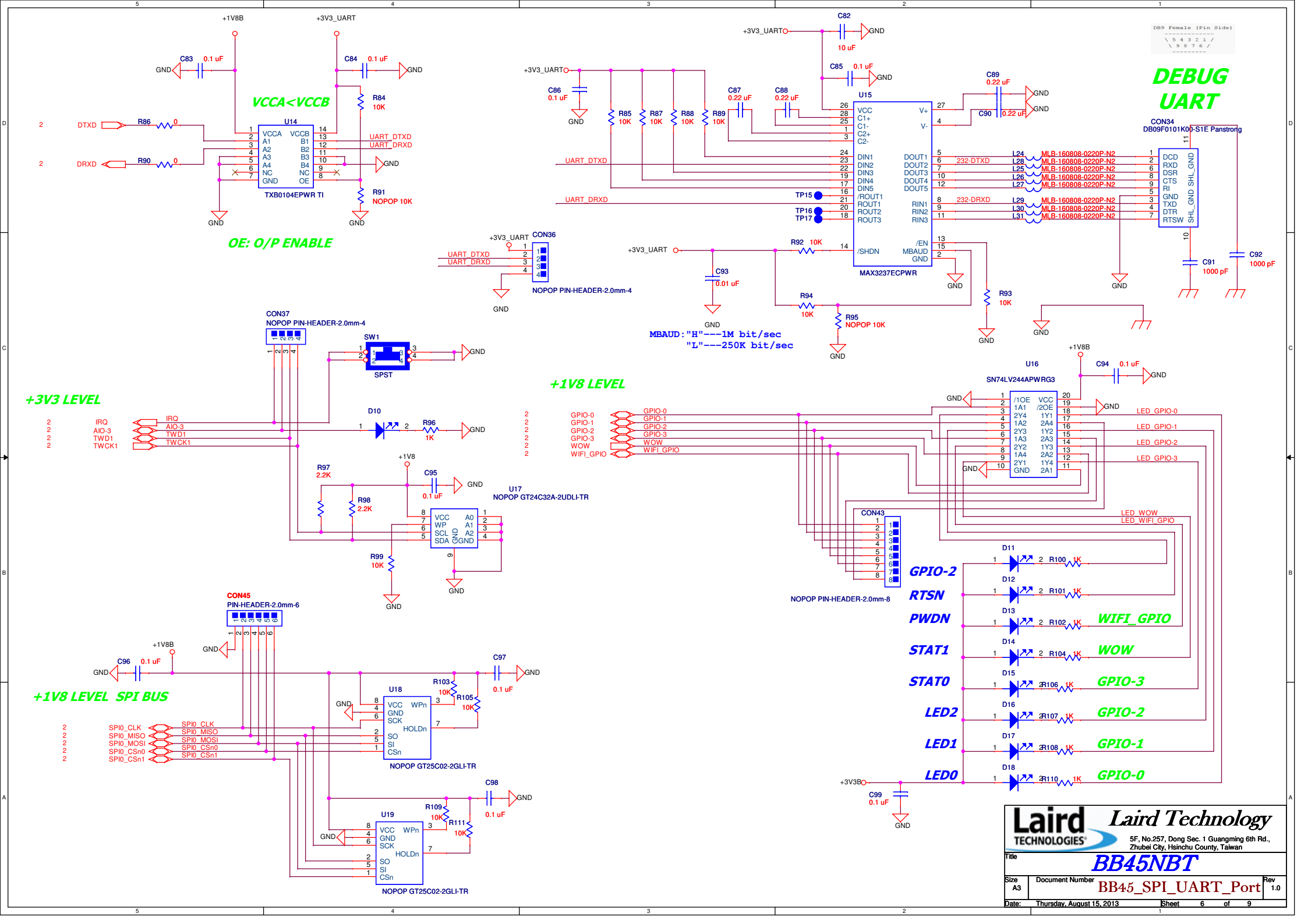


Figure 4.1 TTL-232R-5V and TTL-232R-3V3, 6 Way Header Pin Out


VCCA<VCCB
U14
TXB0104EPWR TI
OE: O/P ENABLE
DEBUG UART
CON34
DB09F0101K00-S1E Panstrong
U15
MAX3237ECPWR
MBAUD:"H"---1M bit/sec
"L"---250K bit/sec
CON36
NOPOP PIN-HEADER-2.0mm-4
CON37
NOPOP PIN-HEADER-2.0mm-4
SW1
SPST
+3V3 LEVEL
+1V8 LEVEL
U16
SN74LV244APWRG3
U17
NOPOP GT24C32A-2UDLI-TR
CON43
NOPOP PIN-HEADER-2.0mm-8
CON45
PIN-HEADER-2.0mm-6
+1V8 LEVEL SPI BUS
U18
NOPOP GT25C02-2GLI-TR
U19
NOPOP GT25C02-2GLI-TR
GPIO-2
RTSN
PWDN
STAT1
STAT0
LED2
LED1
LED0
WIFI_GPIO
WOW
GPIO-3
GPIO-2
GPIO-1
GPIO-0
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BB45_SPI_UART_Port
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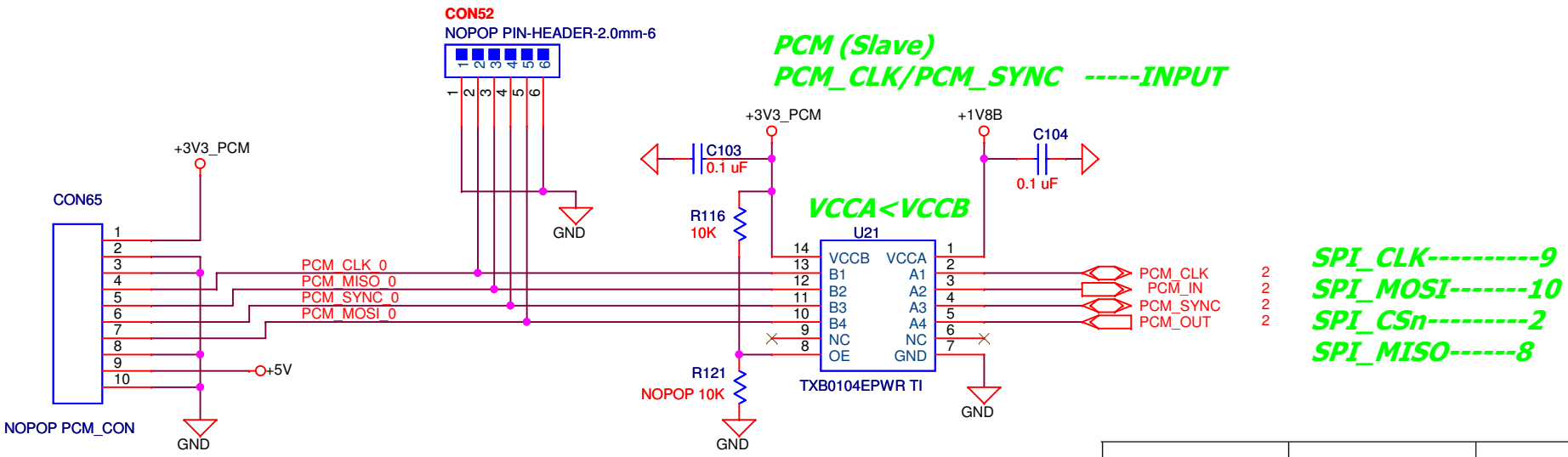

SPI Signal	Casira CN16 Pin (16 Way IDC)	LPT Port Pin (25 Way D-type)
SPI_MISO	2	10
SPI_CSB	3	2
SPI_MOSI	4	8
SPI_CLK	6	9
XAP_RESET	14	16
GROUND	5, 7	24

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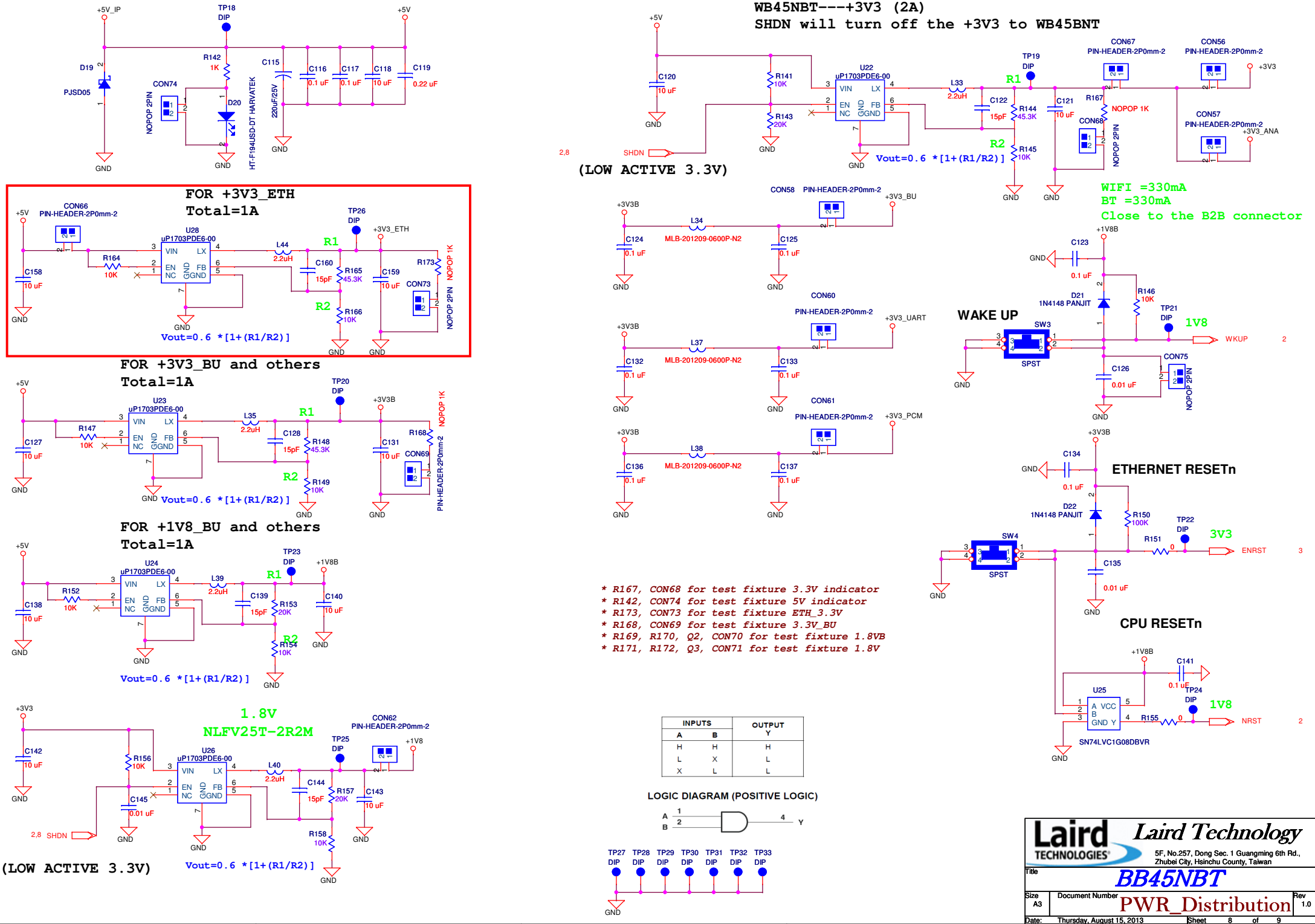
WB45NBT---+3V3 (2A)
SHDN will turn off the +3V3 to WB45BNT
(LOW ACTIVE 3.3V)
WIFI =330mA
BT =330mA
Close to the B2B connector
FOR +3V3_ETH
Total=1A
FOR +3V3_BU and others
Total=1A
FOR +1V8_BU and others
Total=1A
1.8V
NLFV25T-2R2M
(LOW ACTIVE 3.3V)
WAKE UP
ETHERNET RESETn
CPU RESETn
* R167, CON68 for test fixture 3.3V indicator
* R142, CON74 for test fixture 5V indicator
* R173, CON73 for test fixture ETH_3.3V
* R168, CON69 for test fixture 3.3V_BU
* R169, R170, Q2, CON70 for test fixture 1.8VB
* R171, R172, Q3, CON71 for test fixture 1.8V
INPUTS A B
OUTPUT Y
H H H
L X L
X L L
LOGIC DIAGRAM (POSITIVE LOGIC)
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BB45NBT
PWR_Distribution
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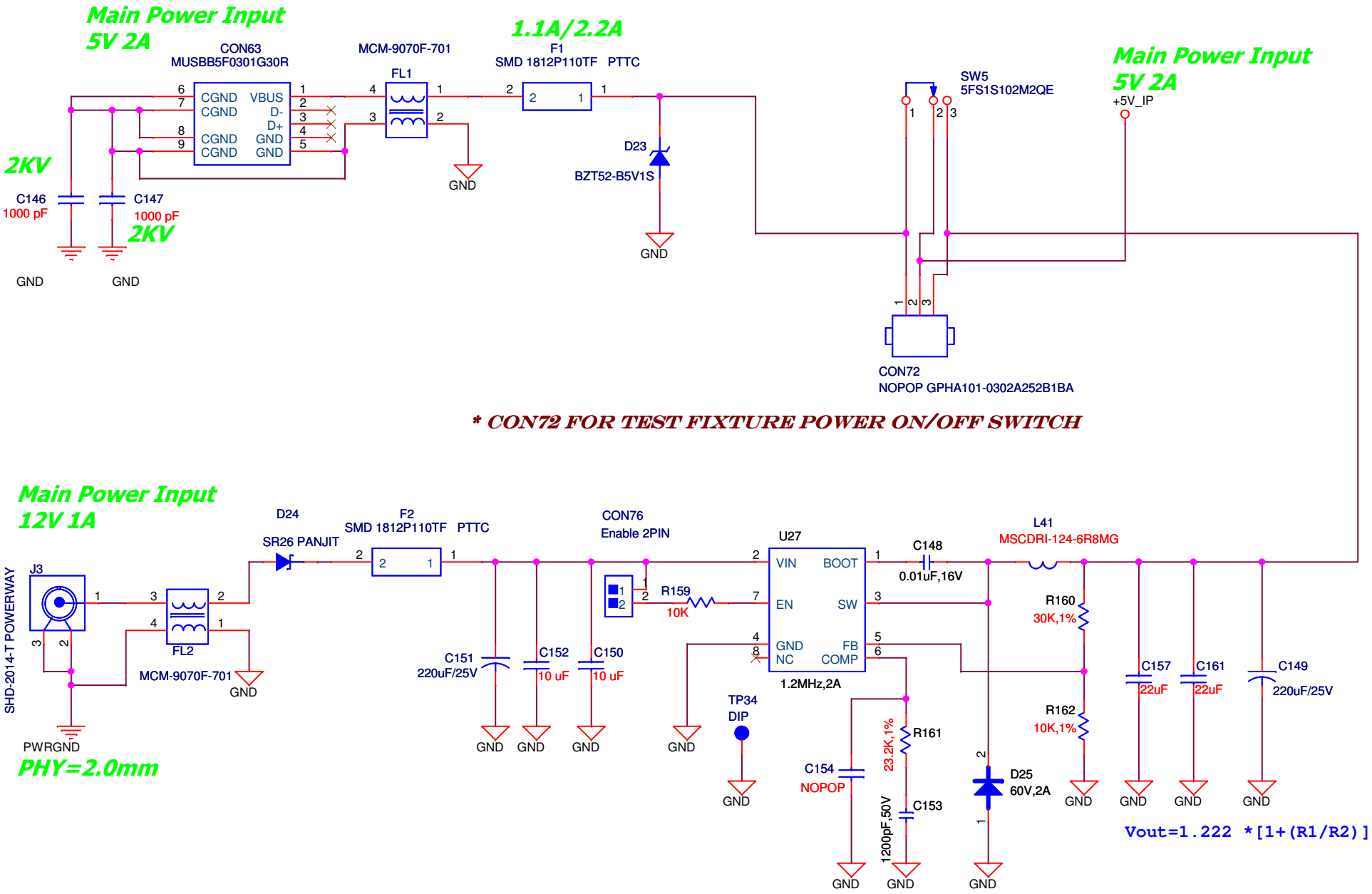

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Size A4	Document Number PWR_Input	Rev 1.0
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