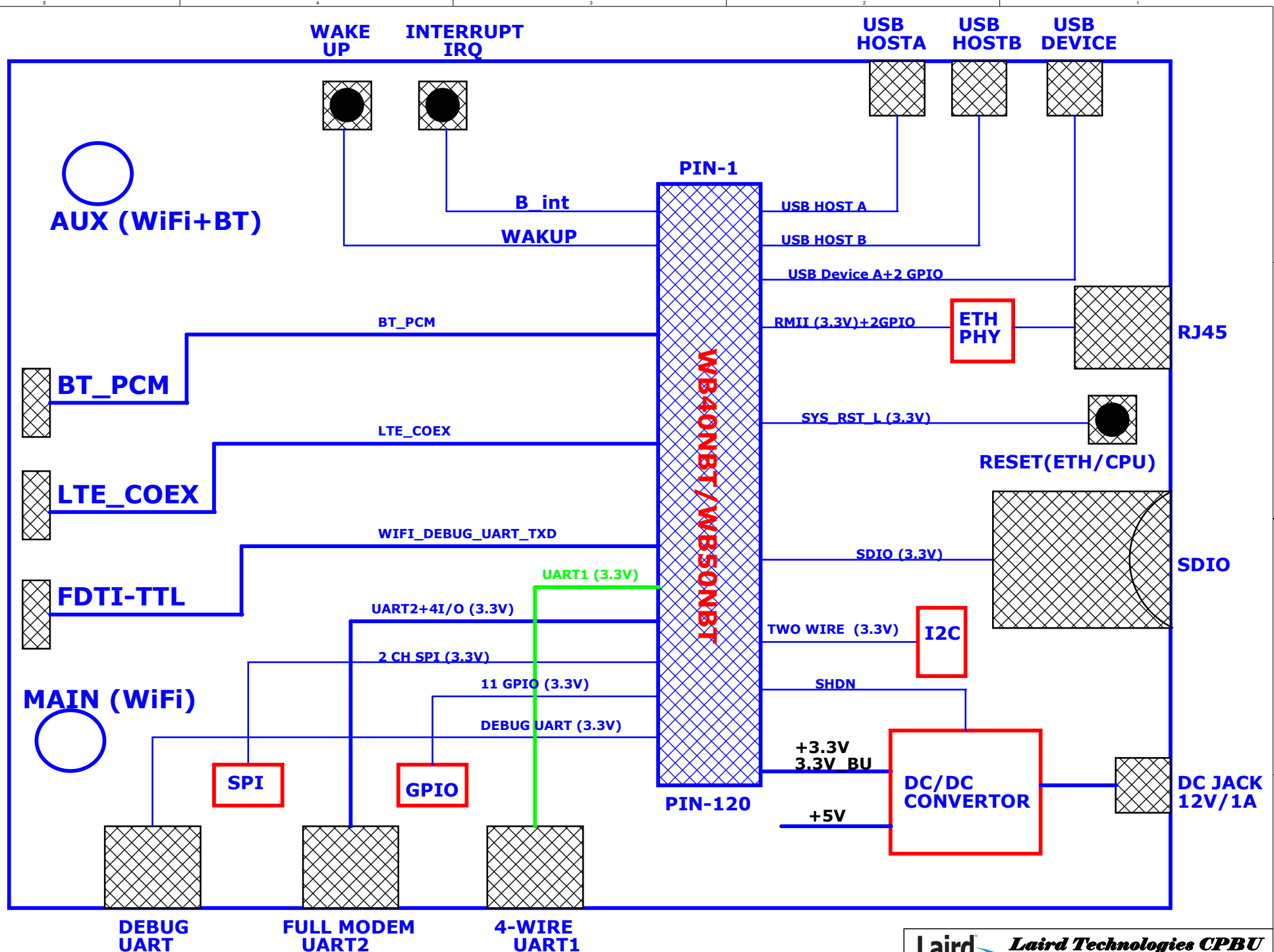




DATE	REVISION NUMBER	INITIALS	Initial Release
2016/03/14	V1.0	Andrew Chen	Initial draft
2016/05/19	V1.1	Andrew Chen	D6/D24 : silkscreen issue. SW3,SW6,SW4-----pin-1 is no connection. D11,D14,D15,D16,D17,D18-----swap placement

PCB design specification

1. Substrate: FR4 ROHS compliant, High TG 140 degree.
2. Solder mask, color=GREEN, Silkscreen color=WHITE
3. Surface finish to be Immersion Nickel/Gold (ENIG) with 1-2 u"
4. Start with 1 oz. copper on all layers.



Laird

Laird Technologies CPBU
5F, No. 257, Dong Sec. 1, Guangming 6th Rd,
Zhubei City, Hsinchu County 30264, Taiwan (R.O.C)

Project Name:

BB50NBT

Designed By:

Andrew Chen

Date :

Friday, September 30, 2016

Reversion :

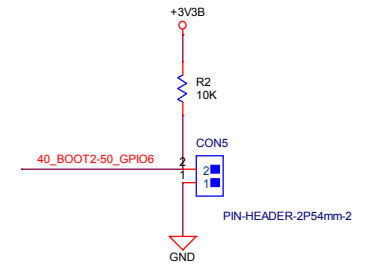
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Sheet

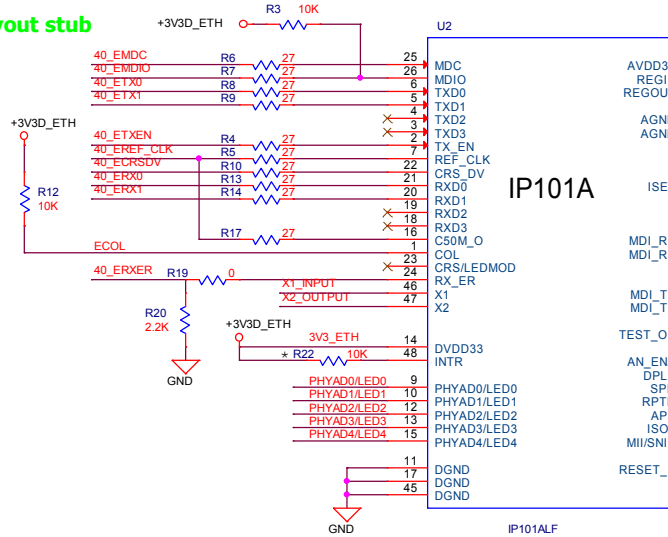
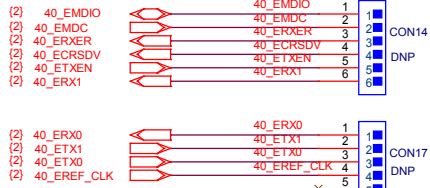
1 OF 9

Approved By:

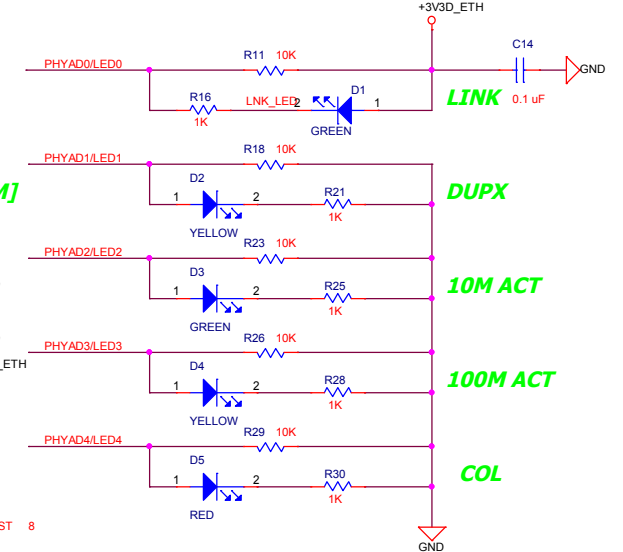




CON14/17 are placed in-line. No layout stub



Set IP101A to RMII Mode
LED and PHY address Configuration
This schematic sets PHY address to 00001



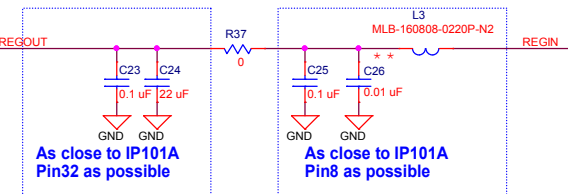
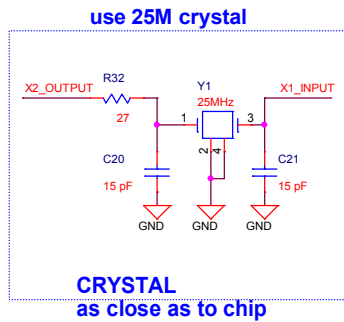
Pin48 could be short 3V3_ETH if interrupt function is not used.

Hardwire Configuration network:

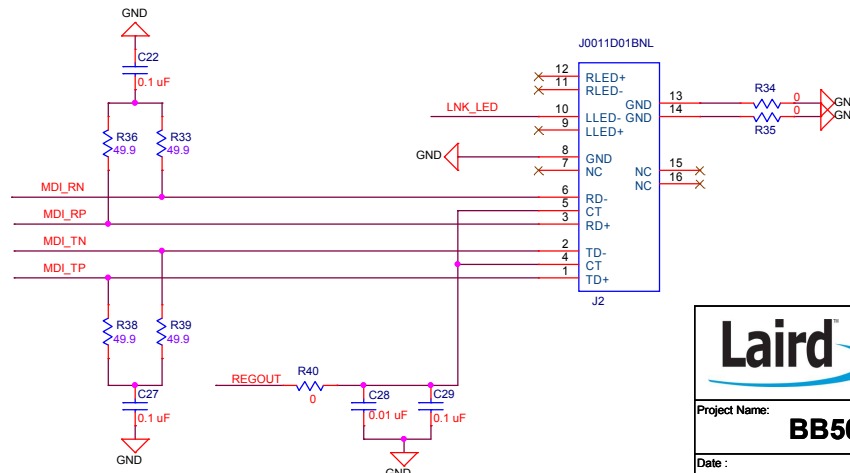
- This configuration shows
Enable: Auto negotiation, Full duplex, 100Mbps,
Link Down Power Saving, RMII interface
Disable: Isolate, Repeater mode
- These seven configuration pins could be connected to VDD or GND directly.

* Pull down U2 pin4 for RMII clock source 25MHz.

Pin1	Pin44	Function
COL/RMII	MII/SNIB	
1	1	RMII, ext 50MHz osc clk in to pin7
1	0	RMII, 25MHz crystal or osc from X1,X2; 50MHz clk out to pin16. (Please refer to the following figure for our recommended application circuit.)
0	1	MII, 25MHz crystal or osc from X1,X2
0	0	SNI, 25MHz crystal or osc from X1,X2



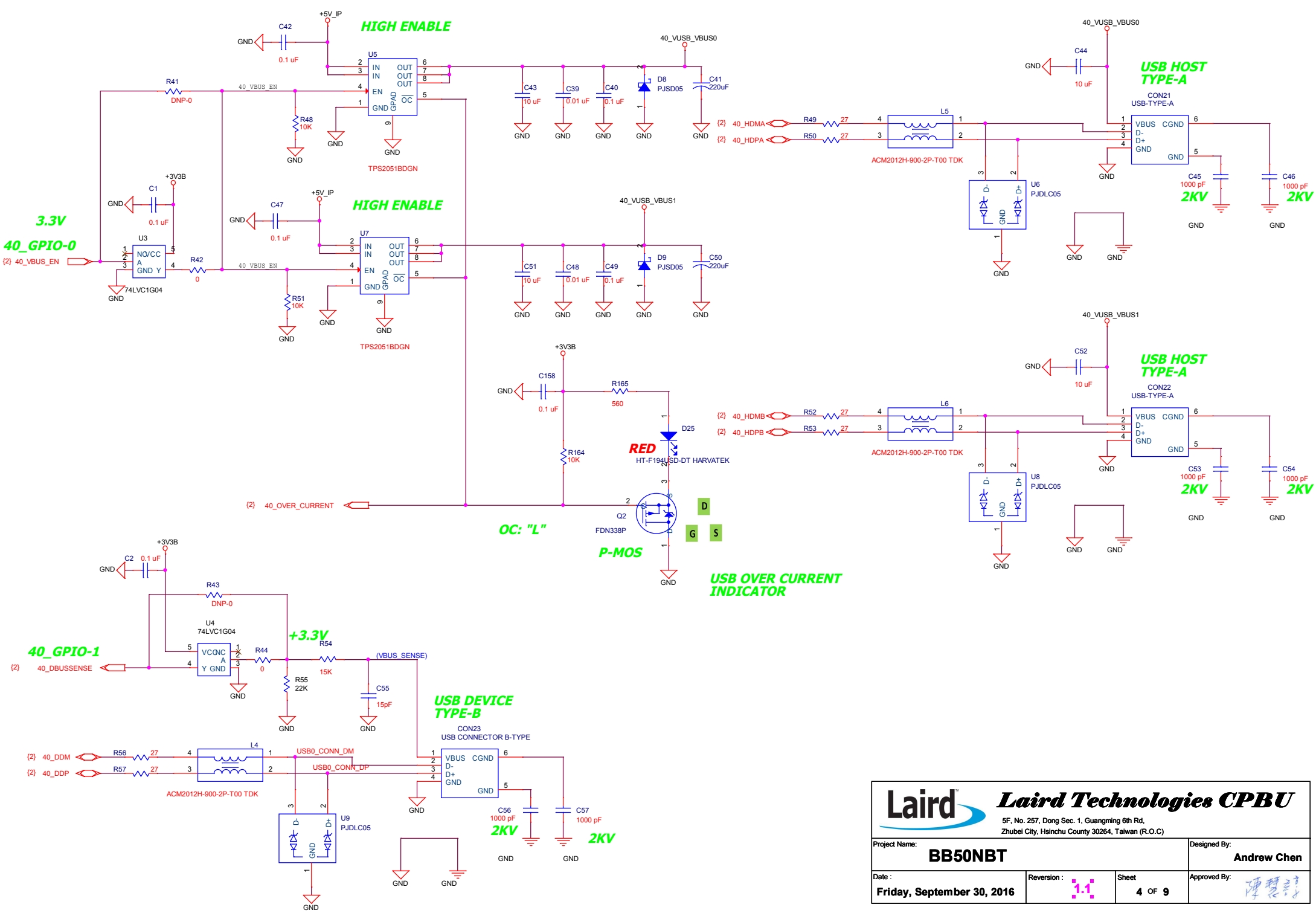
** Bead should be placed as close to IP101A as possible and in the same side as IP101A.



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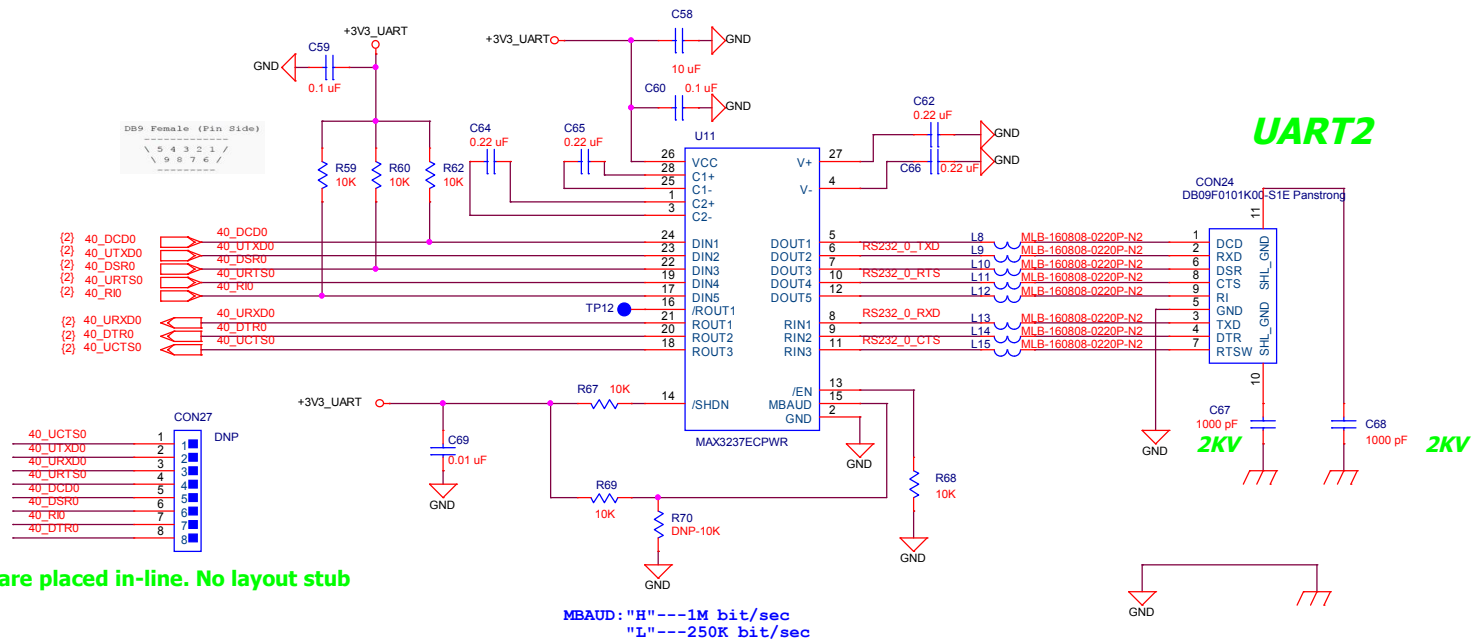
Project Name: BB50NBT		Designed By: Andrew Chen	
Date: Friday, September 30, 2016	Reversion: 1.1	Sheet: 3 OF 9	Approved By:



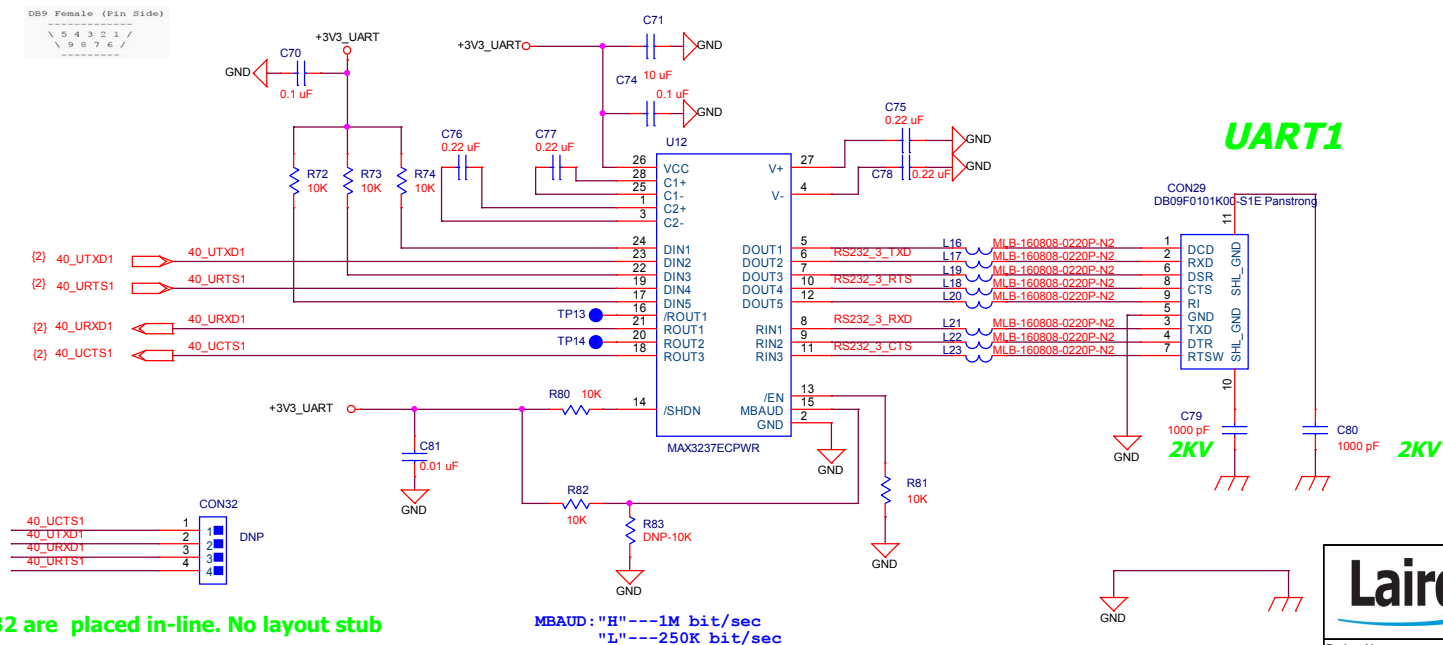


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Date : Friday, September 30, 2016	Reversion : 	Sheet 4 OF 9	Approved By: 



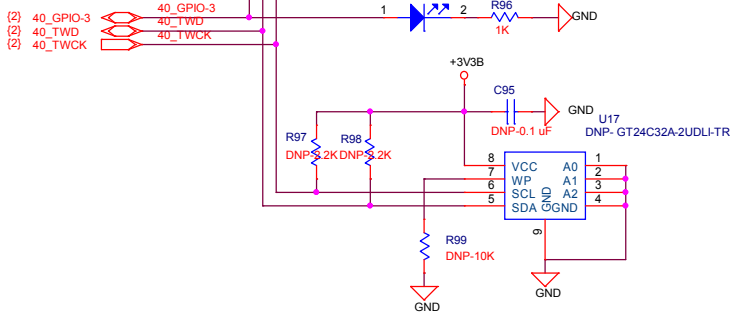
CON27 are placed in-line. No layout stub



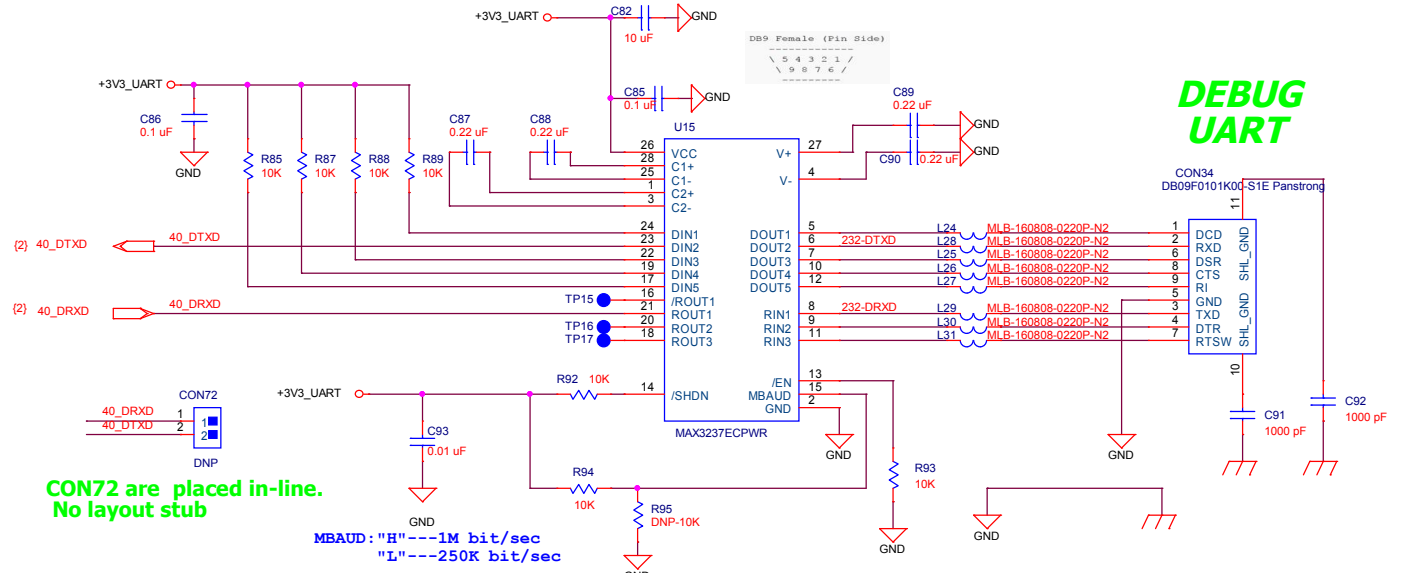
CON32 are placed in-line. No layout stub

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+3V3 LEVEL

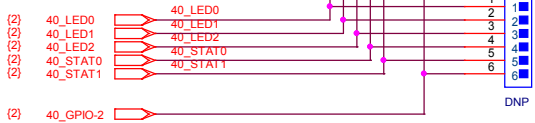


CON72 are placed in-line.
No layout stub



MBAUD: "H"---1M bit/sec
"L"---250K bit/sec

+3V3 LEVEL



CON43 are placed in-line.
No layout stub

GPIO-2

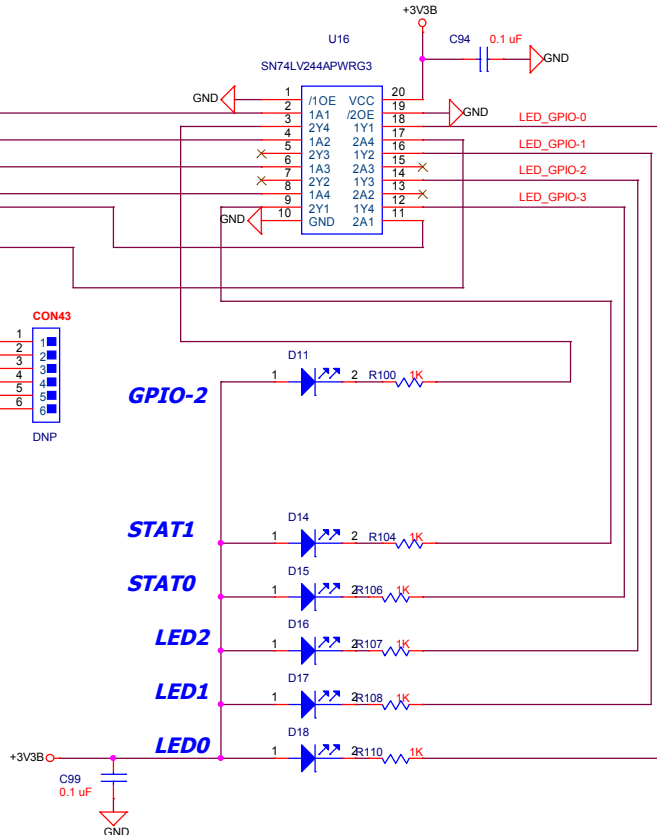
STAT1

STAT0

LED2

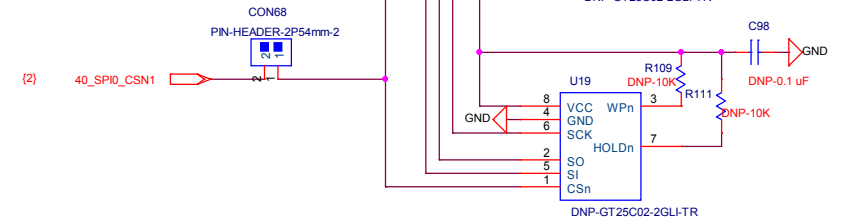
LED1

LED0



+3V3 LEVEL SPI BUS

- (2) 40_SPI0_CLK
- (2) 40_SPI0_MISO
- (2) 40_SPI0_MOSI
- (2) 40_SPI0_CS0





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Project Name: **BB50NBT**

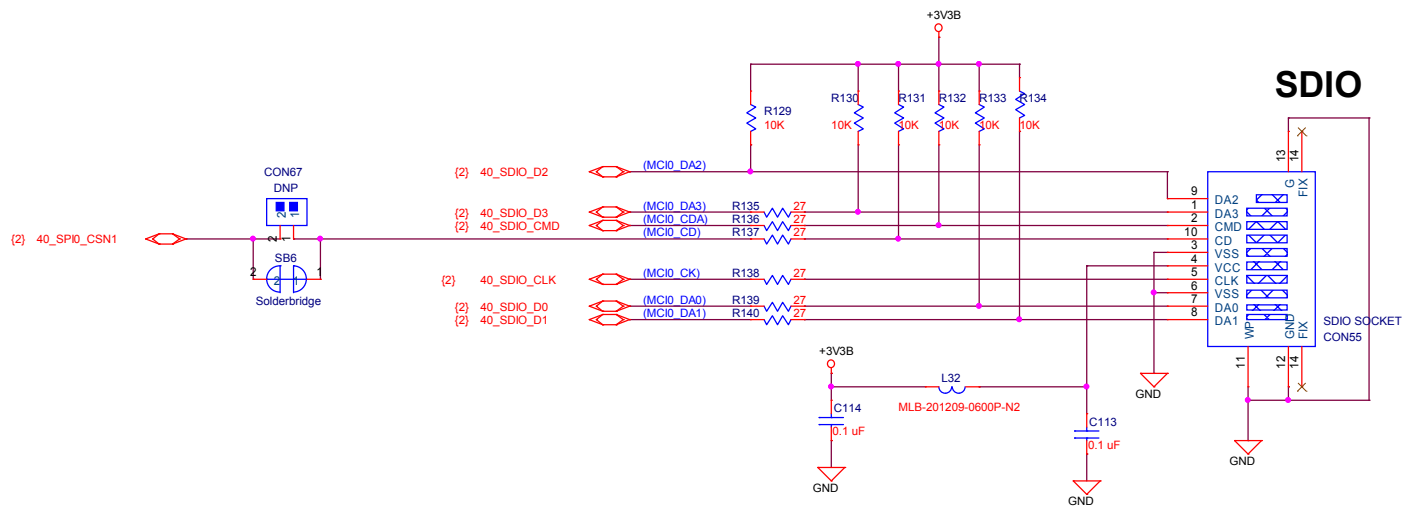
Designed By: **Andrew Chen**

Date: **Friday, September 30, 2016**

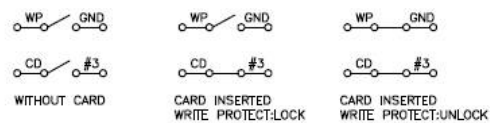
Reversion: **1.1**

Sheet: **6 OF 9**

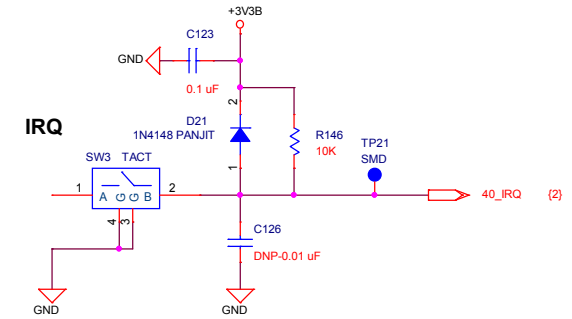
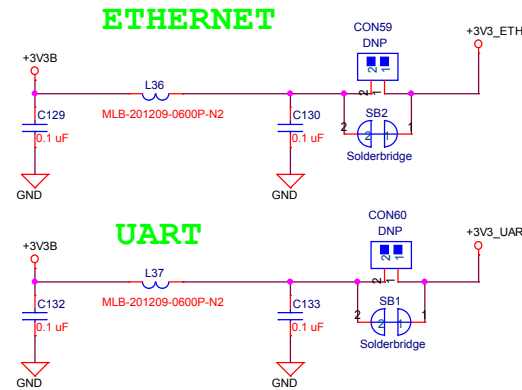
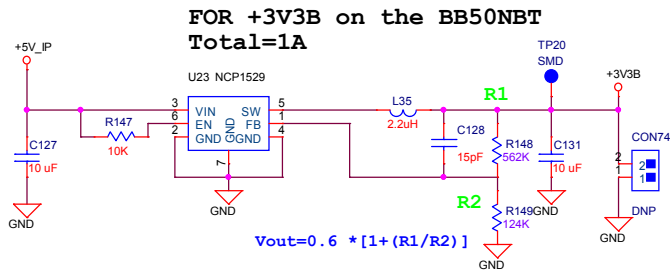
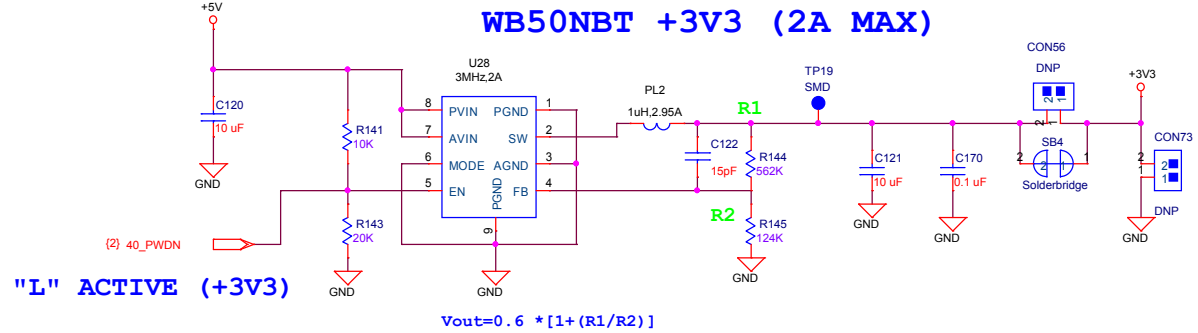
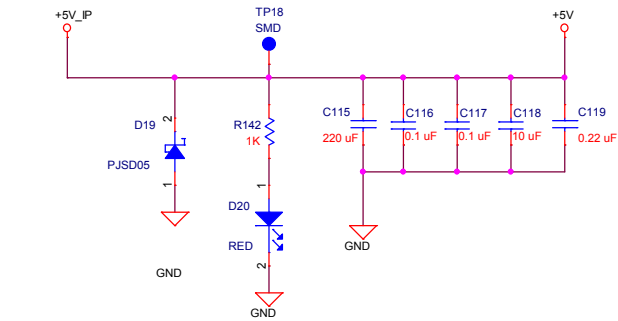
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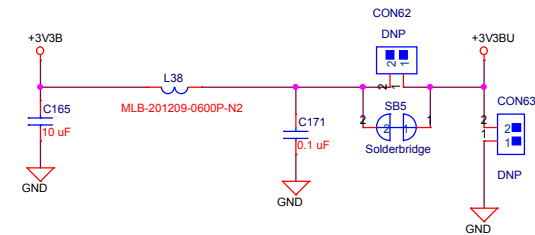
CIRCUIT:



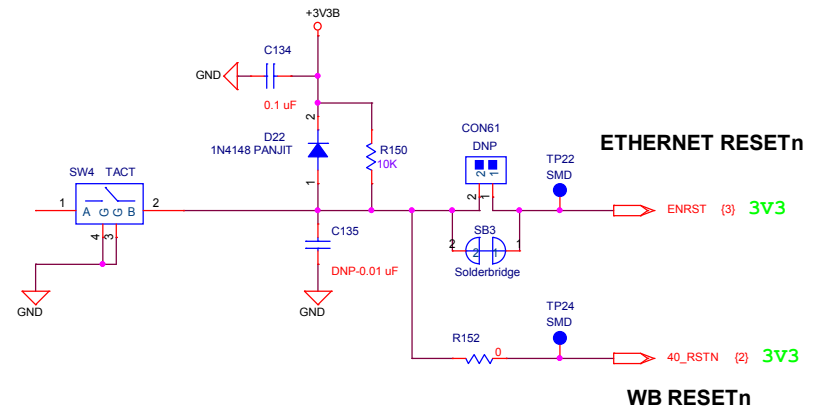
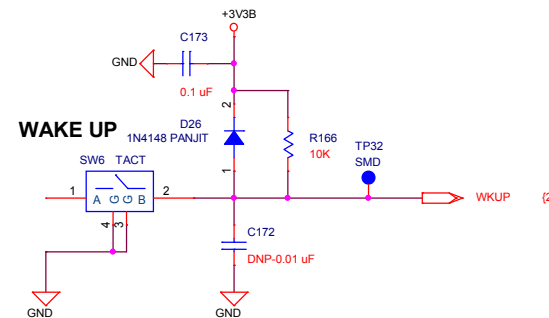
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Project Name: BB50NBT	Designed By: Andrew Chen
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WB50NBT BACKUP POWER



CON63: FOR BACKUP POWER FROM BAT



Main Power Input
12V 1A

PHY=2.0mm

Main Power Input
5V1.8A

Main Power Input
5V 1.8A

$$V_{out} = 0.8 * [1 + (R1/R2)]$$

GND PIN FOR TESTING

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