

# BT8x0 PCB RF Design

*For Laird Bluetooth -ST-type modules* 

## **INTRODUCTION**

The BT8x0 series of modules has the following two product types:

- -SA Has an integrated chip antenna
- -ST Exports the RF signal to an external RF connector (i.e., u.FL) via a solder pad on the module

This document mainly describes how to design the RF trace to keep good insertion, return loss, and  $50\Omega$  impedance for the RF signal trace from the solder pad of the BT module to u.FL connector for the -ST type.

**Note:** The -SA type has its own good LC matching circuit to perform  $50\Omega$  impedance matching on-board from the RF output port of the main chipset to the chip antenna.

#### **ANTENNA CIRCUIT FOR -ST**

We recommend that you place a  $\pi$  - type of matching circuit between the solder pad of RF output port of the BT module and the u.FL for 50 $\Omega$  impedance matching, as shown in the Figure 1.

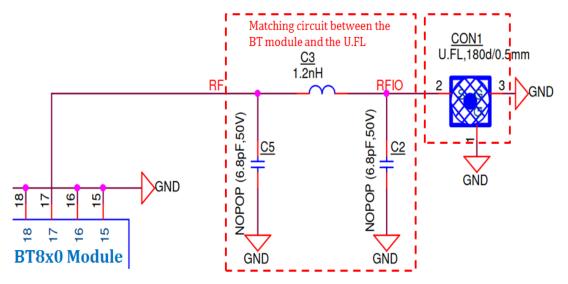


Figure 1: Recommended antenna circuit

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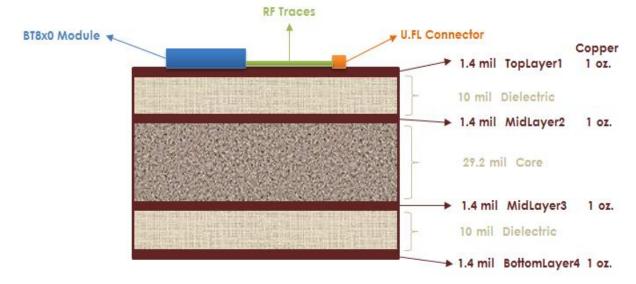
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# PCB LAYER STACK

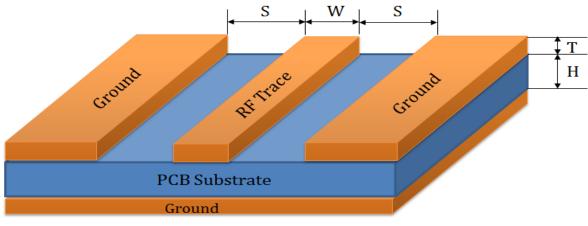


We recommend that OEMs use at least a 4-layer stack for platform design, as shown on the Figure 2.

Figure 2: 4-layer stack

# IMPEDANCE CALCULATION FOR RF TRACE

We recommend the coplanar waveguide structure, as shown in Figure 3.



- H: PCB substrate thickness
- T: Copper thickness
- W: RF Trace width for  $50\Omega$
- S: Space between RF trace and Ground Plane

Figure 3: Recommended coplanar waveguide structure

#### BT8x0 PCB RF Design



**Application Note** 

In accordance to the PCB stack shown in Figure 2, calculate RF trace of impedance with the appropriate trace width and spacing between trace and ground, as shown on the Figure 4.

Sig000 PCB Transmission Line Field Solver - [C:\Program Files (x86)\Polar(Si9000\Untitled.Si9]									
File Edit Configure Help			- Parameter Entr	( Linite					
			<ul> <li>Mils</li> </ul>	C Inches	C Microns	C Milline	tres		
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Coated Copianar Waveg	uide with Ground 15	Substrate 1 Dieleo	etric Er1	4.2000 +/-	0.0000 4.2000	4.2000	Calculate		
CEr C1 C2 W2	D1 ↔ IT1	Lower Trace Widt	h W1	17.0000 +/-	0.0000 17.000	17.0000			
		Upper Trace Widt	h W2	16.0000 +/-	0.0000 16.0000	16.0000	Calculate		
Coated Coplanar Strips With Low	l l	Ground Strip Sepa	aration D1	14.0000 +/-	0.0000 14.0000	14.0000	Calculate		
H1 Er1		Trace Thickness	T1	1.4000 +/-	0.0000 1.4000	1.4000	Calculate		
		Coating Above Su	ibstrate C1	1.0000 +/-	0.0000 1.000	1.0000			
Coated Coplanar		Coating Above Tra	ace C2	1.0000 +/-	0.0000 1.0000	1.0000			
Strips With Low www.polarinstru	iments.com	Coating Dielectric	CEr	4.2000 +/-	0.0000 4.2000	4.2000			
Notes		Impedance	Zo	49.31	49.31	49.31	Calculate		
Coated Coplanar Add your comments here	C Standard						More		
Waveguide 1B	Extended								
	- G.S. Convergence -								
	<ul> <li>G.S. Convergence</li> <li>Fine (Slower)</li> </ul>								
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Figure 4: Calculating RF trace of impedance

For calculation and to get a correct impedance, input the trace width (W1) and spacing (D1) to the PCB design rule/layout tool and assign these rules for the RF trace.

## PCB PLACEMENT AND LAYOUT

Figure 5 shows the placement of the matching circuit and u.FL connector.

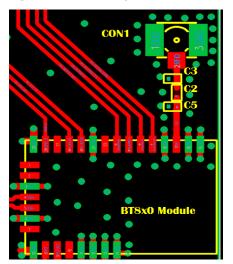


Figure 5: Matching circuit and u.FL connector placement

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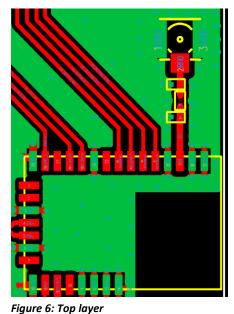
#### BT8x0 PCB RF Design

**Application Note** 



Place the matching circuit and u.FL close to the RF feed pad of the BT8x0 module.

To keep the integrated ground plane to the surrounding RF trace and u.FL connector on both top layer and reference layer (MidLayer 2; see Figure 2), place adequate ground vias to the surrounding as well as shown in Figure 6 and Figure 7.



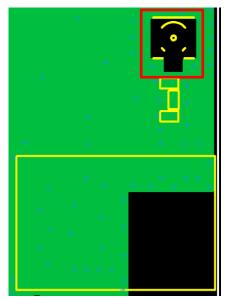


Figure 7: Reference layer

**Note:** We recommend that you keep no ground copper for all layers of the u.FL connector, as shown in the red box of Figure 7.

#### **REVISION HISTORY**

Version	Date	Notes	Contributor(s)	Approver
1.0	12 Jan 2018	Initial Release	Jacky Kuo	Jonathan Kaye