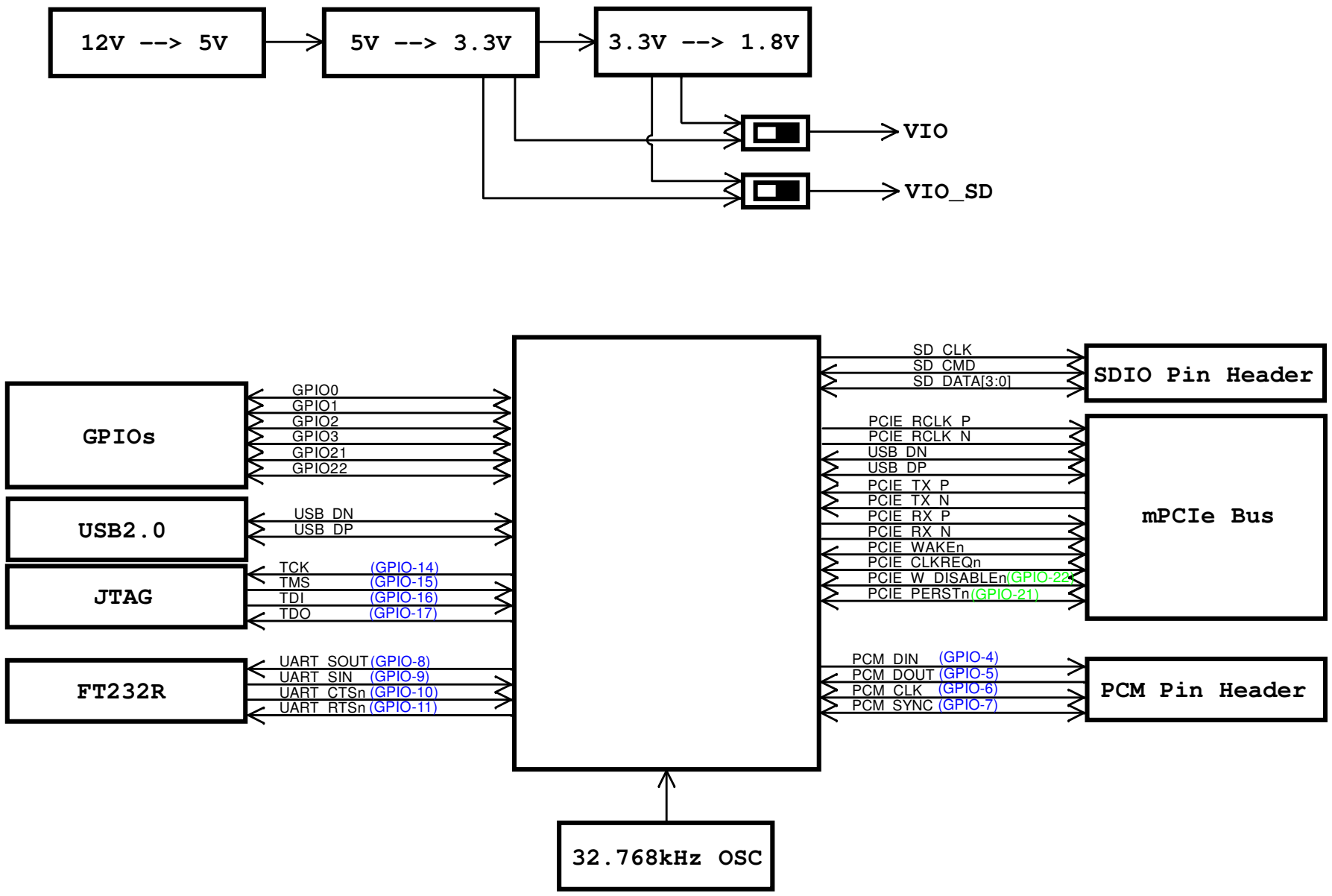


Laird

Laird Technologies CSBU

5F, No. 257, Dong Sec. 1, Guangming 6th Rd,
Zhubei City, Hsinchu County 30264, Taiwan (R.O.C)

Project Name :	Schematic Name :	Drawing By :
DVK-60-SIPT	DVK-60-SIPT_Blockdiagram	*<Kai Wei>*

Date :	Sheet :	Revision :
Friday, May 26, 2017	1 of 6	1.0

DATE	REVISION NUMBER	INITIALS	INITIAL RELEASE
2016/08/11	A0	Kai Wei	Initial Draft
2016/08/18	A0	Kai Wei	Clean up for EVT design review 1. Change J6,J7,J8 from female to male pin header
2016/08/22	A0	Kai Wei	Clean up for EVT design review 1.Add C49 (0.1uF/0402) and C50 (0.01uF/0402) for VIO on FTDI chip. 2.Change J1,J2,J3,J5,J12,J13,J20,R12,R13,R51,C47,C48 to NP. 3.Change the Orcad symbol of SSD60NBT to the latest one which updated on 8/22. 4.Change U9 to RT8270
2016/09/14	A0	Kai Wei	Clean up for EVT design review
2016/09/14	B0	Kai Wei	Add C53,C54
2017/05/26	1.0	Kai Wei	Update Silkscreen : 1.Change model name to DVK-60-SIPT 2.Correct the HOST CONFIG setting

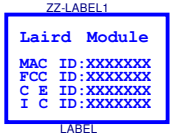
PCB design specification

1. Substrate: FR4 ROHS compliant, TG 140 degree.
2. Solder mask color=BLUE, Silkscreen color=WHITE
3. Surface finish to be Immersion Nickel/Gold (ENIG) with 1-2 u"
4. Start with 1/2 oz. copper on all layers.

ZZ-PCB1

PCB Substrate

ZZ-LABEL1

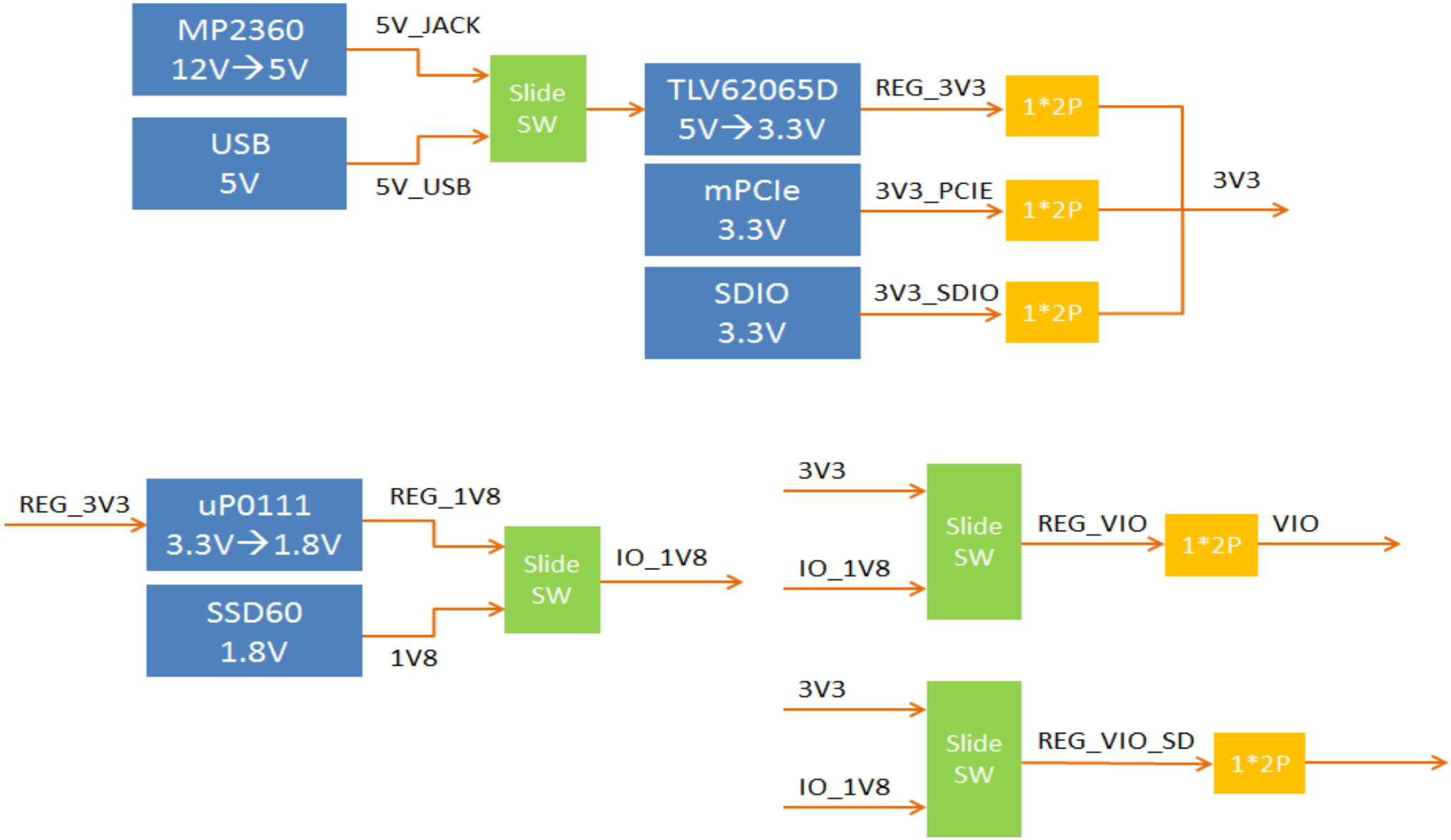


LABEL

Laird Technologies CSBU
5F, No. 257, Dong Sec. 1, Guangming 6th Rd,
Zhubei City, Hsinchu County 30264, Taiwan (R.O.C)

Project Name :	Schematic Name :	Drawing By :
DVK-60-SIPT	DVK-60-SIPT_Title and History	<Kai Wei>

Date : Friday, May 26, 2017 | Sheet : 2 of 6 | Revision : 1.0



Laird

Laird Technologies CSBU

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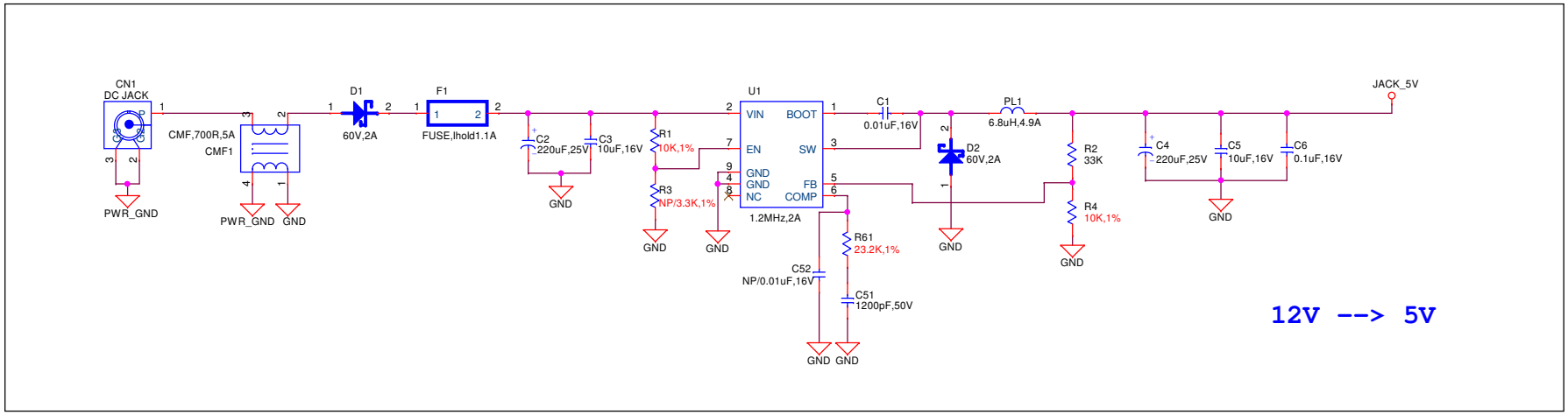
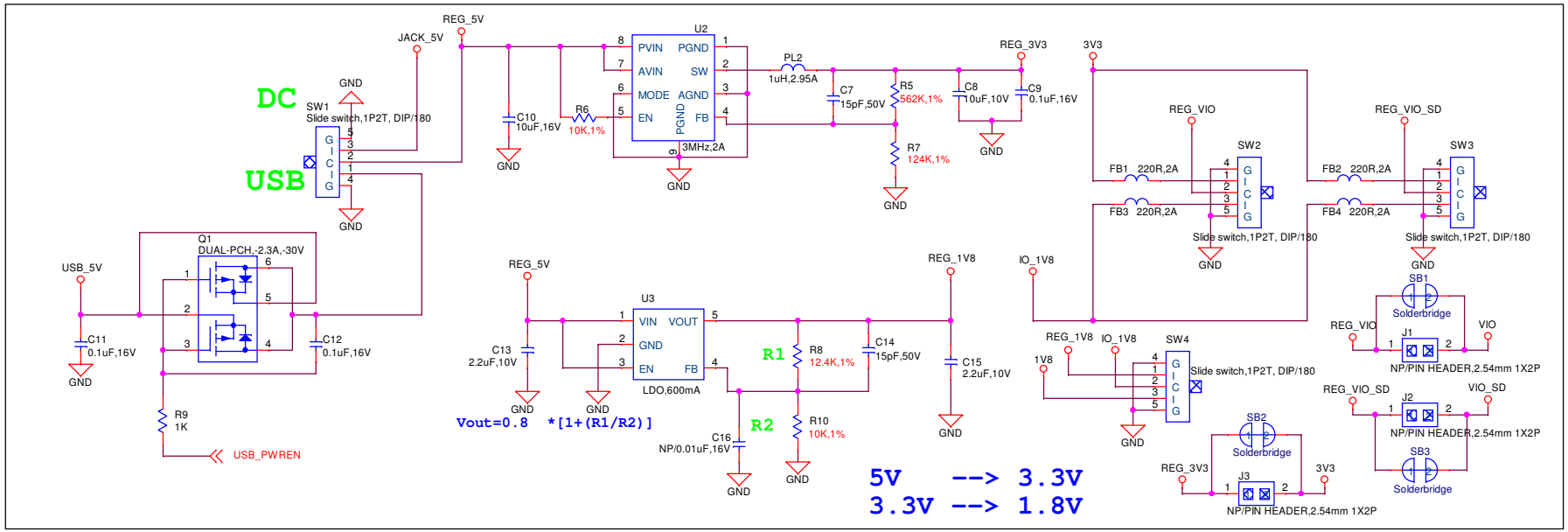
Zhubei City, Hsinchu County 30264, Taiwan (R.O.C)

Project Name :	Schematic Name :	Drawing By :
DVK-60-SIPT	**DVK-60-SIPT_Power Tree**	***<Kai Wei>***

Date :	Sheet :	Revision :
Friday, May 26, 2017	**3 of 6**	1.0





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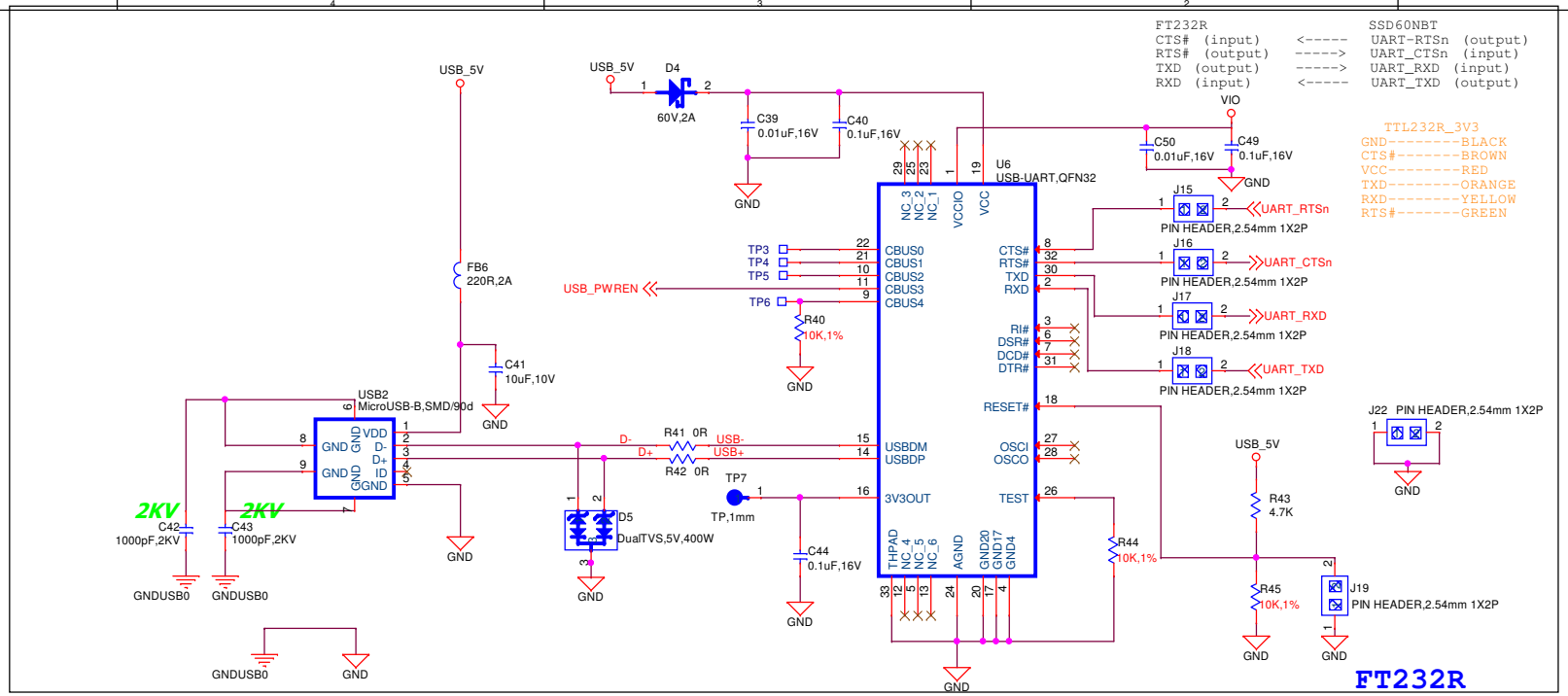
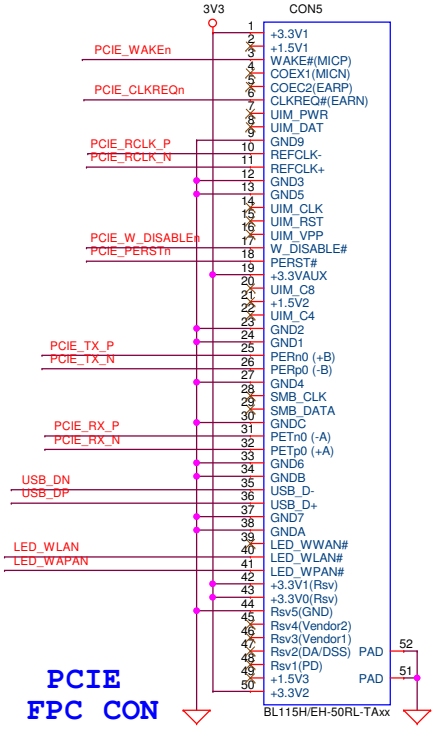
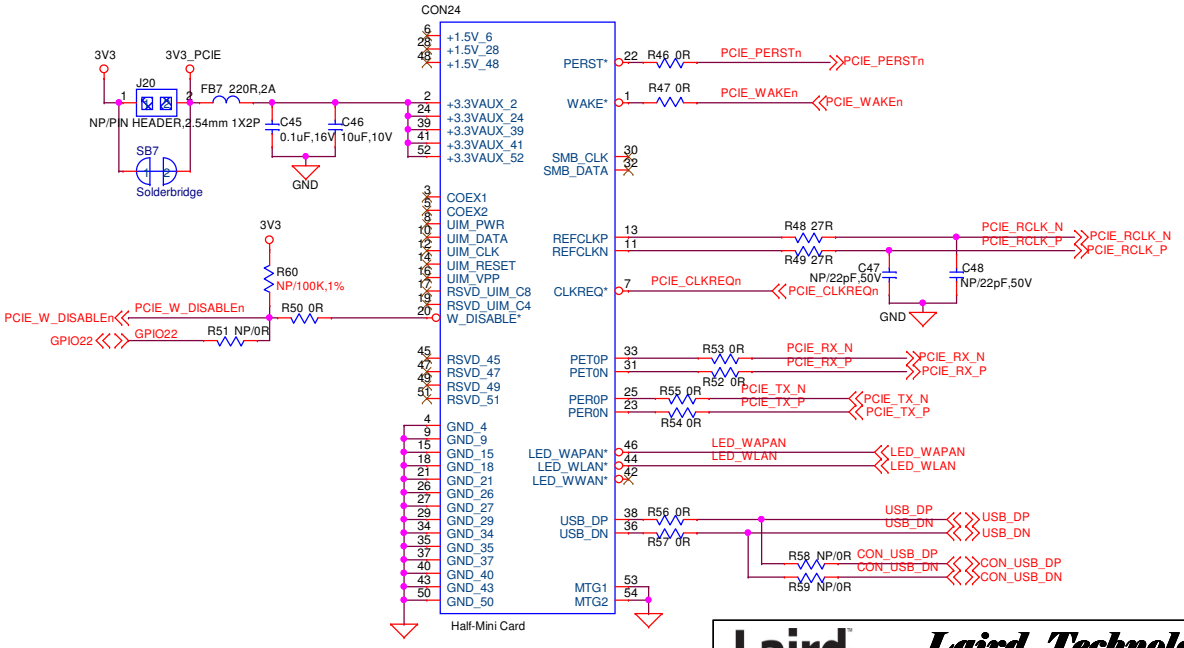
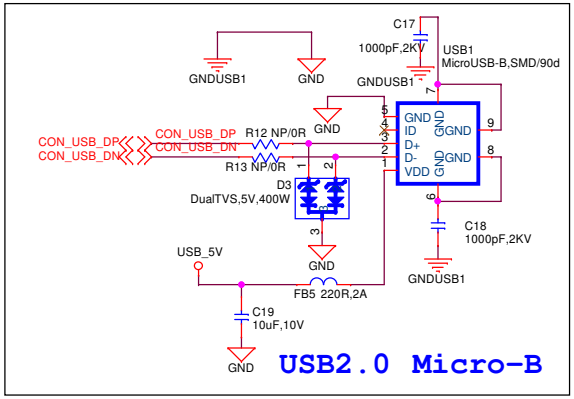
Project Name : DVK-60-SIPT	Schematic Name : DVK-60-SIPT_Power	Drawing By : <Kai Wei>
Date : Friday, May 26, 2017	Sheet : 4 of 6	Revision : 1.0

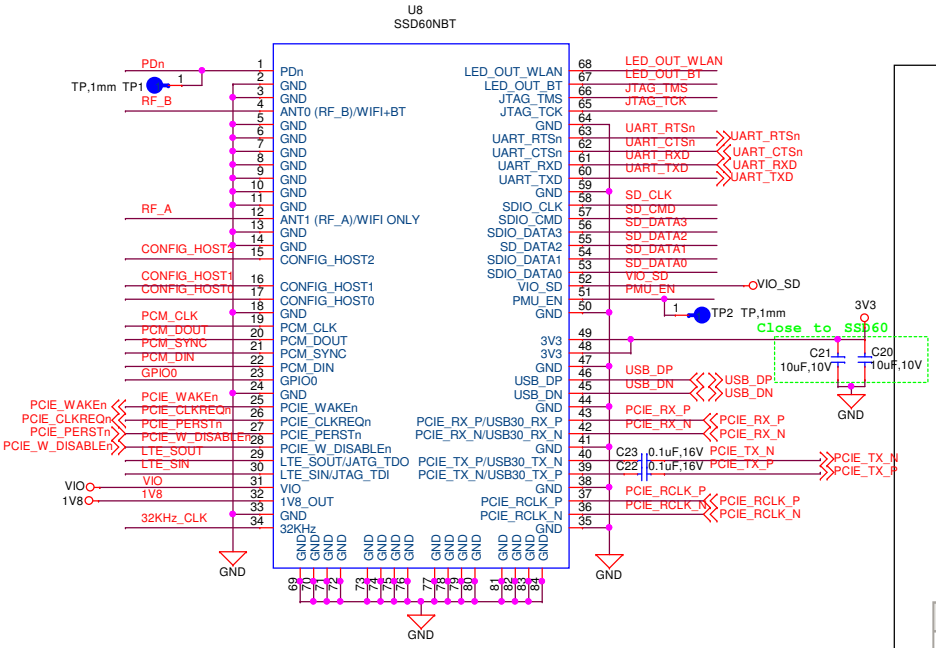


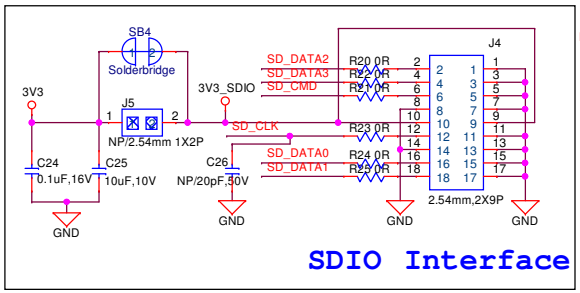


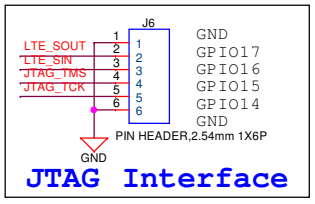


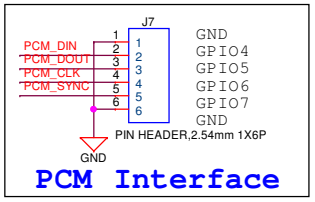
Laird **Laird Technologies CSBU** 5F, No. 257, Dong Sec. 1, Guangming 6th Rd, Zhubei City, Hsinchu County 30264, Taiwan (R.O.C)		
Project Name : **DVK-60-SIPT**	Schematic Name : **DVK-60-SIPT_mPCIe/UART**	Drawing By : *<Kai Wei>*
Date : **Friday, May 26, 2017**	Sheet : **5 of 6**	Revision : **1.0**

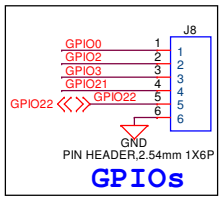


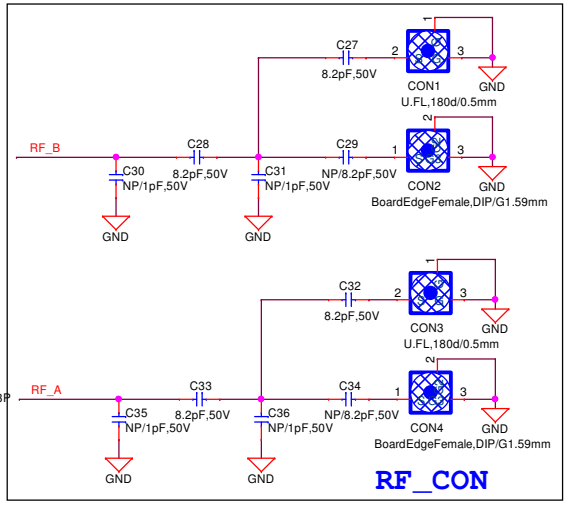


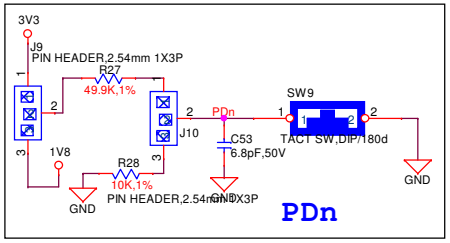


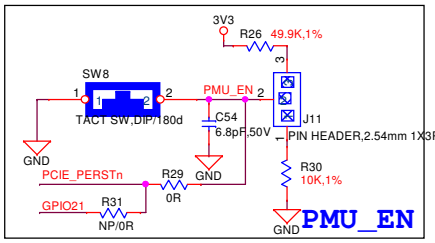


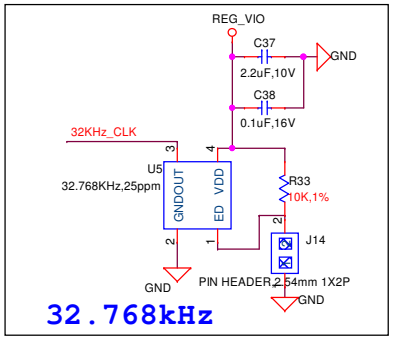


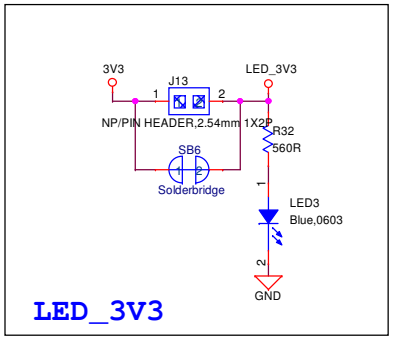


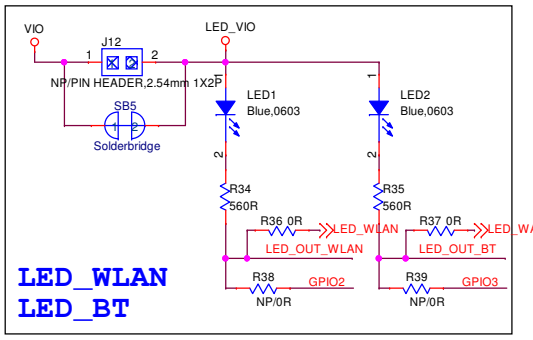


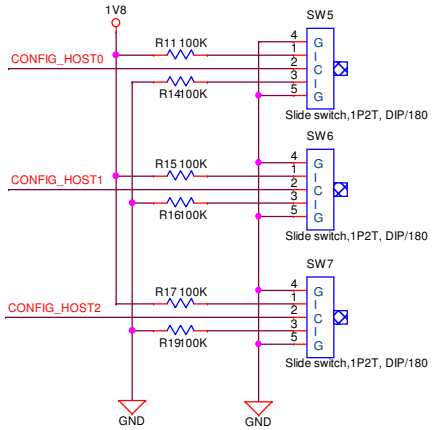












BootStrap Config. (REF:1V8)

Configuration Bits	Pin Name	Configuration Function
CON[3]	CONFIG_HOST[3]	Strap Test Mode 0 = strap test mode to select individual test mode 1 = normal mode (default in pad)
CON[2]	CONFIG_HOST[2]	Firmware Boot Options No hardware impact. Software reads and boots accordingly. See table below.
CON[1]	CONFIG_HOST[1]	
CON[0]	CONFIG_HOST[0]	

Strap Value	WLAN	Bluetooth/ BLE	ROM Notes	Firmware Download Mode	Number of SDIO Functions
000	SDIO	UART	--	Parallel	1 (WLAN)
001	SDIO	SDIO	--	Parallel	2 (WLAN, Bluetooth)
010	PCIe	USB 2.0	Initialize USB 2.0 PHY and COM PHY PCIe portion	Parallel	--
011	PCIe	UART	Initialize only COM PHY PCIe portion	Parallel	--
[illegible]	[illegible]	[illegible]	USB 3.0 and USB 2.0 PHY	[illegible]	[illegible]
101	USB 2.0	USB 2.0	Initialize only USB 2.0 PHY	Parallel	--
110	USB 3.0/2.0	USB 3.0/2.0	Initialize both COM PHY USB 3.0 and USB 2.0 PHY	Parallel	--
111	USB 3.0	USB 3.0	Initialize only COM PHY USB 3.0 portion	Parallel	--

Project Name :	Schematic Name :	Drawing By :
DVK-60-SIPT	DVK-60-SIPT_SIP	<Kai Wei>
Date : Friday, May 26, 2017	Sheet : 6 of 6	Revision : 1.0