<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION NUMBER</th>
<th>INITIALS</th>
<th>INITIAL RELEASE</th>
</tr>
</thead>
<tbody>
<tr>
<td>2016/08/11</td>
<td>A0</td>
<td>Kai Wei</td>
<td>Initial Draft</td>
</tr>
</tbody>
</table>
| 2016/08/18 | A0              | Kai Wei  | Clean up for EVT design review  
1. Change J6, J7, J8 from female to male pin header |
| 2016/08/22 | A0              | Kai Wei  | Clean up for EVT design review  
1. Add C49 (0.1uF/0402) and C50 (0.01uF/0402) for VIO on FTDI chip.  
2. Change J1, J2, J3, J5, J12, J13, J20, R12, R13, R51, C47, C48 to NP.  
3. Change the Orcad symbol of SSD60NBT to the latest one which updated on 8/22.  
4. Change U9 to RT8270 |
| 2016/09/14 | A0              | Kai Wei  | Clean up for EVT design review                                                   |
| 2016/09/14 | B0              | Kai Wei  | Add C53, C54                                                                     |
| 2017/05/26 | 1.0             | Kai Wei  | Update Silkscreen:  
1. Change model name to DVK-60-SIPT  
2. Correct the HOST CONFIG setting |

**PCB design specification**

1. Substrate: FR4 ROHS compliant, TG 140 degree.
2. Solder mask color=BLUE, Silkscreen color=WHITE
3. Surface finish to be Immersion Nickel/Gold (ENIG) with 1-2 u"  
4. Start with 1/2 oz. copper on all layers.
DVK-60-SIPT
DVK-60-SIPT_Power Tree
Friday, May 26, 2017

Laird Technologies CSBU
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Zhubei City, Hsinchu County 30264, Taiwan (R.O.C)

Project Name : DVK-60-SIPT
Schematic Name : DVK-60-SIPT_Power Tree
Drawing By : <Kai Wei>

Date : Friday, May 26, 2017
Sheet : 3 of 6 Revision : 1.0
Vout = 0.8 * [1 + (R1/R2)]