



| DATE       | REVISION<br>NUMBER | INITIALS | Initial Release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------------|--------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10Jan2016  | A0 ( EVT1 )        | RK       | SCH reviewed draft.<br>Added R122, R111, R123, C59, C49, C68, R124, TP21. Make JP1 and J20 NOPOP. Re-wire J29. Add C53 and C54 300pF MPN.<br>Add J34 coincell holder Vendor2 MPN. Added C69. Some wiring changes. Make C63 NOPOP.<br>Add sheet in BOM for Jumpers to be Fitted and SW4, SW5 and SW6 switch setting positions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 16May2016  | A1 ( EVT2 )        | RK       | Change U5 BL652-SX-A0 31 pin module (using WLCSP nRF52832-CHAA) to BL652-SX-A1 39 module (using QFN nRF52832-QFAA-xx).<br>Hence many wiring changes.<br>Change R59 30K 1% to 33K 1% (to generate 5V at D6pin2).<br>Changed U3 Dual OpAmp PCB footprint from SOP8 to SOIC-8.<br>Make Coulomb counter IC U4 a NOPOP hence, U4,C7(0.1uF), R30(3R3), Do Not Fit. Fit jumper in J7(default).<br>Change JP1 from NOPOP to Fit.<br>Update ZZ-PCB1 Description (DVK-BL652-A1)<br>Add Jumpers fitted list sheet. Fit Test Hook (black) into TP14 (GND).<br>Make the added DAC IC U17 a NOPOP hence, U17, C69(0.1uF), R110(0R), R109(0R) Do Not Fit.<br>Add SPI flash IC U18 and associated C5(0.1uF), R125(10K), R126(10K), SB4, SB5, SB6, SB7.<br>Add Y3 32.76kHz crystal and associated C71(15pF), C70(15pF), SB8, SB9, R127(0R), R128(0R).<br>Change J40 from 2pin header to 3pin header but still a NOPOP.<br>Add J44 2pin header but is a NOPOP<br>Change J29 from 6pin header to 10pin header but still a NOPOP.<br>Change J41 from 8pin header to 10pin header but still a NOPOP.<br>Add series 560R resistors R95, R96, R97, R129, R130, R131, R132, R133 in series with Arduino connector J30 (which carries signals D2 to D7).<br>Make R97 560R a NOPOP.<br>Add series 560R resistors R134, R135, R136 in series with Arduino connector J32 3 signals D8, D9, AREF).<br>Add series 560R resistors R93, R92, R80, R79, R50 in series with Arduino connector J31 five signals A5, A4, A3, A2, A1).<br>Change R123(0R) from a NOPOP to Fit on PB3(U14 ball J5).<br>Add C72(0.1uF) to GND on PB2(U14 ball G2) and wire to VCC_IO_UART.<br>Connect PB1 (U14 ball F1) to GND.<br>Delete from design R95, R96 560R. Add U5 PCB footprint name "MODULE_BL652Q_39P_SMD".<br>Change U17 PCB footprint from SOT23-6 to SOT23_6.<br>Change U13 from UPI uP0111AMA5-00 to RT9187BGB.<br>Change U8 symbol from 8-pin to 9-pin.<br>Change J40 from 3pin header to 2pin header but still a NOPOP.<br>Remove R7(0R) and move R14 (560R) to R7 location. |
| 23June2016 | B0                 | RK       | Change C70 from 15pF to 10pF.<br>Change C71 from 15pF to 12pF.<br>Change J8 to NOPOP.<br>Change Q1 MPN from Secos SST2623J to Fairchild FDC6310P.<br>Change U8 PCB footprint from PSOP_8_PGA to PSOP_8_PG (to match PCB layout).<br>Change ZZ-PCB1 description, i.e. size 120x85x1mm and name of PCB (DVK-BL652-B0).<br>Add secondary source 19-217/BHC-ZL1M2RY/3T to D1, D2, D3.<br>Add Chern-Yi 43-1P battery holder as secondary source for J34.<br>Added Mag. Layers MCM-9070M-301 as secondary source for CMF1.<br>Add U6 and U9 secondary source RT9187GSP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15Aug2016  | 1.0                | RK       | Release.<br>Change R25 from 10K to NOPOP. Change PCB decription from DVK-BL652-B0 to DVK-BL652-1.0.<br>Add Block Diagram.<br>Move jumper from J12pin2-1 to J12pin2-3 (so default is nAutoRUN mode). Add jumper on J6pin2-1 (connect temperature sensor to BL652).<br>Make R111 0R a NOPOP.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

## PCB design specification

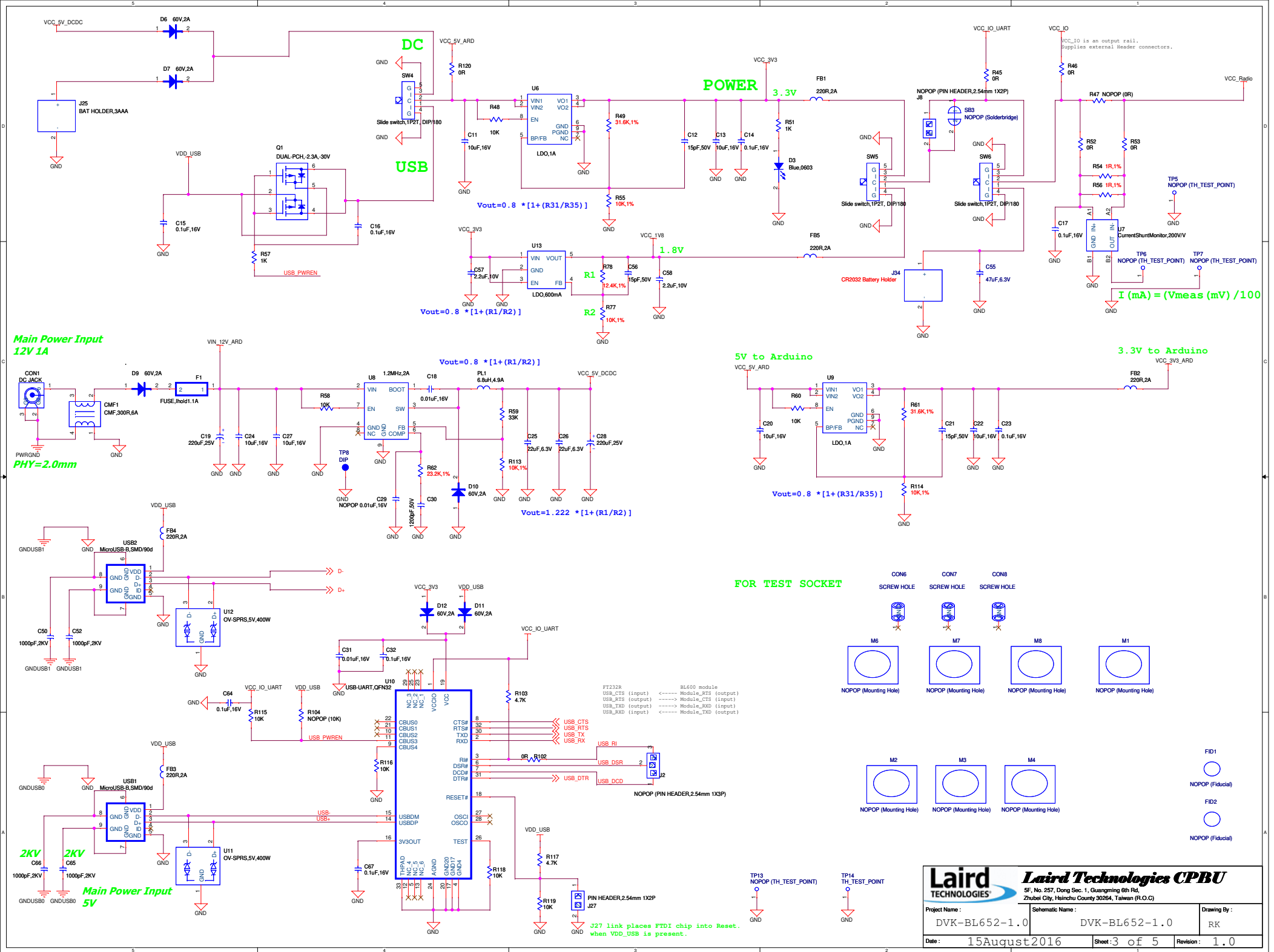
1. Substrate: FR4 ROHS compliant, High TG 140 degree.
2. Solder mask, color=BLUE, Silkscreen color=WHITE
3. Surface finish to be Immersion Nickel/Gold (ENIG) with 1-2 u"
4. Start with 1/2 oz. copper on all layers.

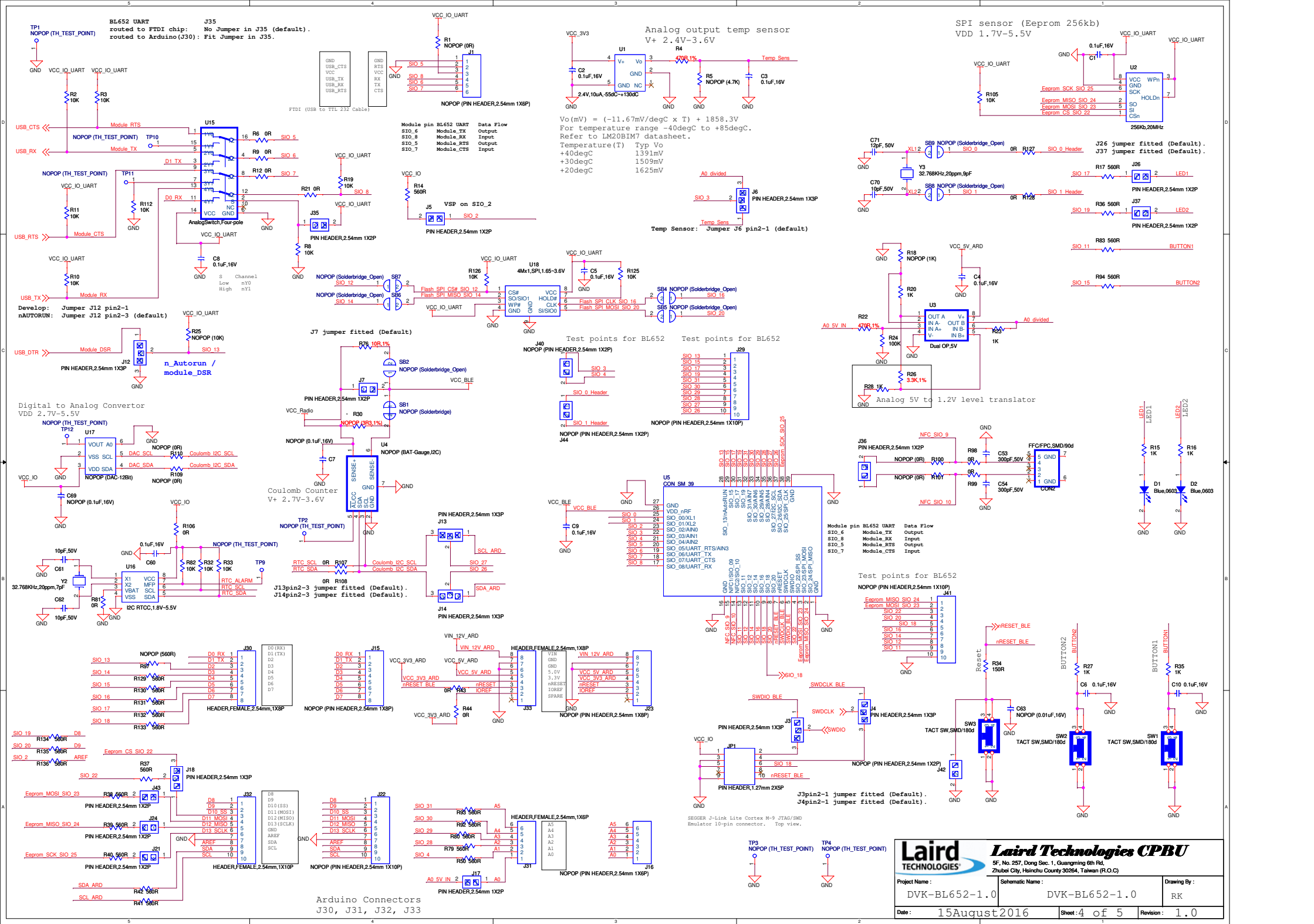
ZZ-PCB1



PCB Substrate

|                                 |  |                                                                                                                                                    |  |
|---------------------------------|--|----------------------------------------------------------------------------------------------------------------------------------------------------|--|
| <b>Laird</b><br>TECHNOLOGIES    |  | <b>Laird Technologies CPBU</b><br><small>5F, No. 257, Dong Sec. 1, Guangming 6th Rd,<br/>Zhubei City, Hsinchu County 30264, Taiwan (R.O.C)</small> |  |
| Project Name :<br>DVK-BL652-1.0 |  | Schematic Name :<br>DVK-BL652-1.0                                                                                                                  |  |
| Date : 15August2016             |  | Drawing By :<br>RK                                                                                                                                 |  |
| Sheet : 2 of 5                  |  | Revision : 1.0                                                                                                                                     |  |

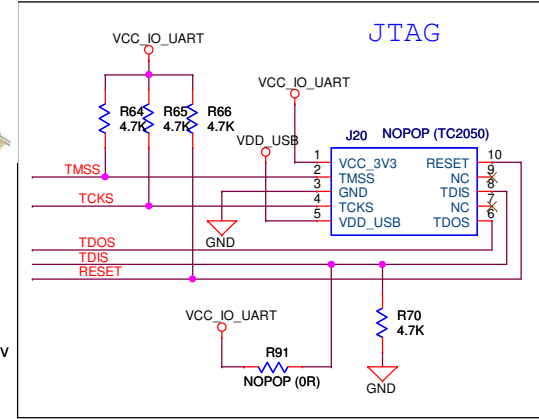
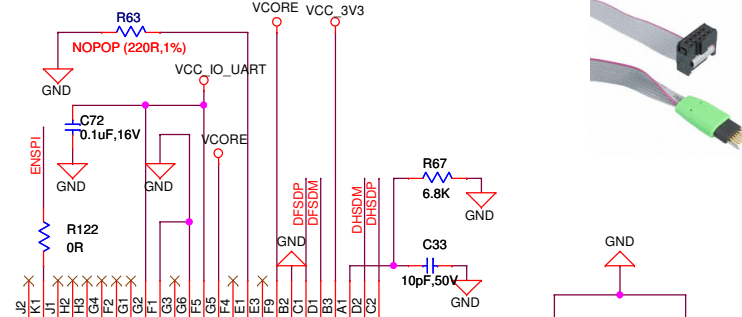
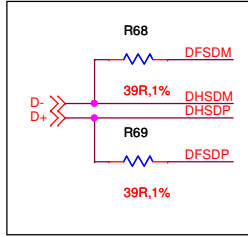




# JLINK

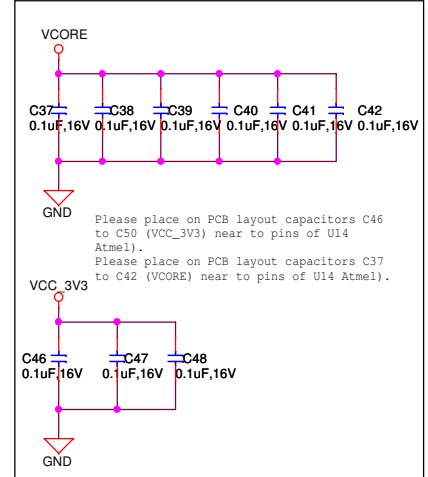
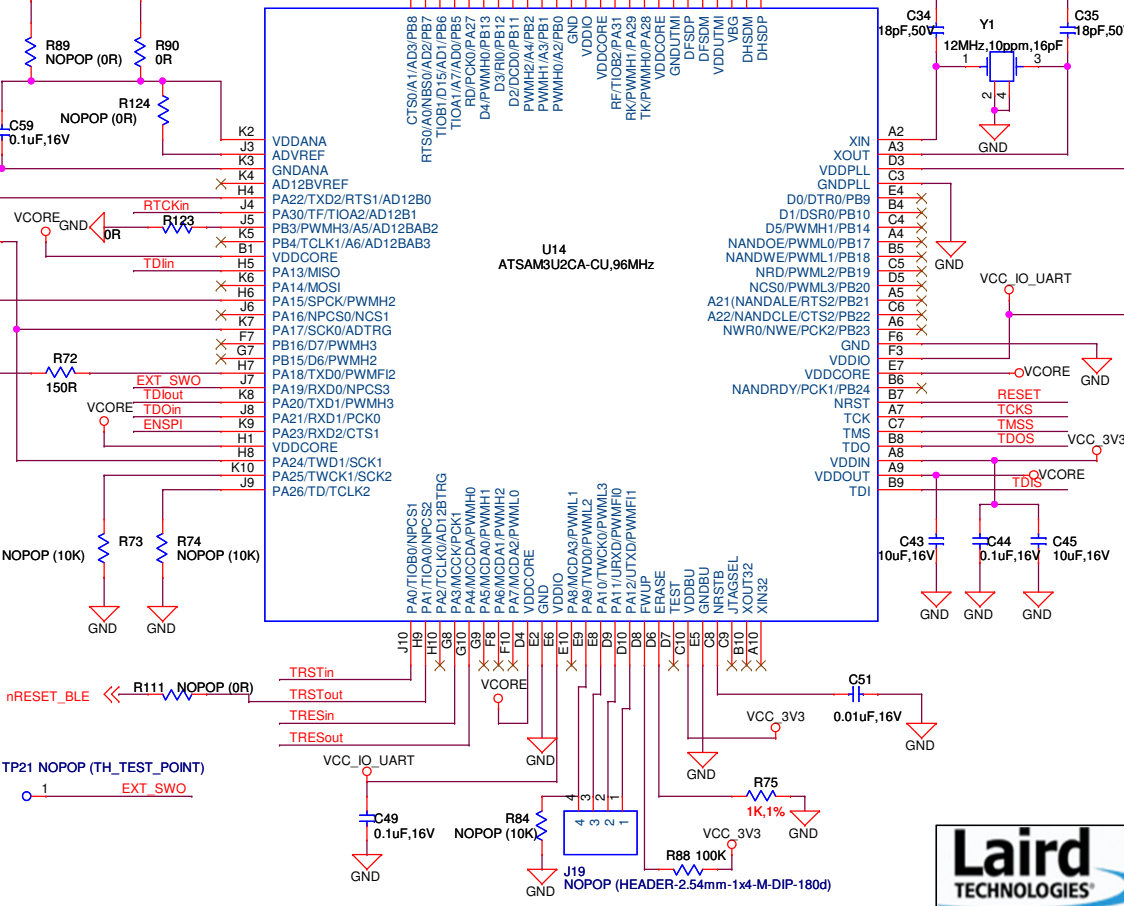
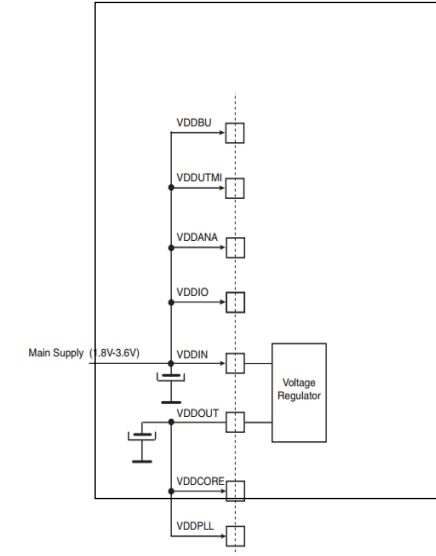
# Close to MCU

| Net        | ATSAM3U2CA | BL652 module |
|------------|------------|--------------|
| SWDCLK     | H4+K7+H8   | Pin6         |
| SWDIO      | H7+G7      | Pin5         |
| nRESET_BLE | H9 (PA1)   | Pin7         |
| SIO.18     | J8 (PA21)  | Pin9         |



Wire nRF52 PO.21 (nRESET\_BLE) to ATSAM PA1.  
Wire nRF52 PO.18 (SWO) to ATSAM PA21.

TO BL652



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|                                 |                                   |                    |
|---------------------------------|-----------------------------------|--------------------|
| Project Name :<br>DVK-BL652-1.0 | Schematic Name :<br>DVK-BL652-1.0 | Drawing By :<br>RK |
| Date :<br>15August2016          | Sheet : 5 of 5                    | Revision : 1.0     |