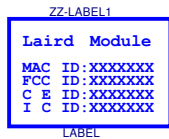
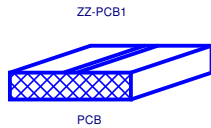


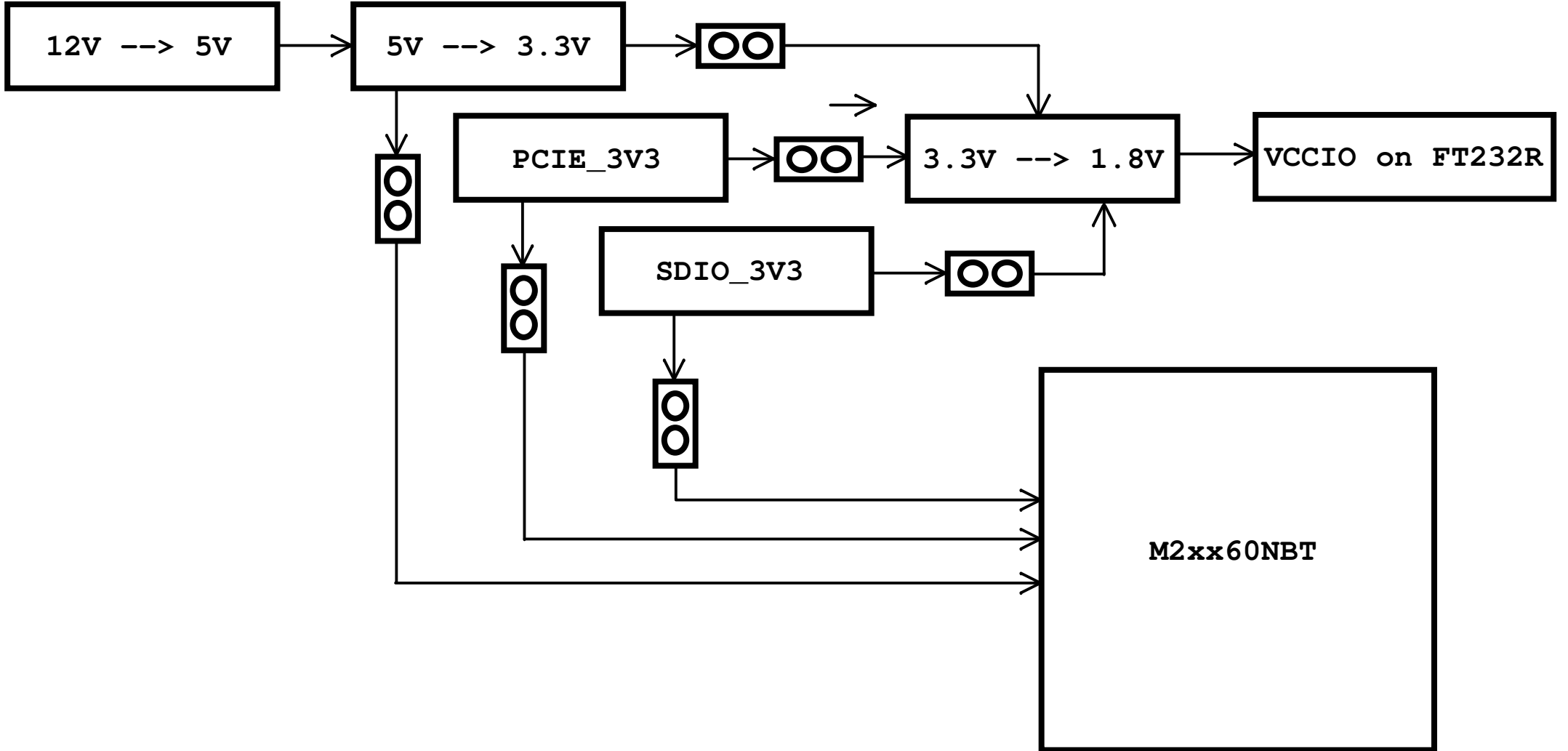
DATE	REVISION NUMBER	INITIALS	INITIAL RELEASE
2016/08/17	A0	Kai Wei	Initial Draft
2016/09/12	A0	Kai Wei	Clean up for EVT design review
2016/09/19	A0	Kai Wei	1. Add TP1 and J23. 2. Change R50,R51,R52 from 1K to 0R.
2016/09/30	B0	Kai Wei	1. Add R62,R63,R64 and TP1
2017/05/26	1.0	Kai Wei	Swap NET name : PMU_EN and PCIE_W_DISABLE_N
2017/08/31	1.1	Kai Wei	Add WOW and WOBT

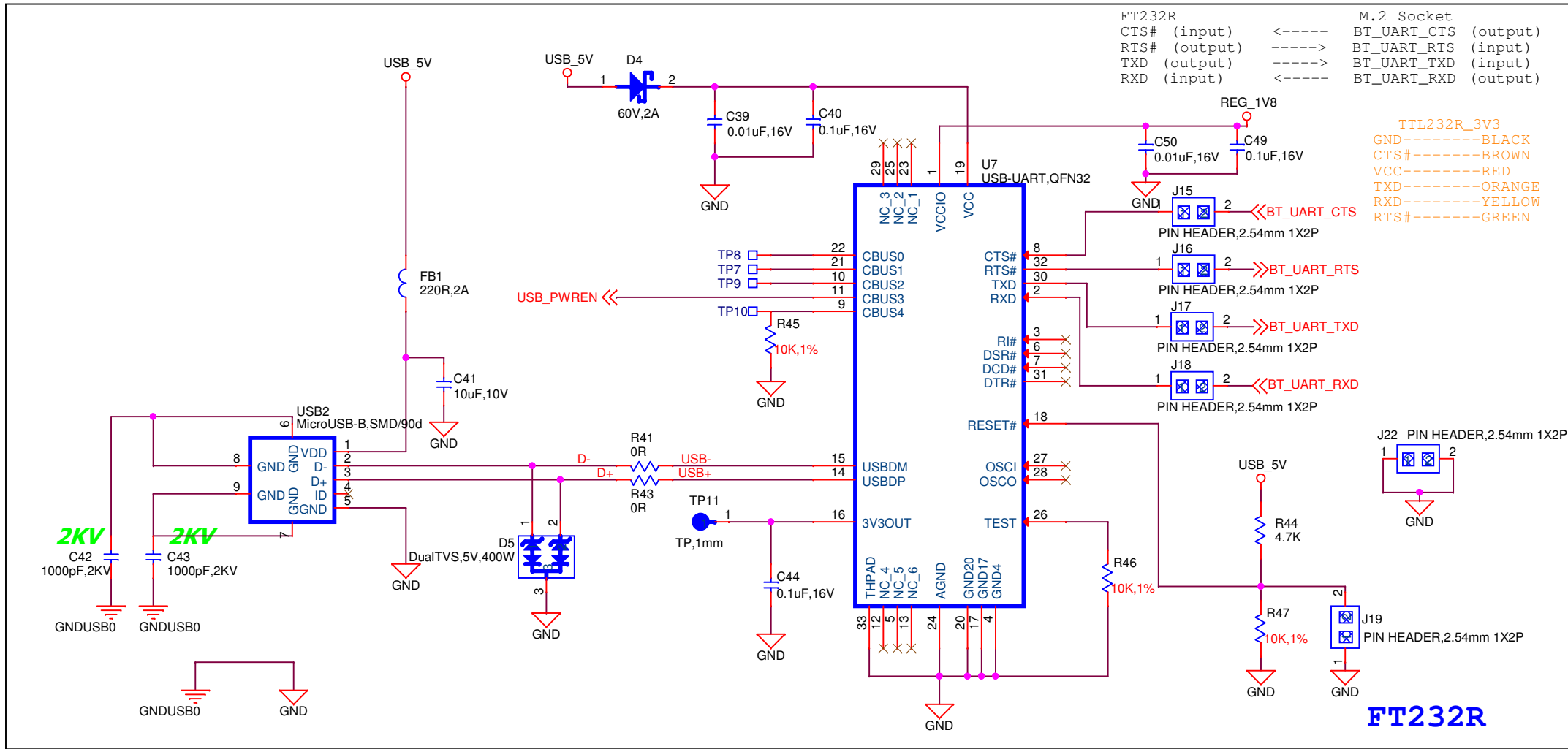
PCB design specification

1. Substrate: FR4 ROHS compliant, TG 140 degree.
2. Solder mask color=BLUE, Silkscreen color=WHITE
3. Surface finish to be Immersion Nickel/Gold (ENIG) with 1-2 u"
4. Start with 1/2 oz. copper on all layers.



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Project Name :	Schematic Name :	Drawing By :
DVK-60-2230C	DVK-60-2230C_Title and History	<Kai Wei>
Date : Monday, September 11, 2017	Sheet : 2 of 6	Revision : 1.1



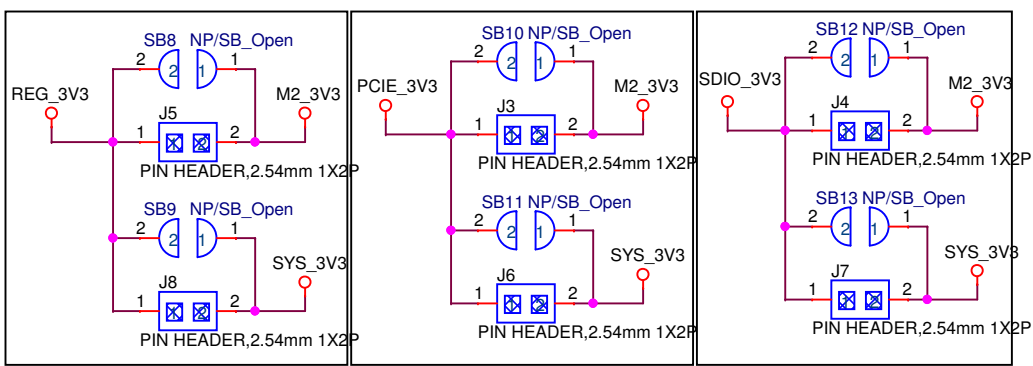


FT232R
CTS# (input) <----->
RTS# (output) <----->
TXD (output) <----->
RXD (input) <----->

M.2 Socket
BT_UART_CTS (output)
BT_UART_RTS (input)
BT_UART_TXD (input)
BT_UART_RXD (output)

TTL232R_3V3
GND-----BLACK
CTS#-----BROWN
VCC-----RED
TXD-----ORANGE
RXD-----YELLOW
RTS#-----GREEN

FT232R

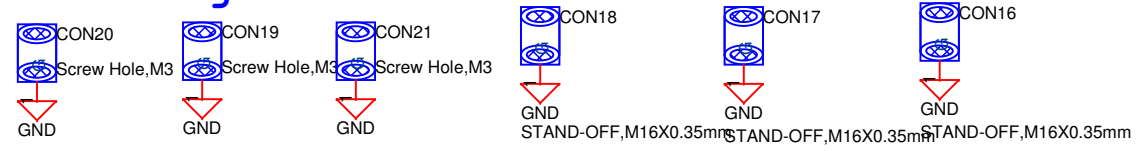


REG_3V3

PCIE_3V3

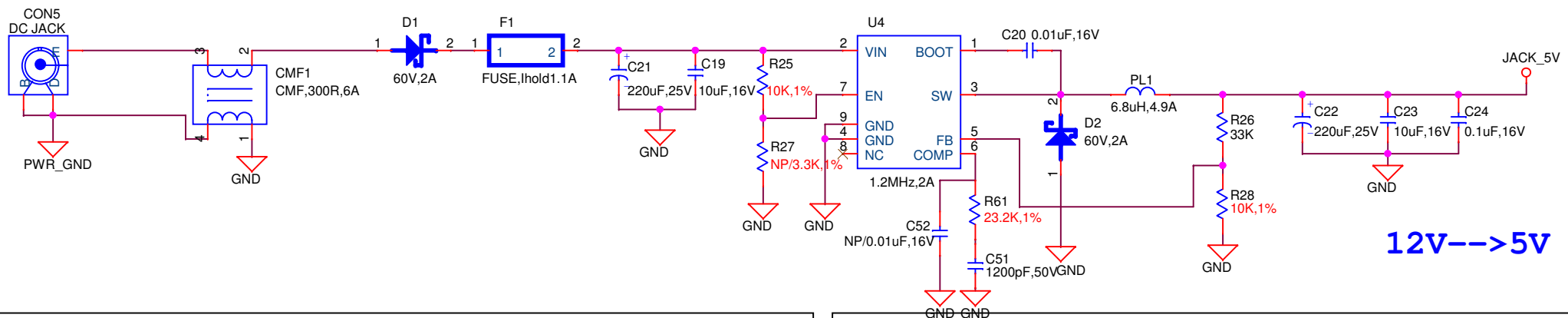
SDIO_3V3

Mounting Hole

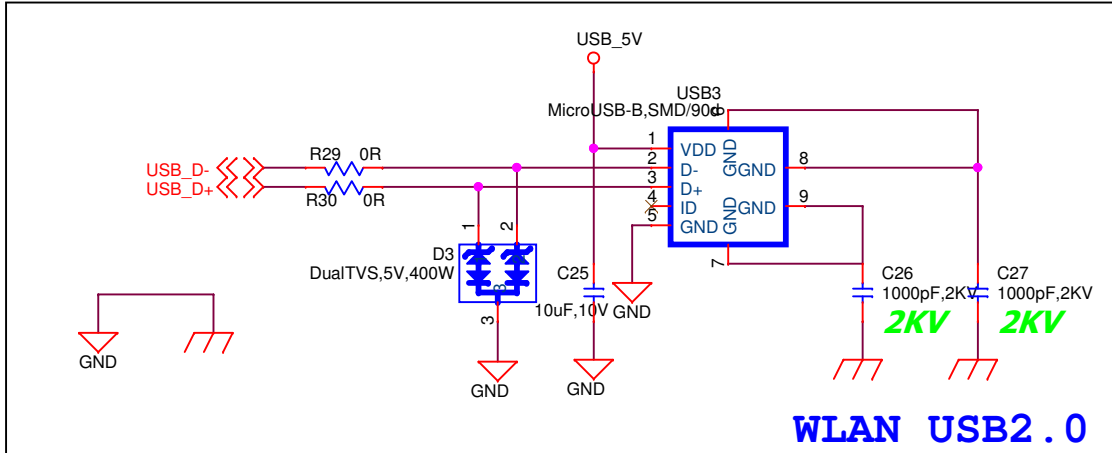


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Zhubei City, Hsinchu County 30264, Taiwan (R.O.C)

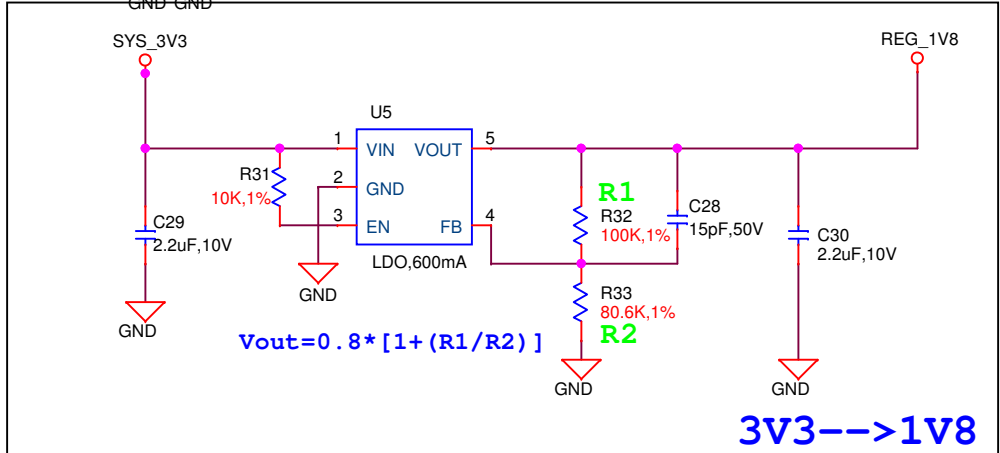
Project Name : DVK-60-2230C	Schematic Name : DVK-60-2230C_Interface	Drawing By : <Kai Wei>
Date : Monday, September 11, 2017		Sheet : 4 of 6
Revision : 1.1		



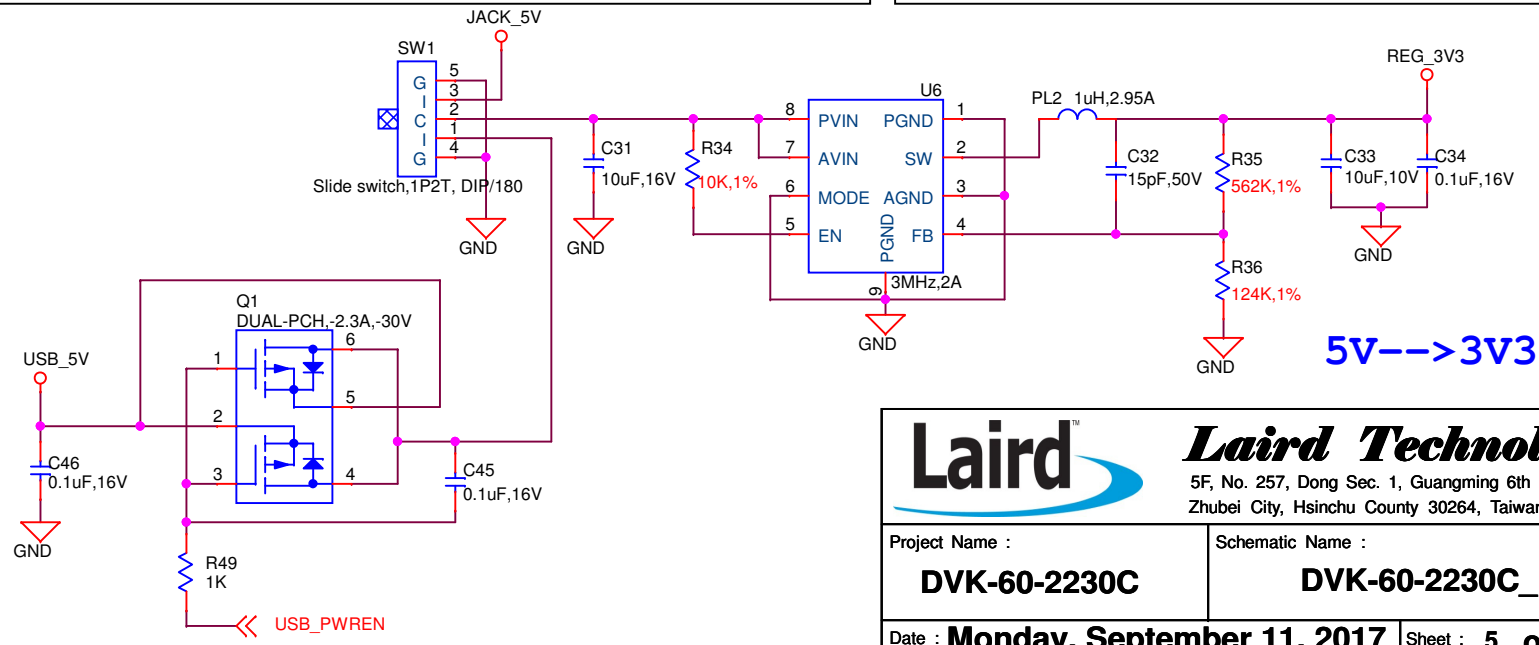
12V-->5V



WLAN USB2.0

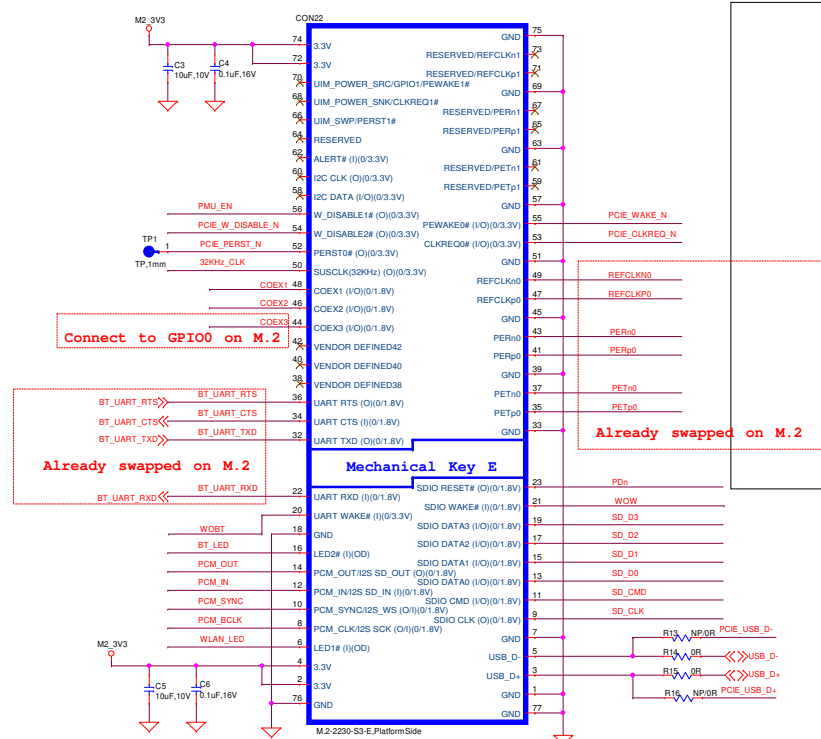
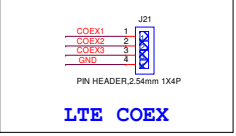
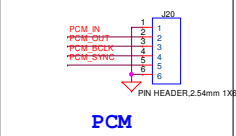
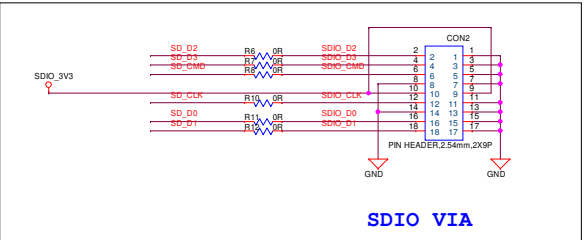
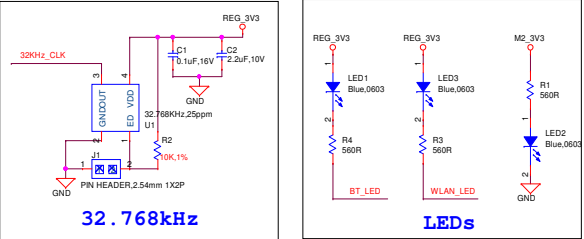


3V3-->1V8



5V-->3V3

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Project Name : DVK-60-2230C	Schematic Name : DVK-60-2230C_Power
Drawing By : <Kai Wei>	
Date : Monday, September 11, 2017	Sheet : 5 of 6
Revision : 1.1	



Connect to GPIO0 on M.2

Already swapped on M.2

Already swapped on M.2

