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Application Note v1.0

BACKGROUND

The objective of the LT1110 development team is to maintain backwards compatibility between new versions of firmware and former versions of firmware. Recently, when scrutinizing timing on a logic analyzer between versions of firmware, we observed that timing had changed slightly between versions of firmware. We cannot go back in time and correct the timing of the affected versions. We determined that the best course of action was to revert timing back to be compatible with the original production versions and provide instructions for reconfiguring the timing to be compatible with either timing variation.

AFFECTED VERSIONS

This issue only affects RF Profile 0x04 (230 kbps RF rate, FEC disabled). The following table (Table 1) shows the timing variations:

Table 1: Timing variations

Firmware Version	Default Timing Configuration	
v0 – v4.1	Timing Configuration A	
v4.2 – v5.6	Timing Configuration B	
v5.7 and beyond	Timing Configuration A	

COMPATIBILITY INSTRUCTIONS

Table 2 shows the EEPROM configuration settings required for compatible timing between the versions when individual networks contain radios using a mix of firmware versions where the default timing configuration is different.

Table 2: EEPROM configuration settings

Firmware Version	Default Configuration (Preferred Setting)	Timing Configuration A	Timing Configuration B
v0 - v4.1	Timing Configuration A: Address 0x45, bit 7: Set Address 0x56, bit 5: Set	 Address 0x45, bit 7: Set Address 0x56, bit 5: Set 	 Address 0x45, bit 7: Clear Address 0x56, bit 5: Clear v0 - v3.7: Address 0x30 = 0x00 v3.8 - v4.1: Address 0x30 = 0x62 Address 0x31 = 0x5B Address 0x32 = 0x7E Address 0x34 = 0x02 Address 0x35 = 0x3B Address 0x36 = 0x05

Memory Map and Firmware

Application Note



Firmware Version	Default Configuration (Preferred Setting)	Timing Configuration A	Timing Configuration B
v4.2 - v5.6	Timing Configuration B:	Upgrade firmware to v5.7 or	 Address 0x37 = 0x06 Address 0x3B = 0x31 Address 0x3C = 0x09 Address 0x46 = 0x3C Address 0x50 = 0x01 Address 0x45, bit 7: Set
	Address 0x45, bit 7: SetAddress 0x56, bit 5: Set		 Address 0x56, bit 5: Set
v5.7 and beyond	Timing Configuration A: Address 0x45, bit 7: Set Address 0x56, bit 5: Set	 Address 0x45, bit 7: Set Address 0x56, bit 5: Set 	 Address 0x45, bit 7: Clear Address 0x56, bit 5: Clear Address 0x30 = 0x62 Address 0x31 = 0x5B Address 0x32 = 0x7E Address 0x34 = 0x02 Address 0x35 = 0x3B Address 0x36 = 0x05 Address 0x37 = 0x19 Address 0x3B = 0x31 Address 0x3C = 0x09 Address 0x46 = 0x3C Address 0x50 = 0x01

REVISION HISTORY

Version	Date	Notes	Approver
1.0	26 Sept 2016	Initial Release	N. Zach Hogya